Single Phase to Three Phase Converter with a Variation-Tolerant Phase Shifting Technique by Two Phase Interleaved PFC Boost Converter

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Abstract: This paper presents a two-phase interleaved critical conduction mode (CRM) power factor correction boost converter with a variation-tolerant phase shifter (VTPS), which ensures accurate 180° phase shift between the two interleaved converters, which converts single phase 230V to three phase 410V. A feedback loop similar to a phase-locked loop controls the amount of the phase shifting of the VTPS. The proposed VTPS has better immunity of process, supply, and temperature variations than the conventional phase shifter. This boosted DC source applied to a hybrid multilevel inverter, It consists of a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. The three phase inverter output voltages, harmonic performance of induction machine current, induction machine outputs and THD is available by using simulation of MATLAB/SIMULINK software.

Keywords: Critical conduction mode (CRM), interleaved boost converter, multilevel inverter (MLI), power factor correction (PFC), variation-tolerant phase shifter (VTPS).

1. Introduction

In recent years, three phase applications increases for high power industries. Mostly single phase wiring adopted in rural areas, but the rural small industries require three phase supply. Single phase to three phase converters required.

POWER factor (PF) defined as the ratio of real power to apparent power is desired to be 100% because the smaller the PF, the larger the power loss and harmonics, which may travel down the power line and disrupt other devices connected to the line [1], [2]. For a higher PF, a power factor correction (PFC) circuit is employed which shapes the input current waveform to be in phase with the input voltage waveform [3]. PFC circuits can be classified as either passive or active PFC among which active PFC is preferred due to its small form factor and higher PF [4]. The operation modes of an active PFC converter can be classified as either continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM) depending on the current flowing through the inductor [3]. For a heavy load, the CCM is usually employed because it can handle more current than the DCM and CRM [5]. At the CCM, however, the hard switching of the freewheeling diode may result in decreased power conversion efficiency. On the contrary, the freewheeling diode is switched softly at the DCM and CRM and thus higher power efficiency can be expected.

For an interleaved power converter operating at the CRM, a master–slave scheme has been widely used [7]–[20]. Among the multiple paralleled converters, a master converter operates as a stand-alone one, while the switching of the other converter, that is, a slave converter, is synchronized with that of the master. For a two-phase interleaved converter, a phase shifter measuring the switching period of the master converter can be used to generate the switching signal of the slave converter, so its switching instant is 180° out of phase from that of the master converter [7]. The simplest way of measuring the switching period of the master converter is to use a ramp generator with UP and DOWN current sources [7]. The mismatch between the two current sources, however, results in the error of the phase shifting, increasing the current ripple Δim. A sample-and-hold circuit can be used to measure the period where only one current source is required [8]. The sampling capacitor has to be discharged at every cycle and the time required for this results in phase shifting error.

The basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. Hybrid multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. The multilevel inverter has gained much attention in recent years due to its advantages in high power possibility with low switching frequency and low harmonics.

In this paper, a two-phase PFC boost converter operating at the CRM is described which employs a variation-tolerant phase shifter (VTPS) ensuring the accurate 180° phase shifting. Input 230V is converted into DC source step up into 410V, this single dc source converted into three phase supply by hybrid multilevel inverter.
2. Proposed concept of single phase to three phase with a Two-Phase Interleaved CRM PFC Boost Converter With A VTPS

Fig. 1 shows the block diagram of the two-phase interleaved PFC boost converter with the proposed VTPS operating at the CRM of single phase to three phase. The upper converter consisting of \( L_M, D_M, \) and \( S_M \) is the master and the lower one consisting of \( L_S, D_S, \) and \( S_S \) is the slave. The output voltage level is compared with the reference level generated by the bandgap reference (BGR) to generate the error voltage \( V_{COMP} \). For the master converter, the fixed slope ramp signal \( V_{RM} \) is compared with the error voltage \( V_{COMP} \) and the switching signal \( \Phi_M \) becomes LOW when \( V_{RM} \) is larger than \( V_{COMP} \), decreasing the inductor current \( I_M \). The voltage level of the secondary winding of the transformers is utilized to detect the zero current of the primary winding. The zero current detector (ZCD) generates the pulse \( V_{DTM} \), setting \( \Phi_M \) to HIGH when the voltage level of the secondary winding is lower than the reference level.

The operation of the slave converter is similar to that of the master except that the slope of the ramp signal \( V_{RS} \) is variable to get the accurate 180° phase difference between the master and slave converters. The slope of \( V_{RS} \) is adjusted by the phase shifting loop consisting of the phase-frequency detector (PFD), charge pump (CP), loop filter, and ramp generator, so the rising edge of the ZCD output \( V_{DTS} \) of the slave converter is locked to that of \( \Phi_{HP} \) which is 180° phase shifted from \( V_{DTM} \) by the phase shifter. Because the switch \( SS \) of the slave converter is turned ON by the rising edge of \( V_{DTS} \), the turn-ON instant of the slave converter is 180° phase shifted from that of the master converter. Fig. 1(a) shows the proposed VTPS block diagram, while the conventional phase shifter requires UP and DOWN current sources whose matching is critical but cannot be very good, the proposed one requires only UP current sources, which can be easily matched. A Monte Carlo simulation has been performed to see the achievable accuracy of the phase shift under environmental variations and the results. The x-axis is the phase difference between the input signal \( V_{DTM} \) and the output signal \( \Phi_{HP} \), and the y-axis represents the number of events. In order to compare the phase shifting accuracy with the conventional ones, the conventional phase shifters with UP and DOWN current sources [7] and with a sample-and-hold circuit [8] are also simulated. As can be seen in the figure, the

The proposed hybrid multilevel inverter, the bottom is one leg of a standard 3-leg inverter with a dc power source. The top is an H-bridge in series with each standard inverter leg. The H-bridge can use a separate dc power source or a capacitor as the dc power source. Single phase (230V) is converted into DC (230V) by bridge rectifier with two phase interleaved CRM PFC boost converter with a VTPS. Then, this boosted voltage (400V) applied to hybrid multilevel inverter which converted into three phase five level inverter. The output voltage \( v1 \) of this leg (with respect to the ground) is either \( +\frac{V_{dc}}{2} \) (S5 closed) or \( -\frac{V_{dc}}{2} \) (S6 closed). This leg is connected in series with a full H-bridge which in turn is
supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S1, S4 closed), 0 (S1, S2 closed or S3, S4 closed), or $-V_{dc}/2$ (S2, S3 closed). When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage.

When only a dc power source is used in the inverter, that is, the H-bridge uses a capacitor as the dc power source, the capacitor’s voltage regulation control. During $\theta_1 \leq \theta \leq \pi$, the output voltage is zero and the current $i > 0$. If S1, S4 are closed (so that $v_2 = +V_{dc}/2$) along with S6 closed (so that $v_1 = -V_{dc}/2$), then the capacitor is discharging ($i_c = -i < 0$ ) and $v = v_1 + v_2 = 0$. On the other hand, if S2, S3 are closed (so that $v_2 = -V_{dc}/2$) and S5 is also closed (so that $v_1 = +V_{dc}/2$), then the capacitor is charging ($i_c = i > 0$) and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, S5 are closed depending on whether it is necessary to charge or discharge the capacitor.

3. Simulation Results

In order to verify the performance of the proposed single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter. The following are results of proposed concept.

![Figure 3: Single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter.](image)

Fig.4. shows the three phase output voltage of proposed converter. Fig.5. shows the PFC boost converter voltage. The PFC boost converter provides 410V dc output from the ac input line voltage of $230*1.4142$ V RMS. In Fig.6, the PF and power efficiency of the PFC boost converter are shown for the input line voltage of 325.26 V RMS with the proposed VTPS.
4. Conclusion

A simulation model for the Single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter hybrid multilevel inverter is developed in MATLAB/SIMULINK. The three phase inverter output is a 5-level phase voltage. The PFC boost converter with the proposed phase shifter shows the lowest input current ripple because the proposed variation-tolerant phase shifter provides the most accurate 180° phase shift. From results it is clear about that, single phase to three phase possible with effective power factor, low ripple in DC voltage and better three phase voltage.

References


