

Single Phase to Three Phase Converter with a Variation-Tolerant Phase Shifting Technique by Two Phase Interleaved PFC Boost Converter

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Abstract: This paper presents a two-phase interleaved critical conduction mode (CRM) power factor correction boost converter with a variation-tolerant phase shifter (VTPS), which ensures accurate 180° phase shift between the two interleaved converters, which converts single phase 230V to three phase 410V. A feedback loop similar to a phase-locked loop controls the amount of the phase shifting of the VTPS. The proposed VTPS has better immunity of process, supply, and temperature variations than the conventional phase shifter. This boosted DC source applied to hybrid multilevel inverter, It consists of a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. The three phase inverter output voltages, harmonic performance of induction machine current, induction machine outputs and THD is available by using simulation of MATLAB/SIMULINK software.

Keywords: Critical conduction mode (CRM), interleaved boost converter, multilevel inverter (MLI), power factor correction (PFC), variation-tolerant phase shifter (VTPS).

1. Introduction

In recent years, three phase applications increases for high power industries. Mostly single phase wiring adopted in rural areas, but the rural small industries require three phase supply. Single phase to three phase converters required.

POWER factor (PF) defined as the ratio of real power to apparent power is desired to be 100% because the smaller the PF, the larger the power loss and harmonics, which may travel down the power line and disrupt other devices connected to the line [1], [2]. For a higher PF, a power factor correction (PFC) circuit is employed which shapes the input current waveform to be in phase with the input voltage waveform [3]. PFC circuits can be classified as either passive or active PFC among which active PFC is preferred due to its small form factor and higher PF [4]. The operation modes of an active PFC converter can be classified as the continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM) depending on the current flowing through the inductor [3]. For a heavy load, the CCM is usually employed because it can handle more current than the DCM and CRM [5]. At the CCM, however, the hard switching of the freewheeling diode may result in decreased power conversion efficiency. On the contrary, the freewheeling diode is switched softly at the DCM and CRM and thus higher power efficiency can be expected.

For an interleaved power converter operating at the CRM, a master-slave scheme has been widely used [7]–[20]. Among the multiple paralleled converters, a master converter operates as a stand-alone one, while the switching of the other converter, that is, a slave converter, is synchronized with that of the master. For a two-phase interleaved converter, a phase shifter measuring the switching period of

the master converter can be used to generate the switching signal of the slave converter, so its switching instant is 180° out of phase from that of the master converter [7]. The simplest way of measuring the switching period of the master converter is to use a ramp generator with UP and DOWN current sources [7]. The mismatch between the two current sources, however, results in the error of the phase shifting, increasing the current ripple ΔI_{in} . A sample-and-hold circuit can be used to measure the period where only one current source is required [8]. The sampling capacitor has to be discharged at every cycle and the time required for this results in phase shifting error.

The basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. Hybrid multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. The multilevel inverter has gained much attention in recent years due to its advantages in high power possibility with low switching frequency and low harmonics.

In this paper, a two-phase PFC boost converter operating at the CRM is described which employs a variation-tolerant phase shifter (VTPS) ensuring the accurate 180° phase shifting. Input 230V is converted into DC source step up into 410V, this single dc source converted into three phase supply by hybrid multilevel inverter.

supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S1, S4 closed), 0 (S1, S2 closed or S3, S4 closed), or $-V_{dc}/2$ (S2, S3 closed). When the output voltage $v = v1 + v2$ is required to be zero, one can either set $v1 = +V_{dc}/2$ and $v2 = -V_{dc}/2$ or $v1 = -V_{dc}/2$ and $v2 = +V_{dc}/2$. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage.

When only a dc power source is used in the inverter, that is, the H-bridge uses a capacitor as the dc power source, the capacitor's voltage regulation control. During $\theta1 \leq \theta \leq \pi$, the output voltage is zero and the current $i > 0$. If S1, S4 are closed (so that $v2 = +V_{dc}/2$) along with S6 closed (so that $v1 = -V_{dc}/2$), then the capacitor is discharging ($ic = -i < 0$) and $v = v1 + v2 = 0$. On the other hand, if S2, S3 are closed (so that $v2 = -V_{dc}/2$) and S5 is also closed (so that $v1 = +V_{dc}/2$), then the capacitor is charging ($ic = i > 0$) and $v = v1+v2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, S5 are closed depending on whether it is necessary to charge or discharge the capacitor.

3. Simulation Results

In order to verify the performance of the proposed single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter. The following are results of proposed concept.

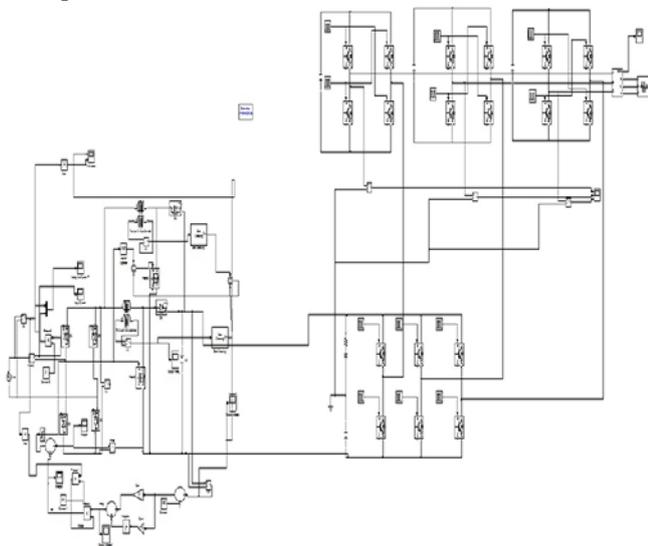


Figure 3: Single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter.

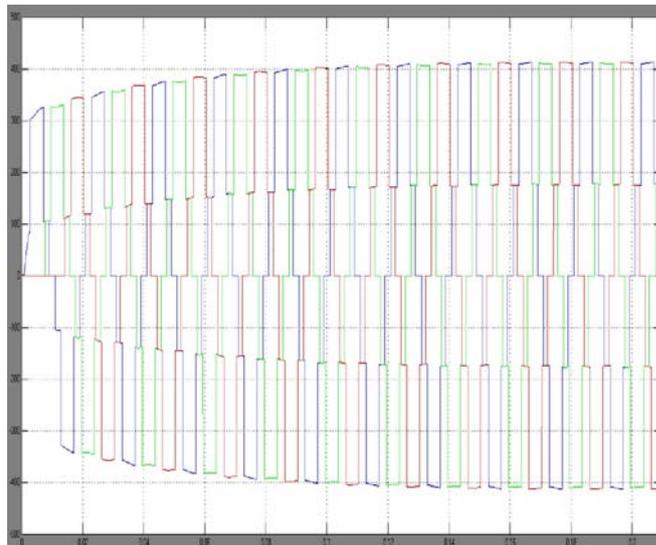


Figure 4: Three Phase output voltage.

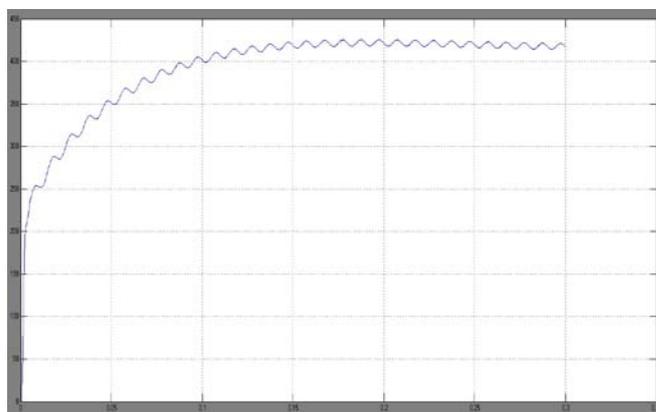


Figure 5: Boost converter DC voltage.



Figure 6: Single phase Power Factor.

Fig.4. shows the three phase output voltage of proposed converter. Fig.5. shows the PFC boost converter voltage. The PFC boost converter provides 410V dc output from the ac input line voltage of 230×1.4142 VRMS. In Fig.6, the PF and power efficiency of the PFC boost converter are shown for the input line voltage of 325.26 VRMS with the proposed VTPS.

4. Conclusion

A simulation model for the Single phase to three phase converter with a Variation-Tolerant Phase Shifting Technique by two phase interleaved PFC Boost Converter hybrid multilevel inverter is developed in MATLAB/SIMULINK. The three phase inverter output is a 5-level phase voltage. The PFC boost converter with the proposed phase shifter shows the lowest input current ripple because the proposed variation-tolerant phase shifter provides the most accurate 180° phase shift. From results it is clear about that, single phase to three phase possible with effective power factor, low ripple in DC voltage and better three phase voltage.

References

- [1] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol.35, no. 1, Jan./Feb. 1999, pp. 36.
- [2] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no.3, May. /June 1996, pp. 509-517.
- [3] J. Rodríguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, Aug. 2002, pp. 724-738.
- [4] S. Onoda, A. Emadi, "PSIM-based modeling of automotive power systems: conventional, electric, and hybrid electric vehicles" *IEEE Transactions on Vehicular Technology*, vol. 53, issue 2, 2004, pp. 390-395.
- [5] D. Zhong B. Ozpineci, L. M. Tolbert, J. N. Chiasson, "Inductorless DCAC cascaded H-Bridge multilevel boost inverter for electric/hybrid electric vehicle applications," *IEEE Industry Applications Conference*, Sept. 2007, pp. 603-608.
- [6] M. S. Elmore, "Input current ripple cancellation in synchronized parallel connected critically continuous boost converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 1996, pp. 152–158.
- [7] J. R. Tsai, T. F. Wu, C. Y. Wu, Y. M. Chen, and M. C. Lee, "Interleaving Phase shifters for critical-mode boost PFC," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1348–1357, May 2008.
- [8] X. Xu, W. Liu, and A. Q. Huang, "Two-phase interleaved critical mode PFC boost converter with closed loop interleaving strategy," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 3003–3013, Dec. 2009.
- [9] J. Zhang, J. Shao, F. C. Lee, and M. M. Jovanovic, "Evaluation of input current in the critical mode boost PFC converter for distributed power systems," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2001, pp. 130-136.
- [10] T. Ishii and Y. Mizutani, "Power factor correction using interleaving technique for critical mode switching converters," in *Proc. IEEE Power Electron. Spec. Conf.*, May 1998, pp. 905–910.
- [11] B. T. Irving, Y. Jang, and M. M. Jovanovic, "A comparative study of softswitched CCM boost rectifiers and Rinterleaved variable-frequency DCM boost rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2000, pp. 171–177.
- [12] C. M. de Oliveira Stein, J. R. Pinheiro, and H. L. Hey, "A ZCT auxiliary commutation circuit for interleaved boost converters operating in critical conduction mode," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 954–962, Nov. 2002.
- [13] T. F. Wu, J. R. Tsai, Y. M. Chen, and Z. H. Tsai, "Integrated circuits of a PFC controller for interleaved critical-mode boost converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2007, pp. 1347–1350.
- [14] C. P. Ku, D. Chen, C. S. Huang, and C. Y. Liu, "A novel SFVM-M3 control scheme for interleaved CCM/DCM boundary-mode boost converter in PFC applications," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2295–2303, Aug. 2011.
- [15] L. Huber, B. T. Irving, and M. M. Jovanovic, "Open-loop control methods for interleaved DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.
- [16] A. Jansen, "Master-Slave Critical Conduction Mode Power Converter," U.S. Patent Application 2006/0077604, Apr. 13, 2006.
- [17] B. Lu, "A novel control method for interleaved transition mode PFC," in *Proc. Appl. Power Electron. Conf.*, Feb. 2008, pp. 697–701.
- [18] L. Huber, B. T. Irving, and M. M. Jovanovic, "Review and stability analysis of PLL-based interleaving control of DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1992–1999, Aug. 2009.
- [19] H. Choi and L. Balogh, "A cross-coupled master-slave interleaving method for boundary conduction mode (BCM) PFC converters," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4202–4211, Oct. 2012.
- [20] H. Choi, "Interleaved boundary conduction mode (BCM) buck power factor correction (PFC) converter," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2629–2634, Jun. 2013.