3.2 Direct conversion scheme:

The direct conversion receiver converts the carrier of the desired channel to the zero frequency immediately in the first mixers. Hence the direct conversion is often called as a zero IF receiver, or a homodyne receiver if the LO is coherently synchronised with the incoming carrier. The synchronization of the LO directly to the RF carrier can be avoided with other techniques in current applications used mostly in optical reception.

Homodyne receivers translates the channel of interest directly from RF to baseband(ω_{IF}=0) in a single stage. Hence these architectures are called Direct IF architectures or Zero-IF architectures. For frequency and phase modulated signals, down conversion must provide Quadrature outputs so as to avoid loss of information. It translates the RF signal directly to the baseband signal.

The block diagram of direct conversion receiver is shown in the Fig 4 [14]. Two direct conversion mixers must be used for demodulation already at RF if a signal with Quadrature modulation is received. Otherwise, a single sideband signal with suppressed carrier contains Quadrature information, like QPSK, would alias its own independent single sideband channels in Quadrature over each other. Hence, the RF mixers are already a part of the demodulator although several other processing steps are performed before the detection of bits. This is also a distinct benefit of the direct conversion scheme. Because the information at the both sides of the carrier comes from the same source having an equal power. Hence the image power is always the same with the desired signal and the Quadrature accuracy requirements are only moderate. Thus the required image rejection is realizable with IC technologies even at high frequencies. A low pass filter with a bandwidth of half the symbol rate is suitable for the channel selection. This gives a noise advantages over other architectures and also image noise filtering is needed between the LNA and mixers. The external components in the signal path are now limited to the preselection filter at the input. Hence only the input of LNA must be matched in order to maintain the filter response unchanged. The interfaces between other blocks can be optimized during the design independently to optimize the performance with respect to noise, linearity and power. Of course, flexibility also increases the design complexity.

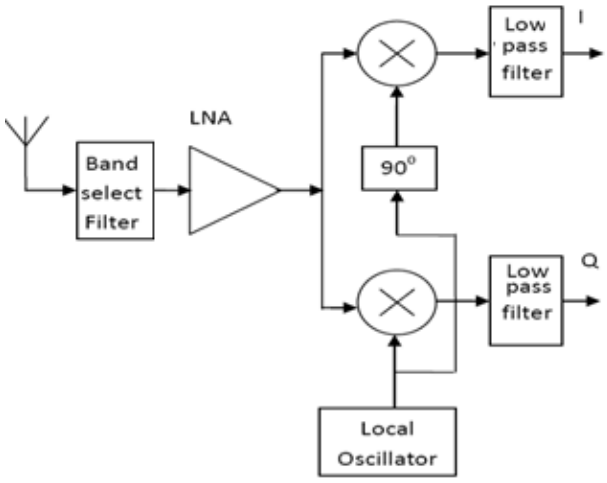

Figure 5: Block diagram of direct conversion receiver

4. Major Functions in Transmitter Design

We used Matlab/Simulink to design ZigBee transmitter design. The functions to be implemented in transmitter are bit to symbol mapping, symbol to chip mapping, serial to parallel conversion, half sine pulse shaping and modulation with high frequency carrier. Initially bit to Chip conversion is achieved by employing direct spread spectrum technique [8]. This spread spectrum technique , serial to parallel conversion and half sine pulse shaping are explained below briefly.
The spread spectrum modulation may be stated as two parts [11].

1. Spread spectrum is a means of transmission in which the data sequence occupies a bandwidth in excess of the minimum bandwidth necessary to send it.
2. The spectrum spreading is accomplished before transmission through the use of a code that is independent of data sequence. The same code is used in the receiver to despread the received signal so that the original data sequence may be recovered.

Spread spectrum modulation was originally developed for military applications, where resistance to jamming is of major concern. However the civilian applications were also benefied from the unique properties of the spread spectrum modulation. For example, in multiple access communications in which a number of independent users are required to share a common communication channel without the external synchronism mechanism, spread spectrum became robust today. There are two types of the spread spectrum techniques.

1. Direct Sequence Spread Spectrum (DSSS)
2. Frequency Hop Spread spectrum (FHSS)

Generally in DSSS, the incoming data sequence is used to modulate a wideband code. This code transforms the narrowband data sequence into a noise like wideband signal. The resulting wideband signal undergoes a second modulation using phase shift keying.

4.1 Serial to Parallel conversion and Half sine pulse shaping

Serial to parallel conversion is implemented by a set of predefined configuration of flip flops, which is explained below([11], [17]). We know that D-flip flop is a one bit storage device. The operation of the D-flip flop is such that at the active edge of the clock waveform, the logic level at D is transferred to the output Q. As a matter of fact, the change in data d(t) will occur slightly after the active edge. Once the flip-flop, in response to an active clock edge, has registered a data bit, it will hold that bit until updated by the occurrence of the next succeeding clock edge.

The mechanism of generating OQPSK waveform is described below [11]. The fundamental circuit for generating the inphase and quadrature data by generating even and odd clock is shown in the Figure 4.3. If we add one more d-flipflop after the D-flipflop at inphase component, we can get QPSK signal. The delay provided by

the D-flipflop should be half of bit duration.

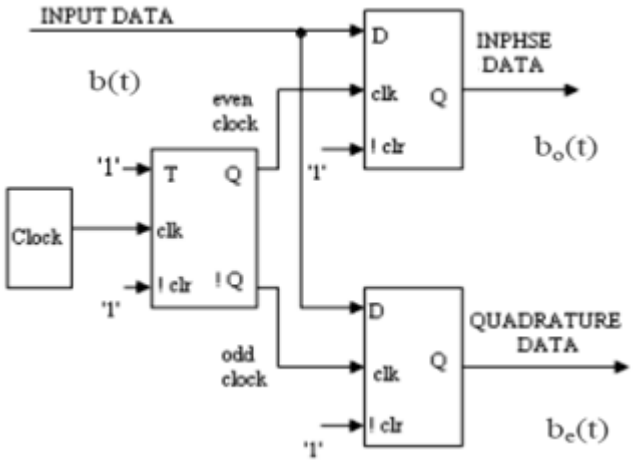

Figure 6: Generation of Inphase and Quadrature data.

Here we have arbitrarily assumed that in every case the active edge of the clock waveforms is the downward edge i.e., negative triggering. We know that T-flip flop toggles its output if the input is „1". Here let the toggle flip-flop is driven by a clock waveform whose period is the bit time T_b. The toggle flip-flop generates an even clock waveform and an odd waveform. These clocks have bit period $2T_b$. The active edge of one of the clocks and the active edge of the other are separated by the bit time T_b. Let the bit stream b(t), which is applied as the data input to both type-D flip flops, one driven by the odd and the other is driven by the even clock waveform. The flip-flops register alternate bits in the bit stream b(t) and hold each such registered bit for two bit intervals, that is for a time $2T_b$. If there are input bit sequence numbered 1,2,3,4 etc., then the bit stream $b_o(t)$ registers bit 1 and holds that bit for time $2T_b$ and next it registers bit 3 for time $2T_b$ and next bit 5 for $2T_b$, etc. The even bit stream $b_e(t)$ holds, for times $2T_b$ each , it results the alternate bits numbered 2,4,6 etc.

Here both $S_e(t)$ and $S_0(t)$ occupy the same spectral range but they are individually identifiable because of the phase Quadrature of the carriers. These four possible output signals have equal amplitude and are in phase quadrature; they have been identified by their corresponding values of b_0 and b_e.

5. Implementation of Zigbee transceiver in Matlab/Simulink

5.1 Design of ZigBee Transmitter

This section describes the implementation of ZIGBEE transmitter system. The implementation was built on Matlab/Simulink using fundamental components in Simulink to demonstrate how reliably complex modulation schemes can be built, cost effectively and efficiently. The design of ZigBee transmitter using OQPSK modulation with half sine pulse shaping is shown in the Figure 5.1 given below ([7], [15]). Here the input bit stream is having a data rate of 250Kbps.

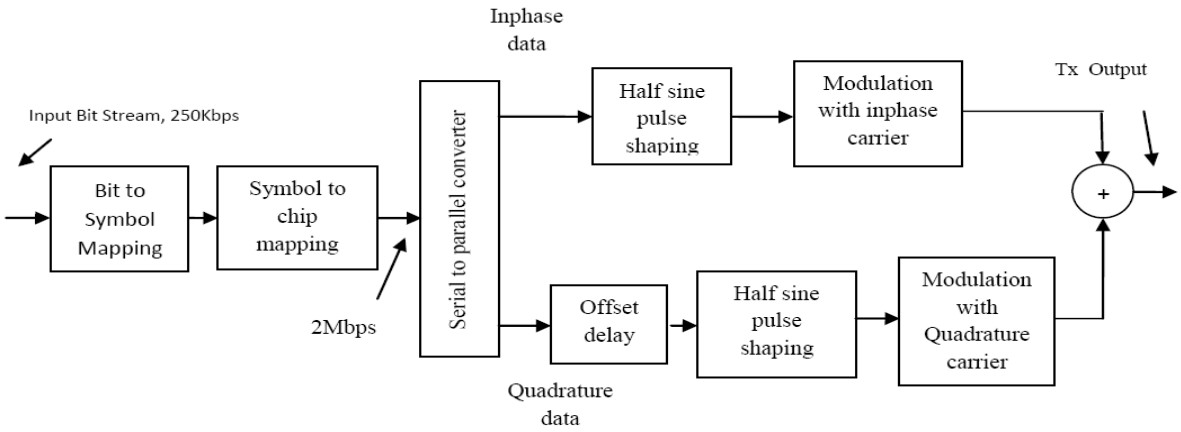

Figure 7: Block diagram of ZigBee Transmitter

Now we are mapping 4 input data bits to a symbol having a symbol rate of 62.5Kilo symbols per second. The symbol is then used to select one of 16 nearly orthogonal 32-chip PN sequences to be transmitted and results in a chip rate of two mega chips per second. After that, resultant chip sequence is send to the serial to parallel converter [8]. It is used here to separate the even indexed chips and odd indexed chips. Following this half sine pulse shaping is performed and signal modulated with a 2.4 GHz carrier on the I and Q data stream and add it to get the required transmitter output signal. Step by step procedure to implement ZigBee transmitter using simulink is presented below.

This section describes the implementation of ZigBee receiver system. Here we are concentrating on the MSK coherent detection technique for recovering original data in receiver. The block diagram of the ZigBee Receiver is shown in Fig 8below.The step by step procedure to implement ZigBee receiver using Simulink is presented below.

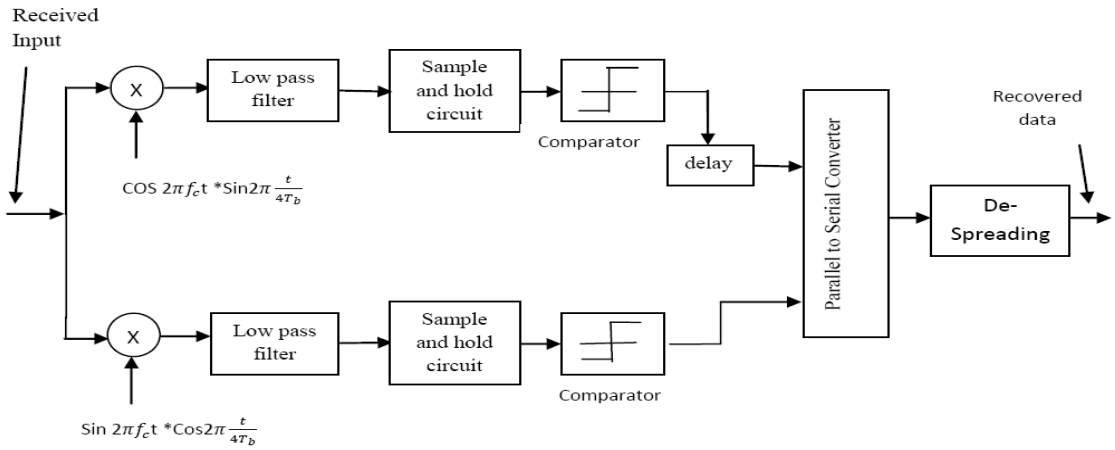

Figure 8: Design of ZigBee Receiver

6. Conclusion

The work presented here helps to implement a transceiver for ZigBee wireless communication system using Matlab/Simulink. Without using mathematically complex blocks, we designed and tested a ZigBee wireless transceiver in Matlab/Simulink. In this thesis previous work of [8]& [15] are used as reference to implement ZigBee transceiver. A model for MSK has been presented, an analysis of which shows that the theoretical maximum bandwidth efficiency of MSK is 2 bits/s/Hz, the same as for QPSK and Offset QPSK.Here, we are indirectly implementing Minimum Shift Keying modulation and demodulation (OQPSK with half sine pulse shaping). As discussed in chapter 4, Half sine pulse shaping avoids the abrupt phase shifts in the transmitted signal so that it reduced lot of burden and the modulated signal is amplifier friendly in real time scenario. Use of direct spread spectrum technique, reduces the interference effects. As discussed in chapter4, out of the three commonly used radio transceivers (superhetrodyne, Low IF and direct conversion transceiver), the use of direct conversion receiver fulfils the requirement of ZigBee i.e., low cost and low power consumption.

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