Table 1: Apc Words For Different Input Values

Input, X	product values	Input, X	product values	address $x_3'x_2'x_1'x_0'$	APC words
00001	A	11111	31A	1 1 1 1	15A
00010	2A	11110	30A	1 1 1 0	14A
00011	3A	11101	29A	1 1 0 1	13A
00100	4A	11100	28A	1 1 0 0	12A
00101	5A	11011	27A	1 0 1 1	11A
00110	6A	11010	26A	1 0 1 0	10A
00111	7A	11001	25A	1 0 0 1	9A
01000	8A	11000	24A	1 0 0 0	8A
01001	9A	10111	23A	0 1 1 1	7A
01010	10A	10110	22A	0 1 1 0	6A
01011	11A	10101	21A	0 1 0 1	5A
01100	12A	10100	20A	0 1 0 0	4A
01101	13A	10011	19A	0 0 1 1	3A
01110	14A	10010	18A	0 0 1 0	2A
01111	15A	10001	17A	0 0 0 1	A
10000	16A	10000	16A	0 0 0 0	0

B. Modified OMS for LUT Optimization

Then the multiplication of size L,of any binary word X, with a fixed coefficient A, instead of storing all the 2L possible values of $C = A \cdot X$, the odd multiples of A may be stored in the LUT only (2L/2) words,while the left-shift operations of one of those odd multiples [8],by all the even multiplies of A could be derived.

Table 2: Oms-Based Design Of The Lut Of Apc Words

Input, X	Product values	Input ,X	Product values	Address $x_3'x_2'x_1'x_0'$	APC words
00001	A	11111	31A	1111	15A
00010	2A	11110	30A	1110	14A
00011	3A	11101	29A	1101	13A
00100	4A	11101	28A	1100	12A
00101	5A	11100	27A	1011	11A
00110	6A	11011	26A	1010	10A
00111	7A	11010	25A	1001	9A
01000	8A	11001	24A	1000	8A
01001	9A	11000	23A	0111	7A
01010	10A	10111	22A	0110	6A
01011	11A	10110	21A	0101	5A
01100	12A	10101	20A	0100	4A
01101	13A	10100	19A	0011	3A
01110	14A	10010	18A	0010	2A
01111	15A	10001	17A	0001	A
10000	16A	10000	16A	0000	0

In Table II, we have shown that, at eight memory locations, the eight odd multiples, $A \times (2i + 1)$ are stored as Pi, for i = 0, 1, 2, . . . , 7. The left-shift operations of A,then the even multiples 2A, 4A, and 8A are derived.Similarly, left shifting 3A then the, 6A and 12A are derived, while left shifting 5A and 7A, then the 10A and 14A are derived. A barrel shifter for producing a maximum of three left shifts could be used to derive all the even multiples of A. It may be seen from Tables II and III that the 5-bit input word X can be mapped into a 4-bit LUT address ($d3d2d1d0$), by a simple set of mapping relations $di = x``i+1$, for i = 0, 1, 2 and $d3 = x0$ ‘’ where $X’’= (x’’3x’’2x’’1x’’0)$ is generated by shifting-out all the leading zeros of $X\_$ by an arithmetic right shift followed by address mapping.

$$X'' = \begin{cases} Y_L, & \text{if } x_4 = 1 \\ Y_L', & \text{if } x_4 = 0 \end{cases}$$

where YL and Y_L are derived by circularly shifting-out all the leading zeros of XL and X_L, respectively.

Table 3: Reduced Apc-Oms Address

Input X' $x_3'x_2'x_1'x_0'$	Product value	# of shifts	Shifted input, X''	Stored APC word	Address $d_3d_2d_1d_0$
0001	A	0	0001	P0=A	0000
0010	2xA	1			
0100	4xA	2			
1000	8xA	3			
0011	3A	0	0011	P1=3A	0001
0110	2x3A	1			
1100	4x3A	2			
0101	5A	0	0101	P2=5A	0010
1010	2x5A	1			
0111	7A	0	0111	P3=7A	0011
1110	2x7A	1			
1001	9A	0	1001	P4=9A	0100
1011	11A	0	1011	P5=11A	0101
1101	13A	0	1101	P6=13A	0110
1111	15A	0	1111	P7=15A	0111

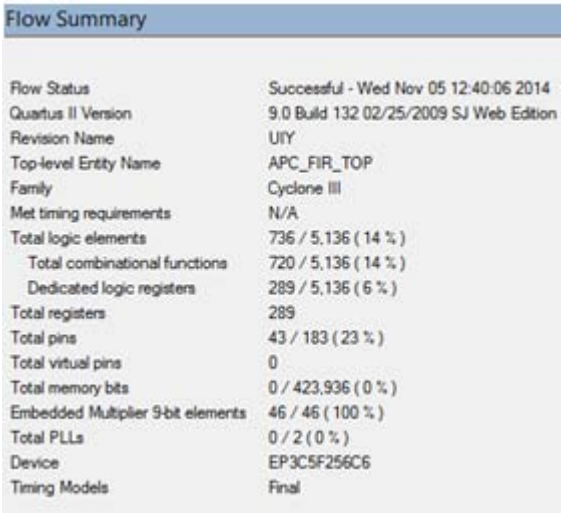

Figure 9: Area analyzer summary

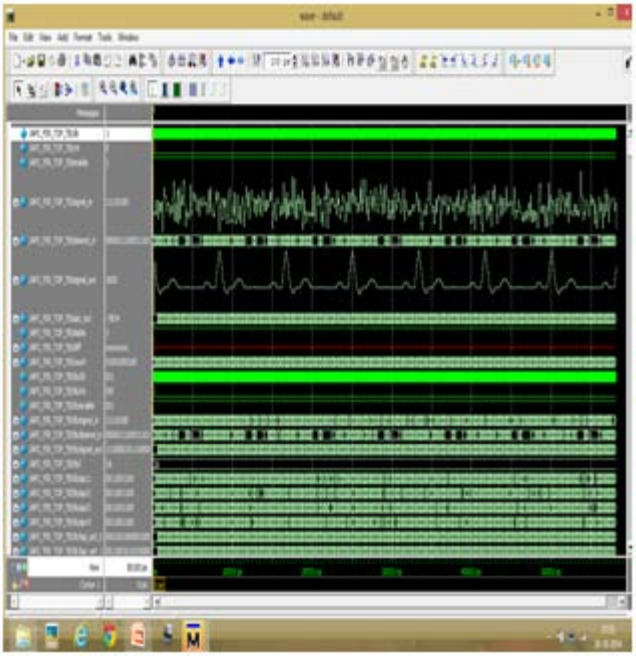

Figure 10: Snapshots of the output waveform

Then the above simulation output is the high accuracy of the input signal.

4. Simulation Results

Simulations have been performed using Modelsim 6.4a Simulation tool technology in. Fig.10 shows the input and output waveform results for proposed APC-OMS technique. Fig.9. shows the area analyzer summary. Proposed APC-OMS provide good accuracy of the input signal.The results of this proposed design reduced the LUT size into third-fourth of the conventional LUT size. By this we can clearly decide that the proposed circuit can have lower area overhead than the other conventional circuits. From the results, it is clear that the proposed circuit can have very less power.

5. Conclusion and Future Work

Analyzing the APC-OMS FIR architecture and performance, this paper presents a new architecture for the LUT.The proposed architecture applies the main concept of the basic APC-OMS technique in implementing the MAC unit and at the same time has many advantages over its basic architecture.The results obtained in the proposed architecture, the LUT size is reduced to Third-Fourth.The proposed architecture can be easily used to implement high order FIR filters e.g. 20-tap with different coefficients wordlength without suffering from large LUT construction and with low hardware complexity needed for the design.The future work is to perform a VLSI implementation of FIR filter for ultra wideband communications.

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