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Low Power Spectral Analysis for Built in Self Test by Using System on Chip

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Abstract: ***The Fast Fourier Transform Algorithm is used for Time to Frequency transform in the receiver side for spectral analysis in the communication. In the 4th Generation, the presence of multiple tones requires fine frequency tuning, which imposes the use of a large number of FFT points. FFT analysis is based on the coherent sampling, but it requires a significantly smaller number of points to make the FFT realization more suitable for on-chip built-in testing and calibration applications that require area and power efficiency. Due to large number of FFT points, more butterfly units are required that leads to large numbers of spectrum with testing complexity. Since all the processing elements are inside a single chip, there is a possible to get distortion. To get the accurate signal, we are using March C- algorithm with reconfigurable Pulse Width Controller is proposed makes way to reduce FFT points with address repetition aware process. Thus the accuracy has been maintained.***

Keywords: Fast Fourier Transform (FFT), coherent sampling, ADC, spectral testing.

1. Introduction

Accurate frequency estimation of distorted and noisy signals in industrial power systems is a challenging problem that has attracted much attention. The full understandings of the signal and system models are required for accurately estimating ADC spectral parameters once the output data has been collected. Most of the methods estimate parameters such as signal-to-noise, total harmonic distortion, spurious-free dynamic range (SFDR).

It is evaluated by means of the Fast Fourier transform (FFT) algorithm. Many of the estimation parameters are based on the coherent sampling. Coherent sampling is the best method for ADC testing. Calibration methods has been used that incorporate analog to digital convertor and digital signal processing [1] resources that to directly quantize the output signals of analog circuits for the computation of Fast Fourier transform (FFT) and dynamic tuning.

The calibration method could be applied to an individual analog block or a cascade of blocks. In practice, the maximum test signal frequency depends on the highest possible ADC sampling frequency [3] and clock frequency for the FFT computation. The presented method that the frequencies can be selected by the designer of built in test [4] to circumvent inaccuracies due to spectral leakage while using small number of FFT points.

The paper is organized as follows. Section II explores ADC for improving accuracy[2]. In section III is a Block diagram of proposed system. In section IV is a new algorithm March C- , Section V is the Calibration unit. Section VI shows the simulation results and finally some conclusions are given.

2. ADC for Improving Accuracy

Generally, ADC is used for converting a analog signal to digital means. Successive Approximation ADC is implemented in order to improve the accuracy.

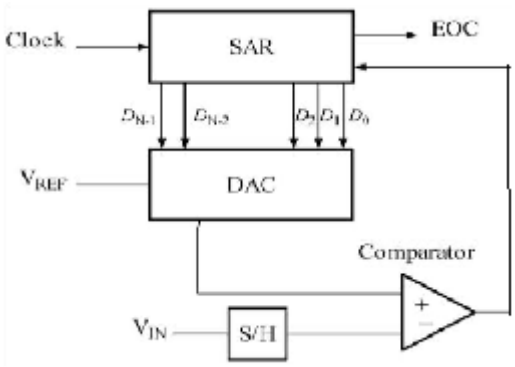

Figure 1: Block diagram of SAR ADC

Successive approximation employs a binary search algorithm in a feedback loop including a 1 bit A/D converter. The Following Figure 1: illustrates architecture which consists of a front end track & hold circuit, comparator, DAC and SAR logic. SAR logic is basically a shift register combined with decision logic and decision register. The pointer points to the last bit changed in the decision register and the data stored in this register is the result of all comparisons performed during conversion period. Throughout the counting process the register monitors the comparator output, o see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. If V IN > V DAC, the MSB of the register is maintained at 1 or else set to 0. After the DAC output has settled to its new value, the comparator is strobe once again and the above sequence is repeated.

3. Block Diagram

Fig. 2 shows the project block diagram which has various modules incorporated to get the accurate signal. The simplest frequency-domain tests use the direct application of the fast Fourier transform. Taking the FFT of the output data while driving the A/D converter with a single, low distortion sine wave, SFDR, and THD can easily be calculated. It is useful to take these measurements at several input amplitudes and frequencies, and plot the results.

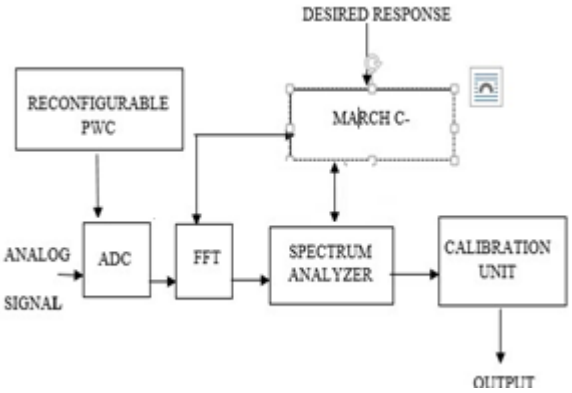

Figure 2: Overview of the Project

3.1 Basic FFT Algorithm

The basic FFT algorithm calculates the spectrum of the input waveform only for certain discrete frequencies known as FFT bins that are separated by the fundamental frequency (f) of the FFT. The f strictly depends on the sampling frequency (f_{samp}) and the length of the FFT (NFFT) as follows: $f \equiv f_{samp}$/NFFT. Thus, to avoid spectral leakage [5] and to accurately measure the frequency components of the input waveform, its frequencies have to be exact integer multiples of f. To achieve high frequency resolution, either the sampling frequency has to be decreased or the length of the FFT has to be increased [6].

The FFT involves separating the N points into smaller groups. We compute the first stage with groups of two coefficients, yielding N/2 blocks, each computing the addition and subtraction of the coefficients scaled by the corresponding twiddle factors. These results are used to compute the next state of N/4 blocks, which will then combine the results of two previous blocks (combining 4 coefficients at this point). This process repeats until we have one main block, with a final computation of all N coefficients.

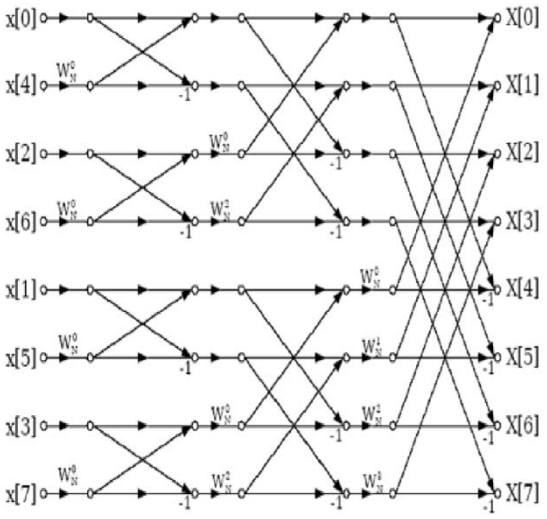

Figure 3: Illustration of FFT stages

In above Figure 3.8, we can see the different stages. In stage 1, there are 4 blocks, with one butterfly per block. In stage 2, there are two blocks with 2 butterflies each and finally in stage 3, there is only one block, combining all 8 coefficients with 4 butterflies.

Decimation in time FFT algorithm is used.
Number of stages = $\log_2 N$
Number of blocks/stage = $N/2^{stage}$
Number of butterflies/block = $2^{stage-1.}$

In the DIT approach, the initial DFT is divided into two transforms, one consisting of a transform of even samples and the other consisting of a transform of odd samples. This process is carried out until the initial transform is reduced to a set of two-point transforms of the initial data.

Fourier Transform (FFT) algorithms
$X(K) = \sum X(N)WN\hat{}nk$; $0 \leq K \leq N-1$ ----- [1]
where
x[n] = x[0], x[1], …, x[N-1]. Lets divide the sequence x[n] into even and odd sequences:
x[2n] = x[0], x[2], …, x[N-2]; x[2n+1] = x[1], x[3], …, x[N-1].

4. March C- Algorithm

The algorithms in most common use are the MARCH tests. March tests have the advantage of short test time but good fault coverage. A March C- based test algorithm [7]is specified by an address order and a number of reads and writes.

A March Test consists of a sequence of March elements, while a March element is a sequence of operations applied to every cell in the memory array before proceeding to the next cell. An operation can consist of writing a 0 into a cell (w0), writing a 1 into a cell (w1), reading an expected 0 from a cell (r0), and reading an expected 1 from a cell (r1). After all operations of a March element have been applied to a given cell, they are applied to the next cell. The address of the next

cell is determined by the address order, which can be either increasing or decreasing address.

The March C- Algorithm is used for detecting the various faults. They are;

1. Stuck-at fault (SAF): The logic value of a memory cell is always stuck-at 1 (SA1) or 0 (SA0).
2. Transition fault (TF): A cell fails to undergo a transition 1 or a transition 0.
3. Address Decoder Fault (ADF): Any fault that affects address decoder. Coupling fault (CF): In this case, a write operation in one cell can influence the value of another cell, and cell is called the coupling cell whereas cell is called the coupled cell.
4. Stuck Open Faults (SOF): A stuck open fault (SOF) means that a cell cannot be accessed, perhaps because of an open word line.
5. Transition Faults (TF): A cell or a line that fails to undergo a 0- 1 or 1-0 transition.

5. Calibration Unit

It will adjust the distorted frequency by fine frequency tuning [8]. The device with the correct measurements is taken as standard, with respect to that the device under test is calibrated.

6. Simulation Results

Simulation has been performed by using the Modelsim6.4a and Quartus II 9.0 for analytical purpose of area, RTL view, delay, etc., The Figure 4 shows the final output waveform in which transmitting a noisy input that is compared with the standard reference signal in order to get accurate signal. The signals are converted from Analog to Digital value, so that low cost in chip implementation, accuracy of signal can be maintained.

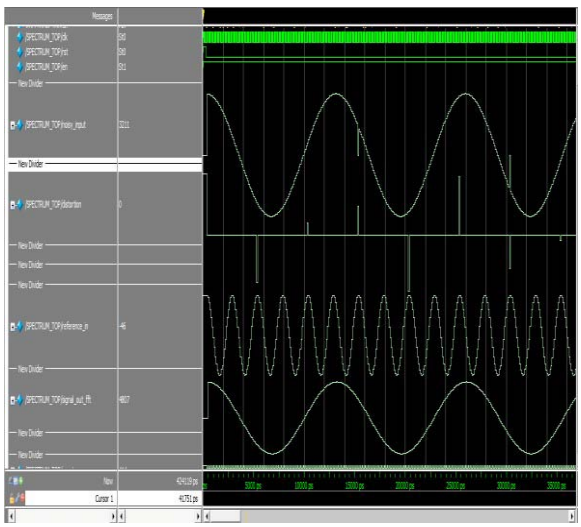

Figure 4: Final output snapshot

Figure 5 shows the Compilation report, which shows the total logical elements that is Area. In our project the occupied Area is 9%.

Maximum frequency = 98.34 MHz
Delay: T = 1/F =0.0101688 ns.
SNR = 35.053db.

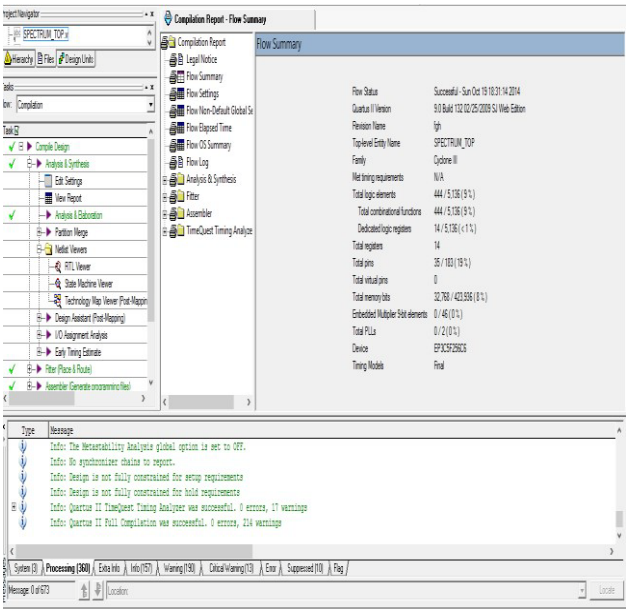

Figure 5: Compilation Report

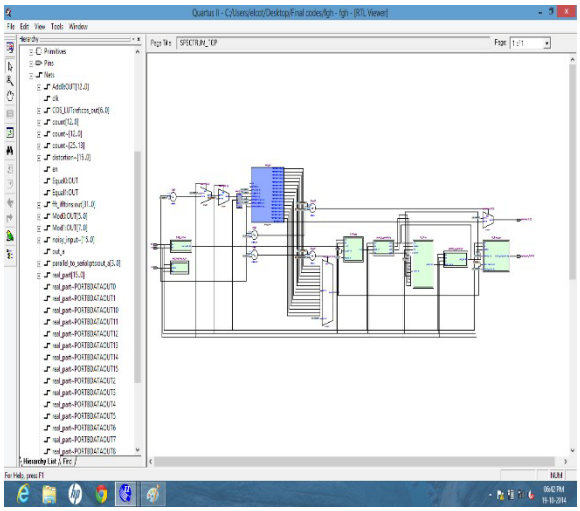

Figure 6: RTL View

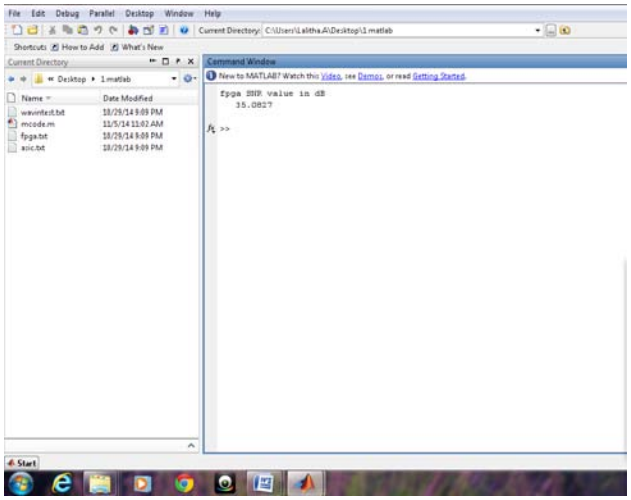

Figure 7: SNR Output

7. Conclusion

Accurate frequency estimation is of great importance in industrial power systems. In this paper, the analytical expression of accuracy of frequency estimated by the non even item interpolation FFT based on built in self testing has been presented with March C algorithm. The interpolation polynomial of the frequency estimation is introduced in the case 64 -point FFT is adopted. From the analytical expression of accuracy of frequency estimation, the variances of frequency estimation are determined by choosing suitable values of length of FFT, sampling frequency, and ADC resolution using SAR. The accuracy of the derived expressions is verified by means of Modelsim simulations and experimental results, where the simulation and theoretic results show very good agreements with noise level changing and frequency variation.

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