The error in the estimated delay using our model is within the acceptable range (< 10%)[19].

3. Comparative Analysis

Table 2: Comparative Analysis

Author	*Year*	*Methodology*	*Advantages*	*Disadvantages*	*Results*
Romi M S et al	2014	Considers the series stack effect along with the internal node voltage and parasitic capacitance while treating the Inverter-Transmission Gate structure as a single entity	1. A novel delay model that consider the Inverter-Transmission Gate structure as a single entity.	Increasingly large variations in PVT in DST cause uncertainty in IC design.	1. The error in the estimated delay using our model is within the acceptable range (<10%).
Marranghello F et al	2014	An accurate analytical delay model for CMOS inverter considering both sub-threshold and super-threshold operating regions.	1. The model can be applied to variability analysis. 2. The overall average error is circa 2.3% and the worst case error is approximately 6.6%. 3. The proposed model does not lose accuracy as V_{dd} is reduced.	The proposed inverter delay model calculates each component individually.	The proposed model is continuous and coherent for different inverter characteristics and conditions.
Marranghello F et al	2013	This paper presents a novel approach for delay modelling of CMOS complex gates, containing series and parallel transistor arrangements. The model uses a charge based approach instead of evaluating voltages as function of time.	1. Model accuracy has been improved. 2. The delay model considers explicitly the most relevant physical effects, without requiring additional fitting parameters. 3. The average error is circa 3%, with the worst case around 11%.	The used transistor model is only valid for strong inversion.	A novel analytical delay model for static CMOS complex gates is proposed for standard cell library characterization.
Mazumdar S et al	2012	The analysis is based on the modelling of RLC load, developed for submicron devices.	1. The maximum error has been found to be 9.4%. 2. The system of differential equations describe the accurate behaviour of the circuit. 3. Minimum error is as low as 2.3%.		A model to describe the output response of a CMOS inverter driving RLC load is proposed. In different regions of operation, the output response has been derived in time domain and for different values of circuit parameters the delay values have been compared.
Huang Z et al	2010	In this paper, the overshooting effect is modelled for CMOS inverter delay analysis in nanometer technologies.	1. The accuracy of switch-models can be enhanced with the assistance use of the transistor-level parameters. 2. The delay time can be reduced greatly by using large inverter sizes.	The calculation time will increase because of numerical procedures.	An analytical model is presented to calculate the CMOS inverter delay time based on the proposed overshooting effect model, which is verified to be in good agreement with SPICE results.
Wang Y et al	2009	By using a non-saturation current model, the analytical input-output transfer responses and propagation delay model are derived.	1. The discrepancy between the proposed model and simulation results is negligible, with average error of about 1%. 2. This analytical model, with different C_L, can be applied to more complex digital circuits. 3. Lower V_{dd} has the advantages of lowering power dissipation and reducing high electric field effects.	1. CMOS intrinsic delay increases rapidly with decreasing V_{dd}.	Delays are in good agreement with those of transistor level simulation results from SPICE, with accuracy of 3% or better.
Rossello J L et al	2004	The model is based on the nth-power-law MOSFET model and	1. A high degree of accuracy. 2. The model is an accurate tool to		An accurate analytical expression for the propagation delay of sub-

		computes the delay from the charge delivered to the gate.	compute the propagation delay and the input rise/fall time. 3.It provides an analytical relationship of the delay to design parameters, input transition time, supply voltage, and temperature.		micrometer CMOS inverters.
Taherzadeh-S M et al	2003	The model was based on the modified version of n^{th} power law MOSFET model.	1. Very good accuracy. 2. The effect of Miller and Parasitic capacitances is considered. 3. Appropriate for short-channel devices.	A two iteration approach is used in this paper.	A new and accurate model for determining delay and power consumption of static CMOS inverters are introduced in this paper.
Bisdounis L et al	1998	The α-power law MOS model, which considers the carriers' velocity saturation effects of short-channel devices, is used.	1. The presented timing model can be used for more complex static gates. 2. The propagation delay of a gate can be computed quickly and accurately using the inverter timing model. 3. The complications associated with trying to generalize the inverter-based model to complex gates are avoided.	Due to the reduction of the discharge current, there is an increase of the propagation delay.	Accurate analytical formulas for the evaluation of the propagation delay for all the cases of input ramps are produced.
Dutta S et al	1995	The paper presents a method to accurately calculate the delay and the output transition-time of a CMOS inverter for any input ramp and output loading is considered.	1. The proposed method is applicable to two extreme cases: infinitely fast and infinitely slow inputs. 2. The delay equations also explain negative delays that arise in case of slow input rise-times.	1. There exists a possibility for the calculation to yield a negative delay value. 2. The scaled delay is sensitive to input transition time.	Delay and transition time values obtained from the program have been found to be typically within 3% of SPICE.
A Nabavi-Lishi et al	1994	The reduction of transistor-level models of CMOS logic gates to equivalent inverters, for the purpose of computing the supply current in digital circuit is presented.	1. Since the inverter model also yields the delay at no extra cost, the timing of the current waveforms can be done automatically, without recourse to a timing simulator. 2. Although CMOS static logic gates are considered, the method is applicable to dynamic logic gates as well. 3. The entire process is being automated in a single package for current and power analysis.	Glitches can contribute as much as 15% of the total current and hence input vectors are encountered where the error is larger.	1.A method for reducing CMOS static gates to equivalent inverters has been introduced 2. The corresponding accuracy is around 12%.
Chow H C et al	1992	An analytical delay model for a CMOS inverter is introduced for the first time which includes channel-length modulation, source-drain resistance and high-field effects.	1.The proposed model is capable of handling both the source-drain resistance and the channel-length modulation effect explicitly. 2. Accuracy is quite good.	A source and drain resistor associated account for the source-drain resistance effect.	The analytical delay model for applications of time-delay optimisations of sub-micrometre MOSFET circuits.
Wu C et al	1990	Physical delay models entirely based upon device equations for small-geometry CMOS inverters with RC tree interconnection networks are presented.	1. The model has a wide applicable range of circuit and device parameters. 2. Adding a small number of drivers/repeaters with large sizes is more efficient in reducing the interconnection delay. 3. The technique of optimal-size repeaters with cascaded input drivers can lead to the lowest delay. 4. This delay model can be generalised to other CMOS logic gates. 5. The developed program can determine the number and the sizes of	1. Cascaded input drivers are less efficient in reducing the interconnection delay when $R_{lni}C_{lni}$ is large. 2. To drive RCloads rather than pure capacitive loads, however, a larger tapering factor has to be used.	1. The maximum relative error of the delay model is only 15%. 2. A tapering factor of 4-8 in cascaded input drivers can obtain a lower delay. 5. The maximum relative error in delay-time calculations is within 15%.

			drivers/repeaters more accurately		
Shiau M et al	1990	Large-signal equivalent circuits of CMOS inverters and RC ladder networks for interconnection lines are considered together with non-stop input waveforms and initial delay times.	1. The output fall (rise) time is a function of input rise (fall) time. 2. It can be applied to non-characteristic input waveform such as a step voltage or a waveform two times smaller in rise/fall time than characteristic waveform. 3. More practical and versatile.	The load capacitances and the device capacitances are all voltage dependent, it has to be linearized.	The relative delay times are still below 16 percent.
Andre J et al	1989	Based on the equivalent inverter concept. Rules for the characterization of equivalent inverters for CMOS complex gates and large combinational blocks like PLAs are derived.	1. It evaluates the propagation times in terms of the technology parameters and of the layout geometrics. 2. Very suitable to be used with a layout to circuit extraction. 3. Easily amenable to automation.	The rules can also be applied to NMOS digital IC but only to the n-enhancement transistors network.	An analytical model for evaluation of delay times in MOS digital circuits.
Jun Y et al	1989	The rise or fall delay time is approximated by a product of polynomials of the input waveform slope, the output loading capacitance, and the device configuration ratio.	1. This approach can be extended to the calculation of CMOS and NMOS transmission gate delay times. 2. The proposed delay model has only 5% errors. 3. It can readily be applied to the case of feedback loops using an iterative technique.	Accurate calculation of rise/fall delay times is atmost important.	This proposed delay model is having an error of less than 5% when compared to other circuits having errors greater than 10%.
Sakurai T	1988	α-power law MOS model including carrier velocity saturation effect which becomes eminent in short-channel MOSFETs.	1. As MOSFETs get miniaturized, the CMOS inverter delay becomes less sensitive to the input waveform slope and to the V_{dd} variation. 2. The result is not dependent on the triode model.	The short-circuit dissipation component increases as MOSFET becomes smaller.	As α becomes small, the transition voltage becomes more sensitive to the gate width ratio of PMOS and NMOS.
Chung-Yu Wu and Ming ChuenShiau	1988	A new model approach calculating the rise, fall and delay times for short-channel CMOS inverters with interconnection lines.	1. The developed model is analytical and suitable for automatic design and optimization. 2. Accuracy is quite acceptable.	The input excitations to the interconnection lines are of non-step waveforms.	The developed model has a maximum error of 16% for the delay times under various conditions.
DeschachtD et al	1988	Timing models are developed based on data-path decomposition in unidirectional elementary cells.	1. Simplicity and homogenity of the formulation. 2. Accuracy. 3. Fast and accurate timing analysis.	For shorter channels, the accuracy of the models does not permit fruitful comparisons.	The real response of any unidirectional macro can be expressed with good accuracy.
Chang L et al	1987	Concept of temperature degradation coefficient of drain current is used in deriving a simplified model to predict the linear temperature coefficient of the delay time of a CMOS inverter.	1. The temperature degradation coefficient is highly bias dependent. 2. The effective temperature degradation coefficient for linear region is larger than saturation region.	Quantitative analysis has been difficult because the theoretical mobility function is not simple enough to facilitate a first-order solution	1. The total delay time coefficient k=3.52, 3.40 & 3.05 for Vcc=3,5 & 7V resp. 2. The avg. error is 3.3% as compared to the measured k.

Table 2shows the comparative analysis for the delay models for the CMOS Inverter-Transmission gate structure in CMOS circuit designs. Based on the comparative analysis done, it is found that in earlier base, the CMOS inverter-Transmission gate structure is considered individually and then analysed.

Considering the CMOS Inverter-Transmission gate structure as a single entity is a better option. The most recent paper treated the Inverter-Transmission Gate as a single structure considering the series stack effect along with the internal node voltage and parasitic capacitance. This model is used to estimate delay for varying input transition time while keeping the size of the Inverter Transmission Gate structure and load capacitance.

4. Conclusion

In this survey paper, a literature review on delay models for CMOS inverter-Transmission gate structure had been presented. A review on the developments that occurred in designing an analytical delay model from considering the

structure individually to treating it as a single entity had done. The most recent paper on this considered the series stack effect along with the internal node voltage and parasitic capacitance while treating the Inverter-Transmission Gate structure as a single entity. It was observed that the error in the estimated delay using this model is within the acceptable range (<10%). This methodology can be integrated with other gate delay models to estimate the impact of PVT variations.

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