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A Survey on Analytical Delay Models for CMOS Inverter-Transmission Gate Structure

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Abstract: ***In this survey paper, a literature study on analytical delay models for a CMOS inverter and transmission gate has been done. Inverter followed by Transmission gate structure appears in many CMOS circuit design. Initially, the delay calculation of this entity is done considering them individually, which is not good. In this case, it does not account for the series stack effect that appears while driving a load through Inverter-Transmission Gate structures. But later on, advancements in this field of research resulted in considering the above said Inverter-Transmission Gate structure as a single entity in calculating the delay parameters or designing the delay model. This paper presents a review on the developments that occurred in designing an analytical delay model from considering the structure individually to treating it as a single entity. The recently proposed model considers the series stack effect along with the internal node voltage and parasitic capacitance, it also proposes a methodology to incorporate the effect of process-voltage-temperature variations and compared against SPICE simulation using 32nm Predictive Technology Modelling (PTM).***

Keywords: CMOS Inverter, Transmission Gate, Delay Model, Leakage Current, Process-Voltage-Temperature Variations, Series Stack Effect.

1. Introduction

Improvements in integrated circuits have enabled space exploration, made automobiles safer and more fuel efficient, revolutionized the nature of warfare, brought much of mankind's knowledge to our Web browsers, and made the world a flatter place. No other technology in history has sustained such a high growth rate lasting for so long. The Metal-Oxide-Semiconductor (MOS) transistor was introduced in terms of its operation as an ideal switch. With the recent development in the VLSI technology, billions of transistors are packed into a single chip.

Intuitively, when an input changes, the output will retain its old value for at least the contamination delay and take on its new value in at most the propagation delay. Rise/fall times are also sometimes called slopes or edge rates. Propagation and contamination delay times are also called max-time and min-time, respectively. The gate that charges or discharges a node is called the driver and the gates and wire being driven is called the load. Propagation delay is usually the most relevant value of interest, and is often simply called delay. Fig. 1 shows the propagation delay and rise/fall time. ***Propagation delay time,*** t_{pd}= maximum time from the input crossing 50% to the output crossing 50%.

- ***Contamination delay time,*** t_{cd}= minimum time from the input crossing 50% to the output crossing 50%.
- ***Rise time,*** t_r= time for a waveform to rise from 20% to80% of its steady-state value.
- ***Fall time,*** t_f= time for a waveform to fall from 80% to20% of its steady-state value.
- ***Edge rate,*** t_{rf}= $(t_r + t_f)/2$

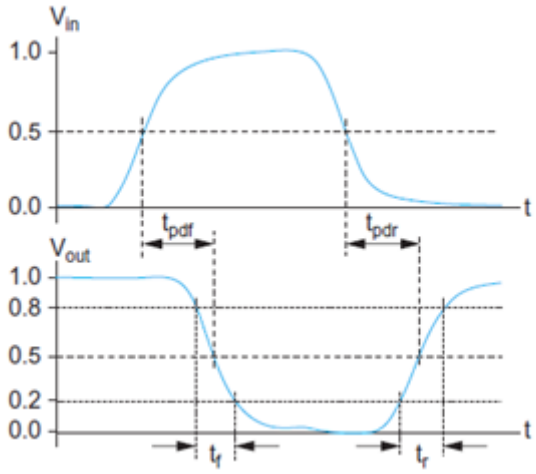

Figure 1: Propagation delay and rise/fall time

The most fundamental way to compute delay is to develop a physical model of the circuit of interest, write a differential equation describing the output voltage as a function of input voltage and time, and solve the equation. The solution of the differential equation is called the transient response, and the delay is the time when the output reaches V_{DD} /2.The differential equation is based on charging or discharging of the capacitances in the circuit. The circuit takes time to switch because the capacitance cannot change its voltage instantaneously. If capacitance Cis charged with a current I, the voltage V, on the capacitor varies as:

$$I = C \frac{dV}{dT} \quad (1)$$

1.1. Variability: Process-Voltage Temperature Variations:

So far, when considering the various aspects of determining a circuit's behaviour, it has only alluded to the variations that might occur in this behaviour given different operating conditions. In general, there are three different sources of variation—two environmental and one manufacturing:

- Process variation
- Supply voltage
- Operating temperature

The variation sources are also known as Process, Voltage, and Temperature (PVT). The aim must be to design a circuit that will operate reliably operate over all extremes of these three variables. Failure to do so causes circuit problems, poor yield, and customer dissatisfaction. Variations are usually modelled with uniform or normal (Gaussian) statistical distributions. Uniform distributions are specified with a half-range a. For good results, accept variations over the entire half-range. Normal distributions are specified with a standard deviation σ. Processing variations are usually modelled with normal distributions.

- **Supply Voltage**

Systems are designed to operate at a nominal supply voltage, but this voltage may vary for many reasons including tolerances of the voltage regulator, IR drops along supply rails, and di/dt noise.

- **Temperature**

As temperature increases, drain current decreases. The junction temperature of a transistor is the sum of the ambient temperature and the temperature rise caused by power dissipation in the package. This rise is determined by the power consumption and the package thermal resistance. Table 1 lists the ambient temperature ranges for parts specified to commercial, industrial, and military standards.

- **Process Variation**

Devices and interconnect have variations in film thickness, lateral dimensions, and doping concentrations. For devices, the most important variations are channel length Land threshold voltage V_t. Channel length variations are caused by photolithography proximity effects, deviations in the optics, and plasma etch dependencies. Threshold voltages vary because of different doping concentrations and annealing effects, mobile charge in the gate oxide, and discrete dopant variations caused by the small number of dopant atoms in tiny transistors.

Table 1: Ambient Temperature Ranges

Standard	Minimum	Maximum
Commercial	0 °C	70 °C
Industrial	−40 °C	85 °C
Military	−55 °C	125 °C

For interconnect, the most important variations are line width and spacing, metal and dielectric thickness, and contact resistance. Line width and spacing, like channel length, depend on photolithography and etching proximity effects. Thickness may be influenced by polishing. Contact resistance depends on contact dimensions and the etch and clean steps.

The following Fig. 4 shows the PVT operating conditions:

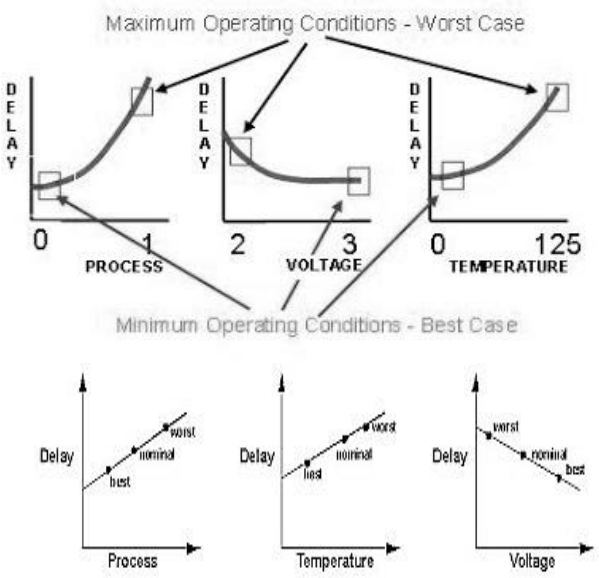

Figure 2: PVT Operating Conditions

1.2. Stack Effect

Sub-threshold current depends exponentially on V_T, V_{DS} and V_{GS}. Therefore it is a function of the terminal voltages, V_D, V_B, V_S and V_G. This means that to know sub-threshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the sub-threshold leakage can be controlled. Input pattern of each gate affects the sub-threshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern.

Source biasing is the general term for several techniques that change the voltage at the source of a transistor. The goal is to reduce V_{GS}, which has the effect of exponentially reducing the sub-threshold current. Another result of raising the source is that it also reduces V_{BS}, resulting in a slightly higher threshold voltage due to the body effect.

1.3. Predictive Technology Modelling

Predictive Technology Model (PTM) for nanoscale CMOS was first developed in 2000.It was widely used in early stage design exploration, providing key insights into advanced process and design research. PTM for high performance design was further improved to achieve a more physical prediction by identifying the scaling trend of primary parameters and incorporating important correlations among them.

In this survey paper, a literature study on analytical delay models for a CMOS inverter and transmission gate has been presented. Inverter followed by Transmission gate structure appears in many CMOS circuit design. Initially, the delay calculation of this entity is done considering them individually, which is not good which does not account for the series stack effect that appears while driving a load through Inverter-Transmission Gate structures. But later on, advancements in this field of research resulted in considering the above said Inverter-Transmission Gate structure as a

single entity in calculating the delay parameters or designing the delay model. This paper presents a review on the developments that occurred in designing an analytical delay model from considering the structure individually to treating it as a single entity. The recently proposed model considers the series stack effect along with the internal node voltage and parasitic capacitance.

The rest of the paper is organized as follows: Section 2 presents the literature review on the developments and advancements in delay modelling of inverter-transmission gate structure over the years. A comparative analysis of different delay models is presented in section 3. Finally, section 4 summarizes the main contributions of the work.

2. Literature Survey

Chang L et al(1987) proposed the concept of the temperature degradation coefficient of the drain current is used in deriving a simplified model to predict the linear temperature coefficient of the delay time of a CMOS inverter[1].

In 1988, Deschacht D et al developed an explicit formulation of the transient response of general combinational CMOS structures, including load conditions and driving waveforms. Results are shown in excellent agreement with less than 10-percent discrepancy [2].

Wu C et al (1988) presented a new modelling approach to calculate the rise, fall, and delay times for short-channel CMOS inverters with interconnection lines. The same approach can be applied to the characterization of complex interconnection nets and other type of short-channel CMOS logic gates [3].

Sakurai T et al (1988) developed an α-power law MOS model including carrier velocity saturation effect which becomes eminent in short-channel MOSFETs. As α becomes small, the transition voltage becomes more sensitive to the gate width ratio of PMOS and NMOS [4].

In 1989, Jun Y et al proposed a new delay model for multiple delay simulation for NMOS and CMOS logic circuits. This approach can easily be extended to the case of multiple-input transitions [5].

Andre J et al (1989) provided an analytical model for the evaluation of propagation times in MOS digital networks is proposed. The model is based in the equivalent inverter concept [6].

Shiau M et al (1990) developed a new physical timing model for small-geometry CMOS inverter with interconnection lines has been developed. Reasonable accuracy, wide applicable range, and high computation efficiency make the developed timing models quite attractive in MOS VLSI timing verification and auto-sizing [7].

Wu C et al (1990) presented Physical delay models entirely based upon device equations for small-geometry CMOS inverters with RC tree interconnection networks. Through extensive comparisons with SPICE simulation results, it is shown that the maximum relative error in delay-time calculations using the developed model is within 15% for 1.5-pm CMOS inverters with RCtree interconnection networks [8].

Chow H C et al (1992) proposed an analytical delay model of a CMOS inverter which includes channel-length modulation and source-drain resistance as well as high-field effects. Calculations of the rise, fall, and delay times show good agreement with SPICE MOS level 3 simulations[9].

In 1994, author Nabavi-Lishi et al developed a method for reducing CMOS static gates to equivalent inverters has been introduced. The technique presented in this paper can be easily applied to dynamic logic gates as well[10].

Dutta S et al (1995) derived a scheme to accurately evaluate the delay and the output transition-time of an inverter. Results obtained from a program implementation have been found to be typically within 3% of SPICE[11].

Bisdounis L et al (1998) introduced an accurate, analytical model for the evaluation of the CMOS inverter transient response and propagation delay for short-channel devices. The final results are in excellent agreement with SPICE simulations[12]. In 2003, Taherzadeh S M et al presented a model that was based on the modified version of n^{th} power law MOSFET model. Rossello J et al (2004) developed accurate analytical expression for the propagation delay of sub-micrometer CMOS inverters that takes into account the short-circuit current, the input–output coupling capacitance, and the carrier velocity saturation effects[13].

Wang Y et al (2009) proposed a new analytical propagation delay model for nano-scale CMOS inverters. Delays predicted by the proposed model has an accuracy of 3% or better[14].

In 2010,Huang Z et al developed the overshooting effect is modelled for CMOS inverter delay analysis in nanometer technologies. The proposed model is used to improve the accuracy of the switch-resistor model for approximating the inverter output waveform[15].

Mazumdar S et al (2012) analysed the behaviour of CMOS inverter driving RLC interconnect load. The maximum error has been found to be 9.4%[16]. Marranghello F S et al (2013) proposed a novel approach for delay modelling of CMOS complex gates, containing series and parallel transistor arrangements. The average error is 3%, with the worst case around 11%[17].

Marranghello F S et al (2014) developed an accurate analytical delay model for CMOS inverter considering both sub-threshold and super-threshold operating regions. This delay model gives an average error of 2.3% and the worst case error of 6.6%.[18].

In 2014, Romi M S et al presented a novel approach for delay modelling of Inverter followed by Transmission Gate structure. The derived model is compared against the SPICE simulation results using 32nm Predictive Technology Model.

The error in the estimated delay using our model is within the acceptable range (< 10%)[19].

3. Comparative Analysis

Table 2: Comparative Analysis

Author	*Year*	*Methodology*	*Advantages*	*Disadvantages*	*Results*
Romi M S et al	2014	Considers the series stack effect along with the internal node voltage and parasitic capacitance while treating the Inverter-Transmission Gate structure as a single entity	1. A novel delay model that consider the Inverter-Transmission Gate structure as a single entity.	Increasingly large variations in PVT in DST cause uncertainty in IC design.	1. The error in the estimated delay using our model is within the acceptable range (<10%).
Marranghello F et al	2014	An accurate analytical delay model for CMOS inverter considering both sub-threshold and super-threshold operating regions.	1. The model can be applied to variability analysis. 2. The overall average error is circa 2.3% and the worst case error is approximately 6.6%. 3. The proposed model does not lose accuracy as V_{dd} is reduced.	The proposed inverter delay model calculates each component individually.	The proposed model is continuous and coherent for different inverter characteristics and conditions.
Marranghello F et al	2013	This paper presents a novel approach for delay modelling of CMOS complex gates, containing series and parallel transistor arrangements. The model uses a charge based approach instead of evaluating voltages as function of time.	1. Model accuracy has been improved. 2. The delay model considers explicitly the most relevant physical effects, without requiring additional fitting parameters. 3. The average error is circa 3%, with the worst case around 11%.	The used transistor model is only valid for strong inversion.	A novel analytical delay model for static CMOS complex gates is proposed for standard cell library characterization.
Mazumdar S et al	2012	The analysis is based on the modelling of RLC load, developed for submicron devices.	1. The maximum error has been found to be 9.4%. 2. The system of differential equations describe the accurate behaviour of the circuit. 3. Minimum error is as low as 2.3%.		A model to describe the output response of a CMOS inverter driving RLC load is proposed. In different regions of operation, the output response has been derived in time domain and for different values of circuit parameters the delay values have been compared.
Huang Z et al	2010	In this paper, the overshooting effect is modelled for CMOS inverter delay analysis in nanometer technologies.	1. The accuracy of switch-models can be enhanced with the assistance use of the transistor-level parameters. 2. The delay time can be reduced greatly by using large inverter sizes.	The calculation time will increase because of numerical procedures.	An analytical model is presented to calculate the CMOS inverter delay time based on the proposed overshooting effect model, which is verified to be in good agreement with SPICE results.
Wang Y et al	2009	By using a non-saturation current model, the analytical input-output transfer responses and propagation delay model are derived.	1. The discrepancy between the proposed model and simulation results is negligible, with average error of about 1%. 2. This analytical model, with different C_L, can be applied to more complex digital circuits. 3. Lower V_{dd} has the advantages of lowering power dissipation and reducing high electric field effects.	1. CMOS intrinsic delay increases rapidly with decreasing V_{dd}.	Delays are in good agreement with those of transistor level simulation results from SPICE, with accuracy of 3% or better.
Rossello J L et al	2004	The model is based on the nth-power-law MOSFET model and	1. A high degree of accuracy. 2. The model is an accurate tool to		An accurate analytical expression for the propagation delay of sub-

		computes the delay from the charge delivered to the gate.	compute the propagation delay and the input rise/fall time. 3.It provides an analytical relationship of the delay to design parameters, input transition time, supply voltage, and temperature.		micrometer CMOS inverters.
Taherzadeh-S M et al	2003	The model was based on the modified version of n^{th} power law MOSFET model.	1. Very good accuracy. 2. The effect of Miller and Parasitic capacitances is considered. 3. Appropriate for short-channel devices.	A two iteration approach is used in this paper.	A new and accurate model for determining delay and power consumption of static CMOS inverters are introduced in this paper.
Bisdounis L et al	1998	The α-power law MOS model, which considers the carriers' velocity saturation effects of short-channel devices, is used.	1. The presented timing model can be used for more complex static gates. 2. The propagation delay of a gate can be computed quickly and accurately using the inverter timing model. 3. The complications associated with trying to generalize the inverter-based model to complex gates are avoided.	Due to the reduction of the discharge current, there is an increase of the propagation delay.	Accurate analytical formulas for the evaluation of the propagation delay for all the cases of input ramps are produced.
Dutta S et al	1995	The paper presents a method to accurately calculate the delay and the output transition-time of a CMOS inverter for any input ramp and output loading is considered.	1. The proposed method is applicable to two extreme cases: infinitely fast and infinitely slow inputs. 2. The delay equations also explain negative delays that arise in case of slow input rise-times.	1. There exists a possibility for the calculation to yield a negative delay value. 2. The scaled delay is sensitive to input transition time.	Delay and transition time values obtained from the program have been found to be typically within 3% of SPICE.
A Nabavi-Lishi et al	1994	The reduction of transistor-level models of CMOS logic gates to equivalent inverters, for the purpose of computing the supply current in digital circuit is presented.	1. Since the inverter model also yields the delay at no extra cost, the timing of the current waveforms can be done automatically, without recourse to a timing simulator. 2. Although CMOS static logic gates are considered, the method is applicable to dynamic logic gates as well. 3. The entire process is being automated in a single package for current and power analysis.	Glitches can contribute as much as 15% of the total current and hence input vectors are encountered where the error is larger.	1.A method for reducing CMOS static gates to equivalent inverters has been introduced 2. The corresponding accuracy is around 12%.
Chow H C et al	1992	An analytical delay model for a CMOS inverter is introduced for the first time which includes channel-length modulation, source-drain resistance and high-field effects.	1.The proposed model is capable of handling both the source-drain resistance and the channel-length modulation effect explicitly. 2. Accuracy is quite good.	A source and drain resistor associated account for the source-drain resistance effect.	The analytical delay model for applications of time-delay optimisations of sub-micrometre MOSFET circuits.
Wu C et al	1990	Physical delay models entirely based upon device equations for small-geometry CMOS inverters with RC tree interconnection networks are presented.	1. The model has a wide applicable range of circuit and device parameters. 2. Adding a small number of drivers/repeaters with large sizes is more efficient in reducing the interconnection delay. 3. The technique of optimal-size repeaters with cascaded input drivers can lead to the lowest delay. 4. This delay model can be generalised to other CMOS logic gates. 5. The developed program can determine the number and the sizes of	1. Cascaded input drivers are less efficient in reducing the interconnection delay when $R_{lnf}C_{lni}$ is large. 2. To drive RCloads rather than pure capacitive loads, however, a larger tapering factor has to be used.	1. The maximum relative error of the delay model is only 15%. 2. A tapering factor of 4-8 in cascaded input drivers can obtain a lower delay. 5. The maximum relative error in delay-time calculations is within 15%.

			drivers/repeaters more accurately		
Shiau M et al	1990	Large-signal equivalent circuits of CMOS inverters and RC ladder networks for interconnection lines are considered together with non-stop input waveforms and initial delay times.	1. The output fall (rise) time is a function of input rise (fall) time. 2. It can be applied to non-characteristic input waveform such as a step voltage or a waveform two times smaller in rise/fall time than characteristic waveform. 3. More practical and versatile.	The load capacitances and the device capacitances are all voltage dependent, it has to be linearized.	The relative delay times are still below 16 percent.
Andre J et al	1989	Based on the equivalent inverter concept. Rules for the characterization of equivalent inverters for CMOS complex gates and large combinational blocks like PLAs are derived.	1. It evaluates the propagation times in terms of the technology parameters and of the layout geometrics. 2. Very suitable to be used with a layout to circuit extraction. 3. Easily amenable to automation.	The rules can also be applied to NMOS digital IC but only to the n-enhancement transistors network.	An analytical model for evaluation of delay times in MOS digital circuits.
Jun Y et al	1989	The rise or fall delay time is approximated by a product of polynomials of the input waveform slope, the output loading capacitance, and the device configuration ratio.	1. This approach can be extended to the calculation of CMOS and NMOS transmission gate delay times. 2. The proposed delay model has only 5% errors. 3. It can readily be applied to the case of feedback loops using an iterative technique.	Accurate calculation of rise/fall delay times is atmost important.	This proposed delay model is having an error of less than 5% when compared to other circuits having errors greater than 10%.
Sakurai T	1988	α-power law MOS model including carrier velocity saturation effect which becomes eminent in short-channel MOSFETs.	1. As MOSFETs get miniaturized, the CMOS inverter delay becomes less sensitive to the input waveform slope and to the V_{dd} variation. 2. The result is not dependent on the triode model.	The short-circuit dissipation component increases as MOSFET becomes smaller.	As α becomes small, the transition voltage becomes more sensitive to the gate width ratio of PMOS and NMOS.
Chung-Yu Wu and Ming ChuenShiau	1988	A new model approach calculating the rise, fall and delay times for short-channel CMOS inverters with interconnection lines.	1. The developed model is analytical and suitable for automatic design and optimization. 2. Accuracy is quite acceptable.	The input excitations to the interconnection lines are of non-step waveforms.	The developed model has a maximum error of 16% for the delay times under various conditions.
DeschachtD et al	1988	Timing models are developed based on data-path decomposition in unidirectional elementary cells.	1. Simplicity and homogenity of the formulation. 2. Accuracy. 3. Fast and accurate timing analysis.	For shorter channels, the accuracy of the models does not permit fruitful comparisons.	The real response of any unidirectional macro can be expressed with good accuracy.
Chang L et al	1987	Concept of temperature degradation coefficient of drain current is used in deriving a simplified model to predict the linear temperature coefficient of the delay time of a CMOS inverter.	1. The temperature degradation coefficient is highly bias dependent. 2. The effective temperature degradation coefficient for linear region is larger than saturation region.	Quantitative analysis has been difficult because the theoretical mobility function is not simple enough to facilitate a first-order solution	1. The total delay time coefficient k=3.52, 3.40 & 3.05 for Vcc=3,5 & 7V resp. 2. The avg. error is 3.3% as compared to the measured k.

Table 2shows the comparative analysis for the delay models for the CMOS Inverter-Transmission gate structure in CMOS circuit designs. Based on the comparative analysis done, it is found that in earlier base, the CMOS inverter-Transmission gate structure is considered individually and then analysed.

Considering the CMOS Inverter-Transmission gate structure as a single entity is a better option. The most recent paper treated the Inverter-Transmission Gate as a single structure considering the series stack effect along with the internal node voltage and parasitic capacitance. This model is used to estimate delay for varying input transition time while keeping the size of the Inverter Transmission Gate structure and load capacitance.

4. Conclusion

In this survey paper, a literature review on delay models for CMOS inverter-Transmission gate structure had been presented. A review on the developments that occurred in designing an analytical delay model from considering the

structure individually to treating it as a single entity had done. The most recent paper on this considered the series stack effect along with the internal node voltage and parasitic capacitance while treating the Inverter-Transmission Gate structure as a single entity. It was observed that the error in the estimated delay using this model is within the acceptable range (<10%). This methodology can be integrated with other gate delay models to estimate the impact of PVT variations.

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