

Design of GDI Based Low Power and High-Speed CMOS Full Adder Circuits

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Abstract: Power consumption and delay are two important considerations for VLSI systems. The objective of this project is to reduce the power and to reduce the delay which increases the speed. Adders are very important components in many applications such as microprocessor and digital signal processing (DSP) architectures. Full Adder is one of the core elements. It used in many of the complex arithmetic logic circuits like multiplication, division, addition. In this paper Full Adder has been generated by the Gate Diffusion Input (GDI) technique. The proposed full adder is simulated with Tanner EDA using 0.18 μ m CMOS Technology. By reducing the Transistor size, the power and delay are reduced. Simulation results show great improvement in terms of Power-Delay-Product (PDP).

Keywords: CMOS, GDI, XOR, XNOR, TANNER EDA

1. Introduction

Most of the very large scale integration applications, such as video and image processing, digital signal processing, microprocessors and Calculation operations. For example subtraction and multiplication are the most commonly used operations [6]. The 1-bit full adder cell is the basic building block of all these modules. Therefore, improvement performance is acute for enhancing the overall module efficiency. In a low-power VLSI system has been used in fast growing technologies like mobile communication and computation. The battery technology is similar for the microelectronics technology because the fine amount of power available for the VLSI systems.

Hence designers are handled VLSI systems with more constraints: low-power consumption, small silicon area, high throughput, and high speed [2] [3]. So construction of low-power and high-performance adder cells is of great interest. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits.

This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents are strongly influenced by the selected logic style. Depending on the application, the circuit to be implemented for performance aspects it become important with disallowing the formulation of universal rules for optimal logic styles [6]. Investigations of low-power logic styles and variety of full adders using static and dynamic logic styles have been reported in the literature so far, however, this technique is used in some arithmetic circuits the full adder performance would affect the system as a whole. One bit full adder cell is the extensively used in arithmetic circuits, thus enhancing the overall module performance and designers are working with fewer constraints such as low-power consumption, small silicon area, high throughput, and high speed.

The paper is organized as follows. Section 2 explores existing conventional CMOS design style [2]. In section 3 is a new style called GDI [1]. This section difference in CMOS logic circuits, and then based on the idea of GDI technique. In section 4 block diagram of the proposed system, Section 5 is the new 1-bit adder has been proposed. Section 6 shows the simulation results in a GDI based full adder and finally some conclusions are given.

2. Existing System

In this Existing adder we will use one XOR and one XNOR and a multiplexer to generate output sum and carry. The expressions for sum and carry are given in below.

$$\text{Sum} = H \text{ XOR } C = H \cdot C' + H' \cdot C$$
$$\text{Cout} = A \cdot H' + C \cdot H$$

Where H is (A XOR B) and H' is compliment of (A XOR B).

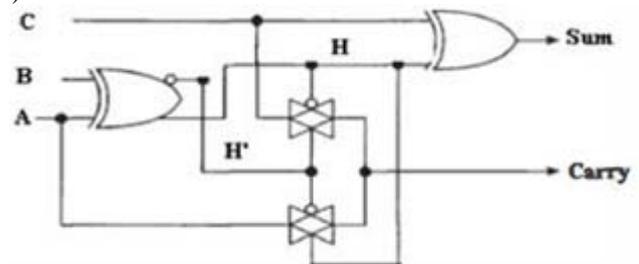


Figure 1: CMOS XOR/XNOR full adder

The existing adder cell has transistors and is mainly based up on XOR-XNOR pass transistor logic and transmission gates. In this existing adder the two transmission gates are used as multiplexer and the sum can be generated by XOR gates and output carry can be generated by XOR/ XNOR gates shown in the above figure 1, and output of XOR gate can be used as the selection line for multiplexer or as the control for the Transmission gate which will get output as the carry [2].

3. The GDI Technique

Gate-Diffusion-Input (GDI) method is based on cell as shown in figure 2. It reminds the basic cell of CMOS inverter but it contains some important changes [1]:

- 1) GDI cell contains three inputs – G (common gate input of PMOS and NMOS), P (input to the PMOS), and N (input to the NMOS).
- 2) Both N and P are connected to bulk of NMOS and PMOS respectively; hence the cell was contrast with CMOS inverter. All the functions are not possible in P-well CMOS process, it can be successfully implemented in Twin-Well CMOS or SOI technologies.

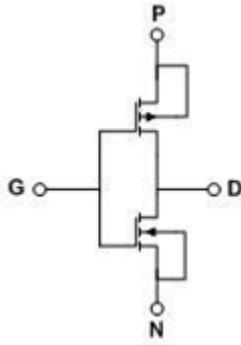


Figure 2: Basic GDI cell

The basic GDI cell is shown in figure 2 and truth table is shown Table1. It should be noted that the source of the PMOS in a GDI cell is not connected to VDD while the source of the NMOS in a GDI cell is not connected to GND [1]. This feature gives the GDI cell two extra input pins to use which makes the GDI design more flexible than a usual CMOS design.

Table 1: Logic Function of Basic GDI Cell

N	P	G	D
0	B	A	A'B
B	1	A	A'+B
1	B	A	A+B
B	0	A	AB
C	B	A	A'B+AC
0	1	A	A'

4. Proposed System

The block diagram of the proposed full adder cell and its structure are shown in Figure 3. In addition, several circuits have been proposed for each module

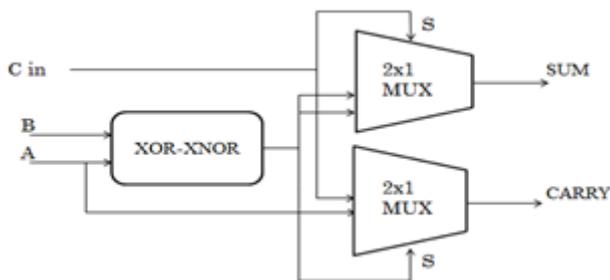


Figure 3: Block diagram of proposed system

The XOR and XNOR gates are play the major role in circuits used for performing arithmetic operations like comparators, compressors, full adders, and so on. Optimized design for XOR and XNOR gates are required for performance of larger circuits. In deep submicron technology, the enhanced design is to small output voltage, less power, less delay, and be noise resistant even with low voltage. Another feature for the Full Adder cell is to have a lesser number of transistors and the concurrent generation of the two non-skewed outputs.

Recently, a structural approach towards the low-power adder cell design has been adopted where the adder cell is partitioned into two stages. The first stage is to generate the intermediate logic functions of XOR and XNOR. This stage is usually implemented in pass transistor logic to reduce the transistor count. These complementary outputs will be fed to the input of the second stage.

In second stage the Sum and Carry outputs are generated [8]. Since adder cells are normally cascaded to form a usual arithmetic circuit, their drivability must be ensured. In short, the driving cell must provide almost full swing outputs. Otherwise, the performance of the circuit will be degraded dramatically or become non operative at low supply voltage.

5. Proposed GDI Based Full Adder

The full adder cell performance has been enhanced by optimizing the adder circuits. In adder equations, the XOR and XNOR functions are the significant variables. Hence XOR and XNOR functions are generated by full adder based GDI technique. In fig. 4, it uses eight transistors to generate the balanced XOR and XNOR functions [9].

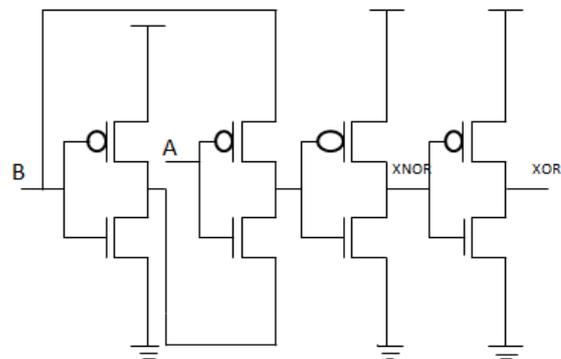


Figure 4: XOR/XNOR cell with the GDI technique

A one-bit binary full adder taking three one-bit inputs: A, B and C and generate sum and carry equation 1 and 2.

$$SUM = C(A \oplus B) + C(A \oplus B) \quad (1)$$

$$CARRY = C(A \oplus B) + A(A \oplus B) \quad (2)$$

The full adder cell based on GDI technique is to design a low power and high performance when comparing to the existence system [8].

The 12 transistors full adder cell has that are shown in figure.5. In the first stage of this cell, XOR and XNOR

functions are generating through GDI technique. This stage shows full swing with low voltage. These outputs will be fed to the input of the second stage and Sum and Carry outputs are generated. Since adder cells are generally cascaded to form a usual arithmetic circuit and their capabilities must be ensured. Output voltage levels are improved with addition of one 0.1pf capacitor added in sum and carry stage.

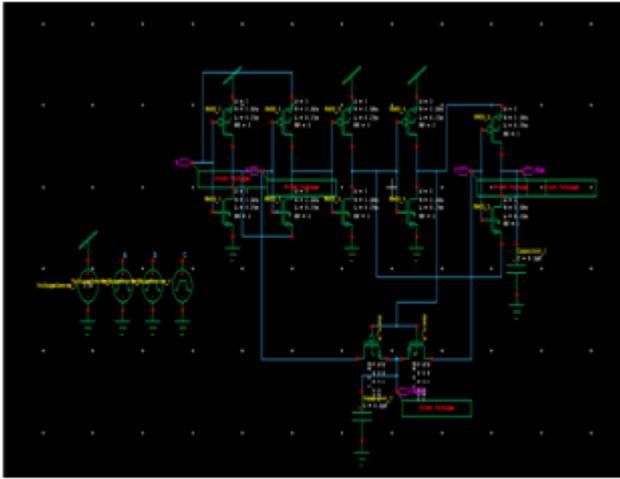


Figure 5: The proposed full adder cell with GDI technique

6. Simulation Results

Simulations have been performed using Tanner EDA 13.0 Simulation tool technology with supply voltage of 3.3V. Fig. 6 shows the input and output waveform results for proposed Full Adder. Table-2 shows comparison of power and delay value in previous system. Proposed Full adder provides sufficient output voltage level and noise margin of around 2V with 3.3V input signals.

The results of this proposed adder circuit can be compared with the different conventional adder circuit designs. Totally 12 transistors are needed to design the proposed adder circuit. Through this we can clearly decide that the proposed circuit can have lower area overhead than the other conventional adder circuits. From the results, it is clear that the proposed adder circuit can have the lower power values, very less delay and also lower PDP values as compared to other conventional adder circuits.

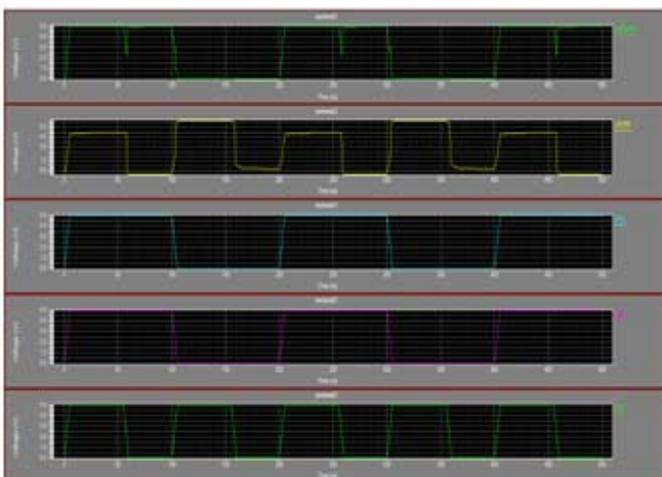


Figure 6: Snapshots of waveform for full adder cell

Table 2: Comparison of Power and Delay

Type	Power (μ W)	Delay (ns)	PDP	No of Transistor
CMOS Based Full Adder	1.29	0.653	0.832	28
GDI Based Full Adder	1.10x10 ⁻⁵	0.401	0.441	12

7. Conclusion

A novel 1-bit full adder cells using the XOR/XNOR gates have been proposed. The power dissipation, propagation delay and power-delay product of the proposed adders have been compared with the existing adders and are found to be efficient. GDI technique is implemented for Basic Logic Gates. The analysis shows that the full adder is novel and an effective technique for reducing power consumption, delay, power delay product (PDP), area and the Transistor count which will effectively reduce the size of the chip.

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