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Implementation of 100BASE-T4 Network Repeater Using FPGA

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Abstract: ***Embedded systems have, in the main, been designed around microcontrollers. But increasing demand for develop performance, efficient signal processing and parallel processing means FPGAs are pass more closely to the heart of the embedded systems. This paper presents the idea of 8 port 100BASE-T4 fast Ethernet repeater design targeting its FPGA implementation is proposed which supports 100Mb/s over low grade category 3 UTP. The total estimated power consumption for proposed design has 335mW after the post placement and routing on Xilinx xc3s400 device. FPGA implementation has various advantage of altering the function of the platform to perform several tasks. The implementation results show the minimum power consumption which reduce drastically compared to that of reported design.***

Keywords: FPGA, CRS, SFD, UTP

1. Introduction

Now a days a designer design a board level product in which FPGA provide the main functionality. The reason to specify an FPGA is its fast I/O response, interface flexibility, parallel processing potential and the ability to integrate specific functionality. More recently, power consumption, security and reliability have become critical. Power consumption is certainly important when it comes to design portable product. This paper concentrates on total estimated power consumption of 8 port Ethernet repeater. Ethernet is a common communication standard used in local area networks to share information between printer, modem, computer and other data device [1]. A Network Repeater is a device that allows many computers to connect to the network through cables connected to ports on the repeater. Repeaters are passive device in that they do not alter the frames that they receive. Instead, they transmit the frames to all ports. Each device receiving a data frame observe it to see if the frame was intend for that device, and if so it transmit the frame. In addition to providing connectivity, repeaters are also a form of hub.

The proposed design support 100BASE-T4 Ethernet standard in which 4 pair of wire in twisted cable. From four pair three are used for transmission and reception and one for collision detection. It is also called category 3 UTP (unshielded twisted pair). 100BASE-T4 is only the standard which support category 3 UTP. The repeater logically joins the cable segments to create a larger network. They improve reliability and performance of network [7]. Each repeater unit has a activity line which is connected to each of the other network repeater port. Each network repeater unit also includes a similar arbitration unit connected to the respective activity lines. When a network repeater port receives frame from a local transceiver for transmission, the arbitration unit of the network repeater unit force an activity signal onto the corresponding activity line.

In proposed method, the design of 8 port network repeater uses very high specific integrated circuit (VHSIC) hardware description language (VHDL) and its implementation targeting on Spartan FPGA device. 100BASE-T4 fast Ethernet provide a high performance solution at a low power. Advances in VLSI technology have pushed integration to the point where it is now possible to design and implement a microprocessor and network controller on a single chip, known as system on chip (SoC) [6]. It is a challenge to find the right balance between power and cost. This becomes more complicated when adding network capability to a device.

2. Network Repeater

Network repeater can be referred to as LAN extenders, Ethernet repeater, cat5 extenders, network extenders and network bridge use a variety of transmission technology over physical medium such as fiber or copper.

A. Basic objective of network repeater

- The objective of Network repeater is that they can exterminate the need for installing costly switches and category 5 wires.
- Collision detection.
- Plug and play device that u can install rapidly to take advantage of existing copper twisted-pair network underlying framework.
- Protect a network from failure of stations, cables, ports and so forth.
- Physical dimension of network extend.
- Cost for network installation provides low, growth and maintenance.

B. Design Specification

The basic function of the repeater is to receive a signal, raise its strength and force it out again. Transceiver performs the electrical function needed to interface the port to repeater core logic. We are not concern with the designing of the transceivers. Assuredly we will attention on the function of the repeater core logic. This requires that we have to work on the transceiver repeater core interface.

The signal crs (carrier sense) indicates that the incoming data is received by the transceiver circuit. Receive clock (rx_clk) clock recovered by the incoming data by the interface circuit and is used to synchronized the three pair of data (rxd0 – rxd5). The signal receive data valid (rx_dv) informs the repeater that the received data, is valid. The receive data error (rx_er) signal indicates that an error was detected in the reception of the data [3].

3. Proposed Network Repeater

To accomplish the function required of the network repeater, the incoming data first buffered and correct symbol generated. With other symbol buffered data must be multiplexed, rely on which data frame should be transmitted to active ports. According to the requirement of signals and operation one manageable unit is designed below as follows:

- Port controller
- Arbiter
- Clock multiplexer
- FIFO
- Symbol generator and output multiplexer
- Core controller

3.1 Port Controller

Here total eight port controllers in this design, one for each port of network repeater. Each port synchronizers crs, link_bar, enable_bar to tx_clk on the receive side. The activity signal is asserted when a carrier has been detected and synchronized. The arbiter uses activity signal to select a port from receives a data. [9] If a port controller's port has been selected and there is no collision, then rx_en is asserted. If the port is not the receiving port, then tx_en is asserted when core controller indicates that tx_data (transmit data) is ready.

The main problem with an Ethernet repeater is that frame collisions come about on the network. When two or more system on the network transmits data at the same time the data frames collide on the cable. When collision happens the network interfaces wait some random amount of time and retransmit data frame. A jam symbol must be generated in that condition and transmitted to all ports, including the one port which previously sending data. Collision caused port will then wait for an arbitrary length of time before attempting to resend data across the network [6]. If 40000 to 75000 successive bits are received from Ethernet port, the device at the other end of that wire is supposed to be 'jabbering", transmitting an infinite stream of bits, so the output from the port is cut off from the rest of the network.

If 60 consecutive collisions or more than 60 collisions are cache from any particular port, the repeaters will separation that port. It will stop processing information from that port, but will still continue to repeat all data frames from the network to the port. If the station on present port has fragmented so that it no longer is fallow the rules of CSMA/CD, then it required to be divided from the network to permit traffic to flow. If another port has been active for more than 450 to 560 bit times without the partition ports crs signal being asserted then the port controller deasserts partition_bar. These conditions will be determined by the value of collision and carrier, as well as whether or not the port has been selected.

3.2 Arbiter

The arbiter will use output activity signals from each of the port controller which supply eight selected signals to port controllers and clock multiplexer. These signals will indicate which port is receiving data. They will be used to gate the rx_en of that port and to choose the appropriate clock for waiting to the FIFO. The arbiter also supplies carrier and collision for use by the port controllers and core controller. Noselect is supplied to the clock multiplexer, indicating that no port is receiving a transmission. Under this condition, all port of the repeater transmits idle characters.

3.3 Clock Multiplexer

The inputs to the clock multiplexer are the eight receive clocks (rx_clk7- rx_clk0), the eight selected lines from the arbiter, noselect from the arbiter, areset, and txclk. Selected and noselect signals are used to select one of the receive clock as the receive clock, rx_clk, or the transmit clock tx_clk (if noselect) for use by the FIFO. In my coding I have considered rx_clk is the direct input to the core logic. The attempt is made to figure 1 hardware in VHDL except "clock multiplexer". I have taken output of clock multiplexer as an input to my design.

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3.4 FIFO

The FIFO will capture the incoming data on the receive side, storing six bits of data (rxd5 – rxd0) on the rising edge of rx_clk. Wptrclr (write-pointer clear), wptrinc (write-pointer increment) are used to advance or clear the FIFO and to indicate which register to read for the outputs demux5 – demux0.

3.5 Core Controller

The function of core controller controls the FIFO read and writes pointers and symbol generation. It also provides tx_data to indicate to the ports that data is ready. The core controller decides what data to transmit, data in the FIFO, or characters. To do this, the controller requires carrier, collision, receive data is valid, and rx_er (receive error) as input and asserts the FIFO and multiplexer control lines.[9]

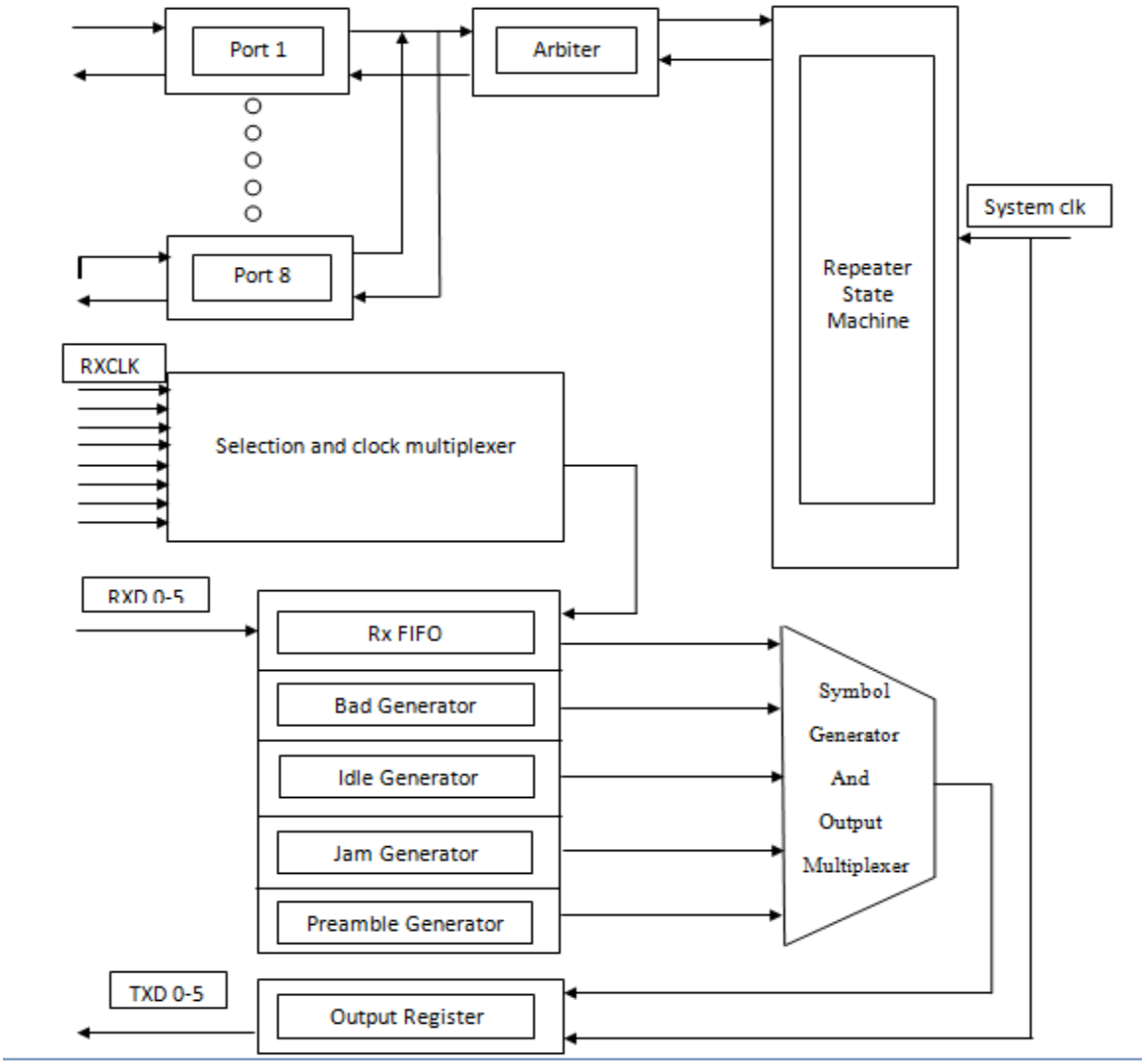

Figure 1: Block Diagram of Network Repeater

3.6 Symbol Generator and Output Multiplexer

The character symbol generator and output multiplexer will generate symbol. These symbols are the;

- Bad character, transmitted to indicate the receive error
- Jam character, transmitted to indicate collision
- Idle character, transmitted to indicate there is no activity on the network
- Preamble character, transmitted to allow for carrier sensing and clock recovery by the receiving node.[9]

4. Result

The proposed architecture is coded using VHDL. The design has been implemented using Xilinx project navigator. The target device is xc3s400 package pq208. Design is simulated using Modelsim simulator (Fig. 2). Result from synthesis report is shown in table number 1.

Number of slices	*Number of slice flip flop*	*Number of 4 input LUTs*	*Number of bounded IOBs*
3584	7168	7168	141

The proposed design is compared with various other similar designs and summery is given in table no. 2. Although the platforms are different, proposed design operates on 335 mW. Power consumption is measured using Xilinx Xpower tool and moderate power consumption is observed. Power analyzes Xilinx report view shown:

```
|------------------------------------------------------------------
Release  - XPower SoftwareVersion:G.28
Copyright (c) 1995-2004 Xilinx, Inc.  All rights reserved.
Design:       core
Preferences:  core.pcf
Part:         3s400pq208-4
Data version: ADVANCED,v1.0,11-03-03

Power summary:                          I(mA)     P(mW)
------------------------------------------------------------------
Total estimated power consumption:                 335
```

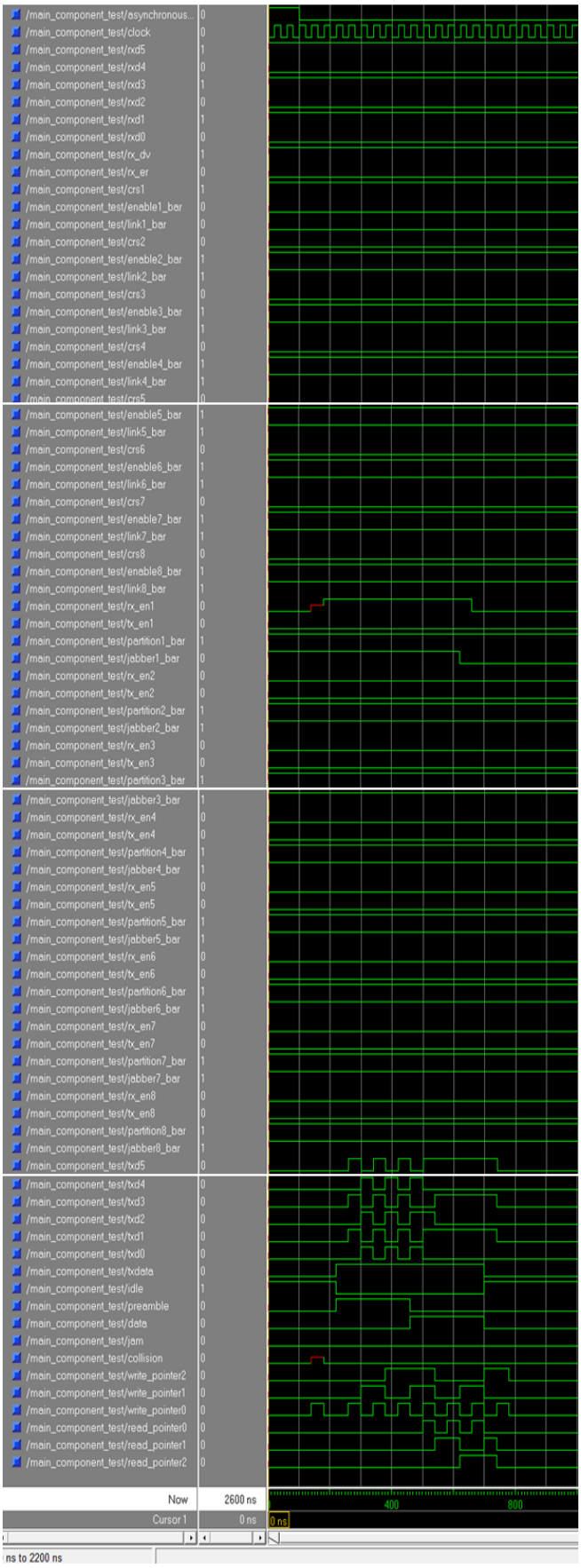

Figure 2: Simulation Waveforms

Table 2: Comparison with other design

Architecture	*Technology*	*Total power consumption*	*Number of ports*
[2]	VUL160A	4.4W	8
[3]	LXT9785	250mW	8
[4]	88E3082 88E3083	1200mW (150mW/port)	8
Proposed	SPARTAN3 XC3S400	335mW	8

5. Conclusion

The paper investigates that in network repeater there are five main components. Out of which port controller is the one facing more problems. In that unit there were combinational loop. From the simulation result shown in figure 2 it is concluded that the repeater receives data on port and retransmit to all other ports. The collision waveform is generated if more than one port active. After continuous transmission jabbering condition created. If the collision occur jam symbol generated. So, after simulating I got the simulation waveforms. In this way Network repeater perform the different functionality.

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