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A Survey on an VLSI Based Data Transfer Schemes

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Abstract: ***Packet data transfer scheme is introduced for intra chip data transfer to solve an interconnection problem. Double transmission lines are provided as a platform of the micro network. A protocol suitable for intra-chip data transfer is proposed to make a router as simple as possible. An application to a parallel VLSI processor is also discussed. In comparison with a multi-bus architecture the parallelism can be greatly increased under the same chip size because of the compactness of the micronetwork. Also a new packet data transfer scheme has been introduce (PDTS) is introduced to reduce the configuration control memory size of a multiple valued dynamic reconfigurable VLSI based on a logic memory architecture In PDTS the CCM size of the memory is proportional not to the no of the distributed memory modules in the reconfigurable Very Large Scale Integration but to the no of read operations in all the memories. Thus remarkable reduction of the CCM size can be achieved in comparison to the conventional control scheme. Moreover the PDTS contributes to fine grain ON/OFF control of current sources in Differential pair circuits(DPCS) utilizing flag information which indicates whether the data is valid or not.***

Keywords: Very large scale integration, packet data transfer technique, micro networks, energy consumption & system on chip interconnections

1. Introduction

One of the most serious problems is performance degradation due to interconnection complexity in recent System-on-Chip implementation. On-chip physical interconnections will present a limiting factor for performance and, possibly, energy consumption. The conventional multi-bus data transfer architecture requires a number of switches, which makes the chip area very large. This paper presents a packet data transfer scheme for intra-chip data transfer to solve the interconnection problem.

The proposed micro network consists of double transmission lines and routers. Each router is directly connected to a processing element (PE). It is the most important factor to implement the routers as simple as possible for reduction of hardware complexity. After completion of a router-router transfer mode, we provide a PE-router transfer mode. Such a two-mode packet data transfer scheme makes free from the packet collision, so that we can design a very simple and high speed router. An application to a parallel VLSI processor is also discussed. The area of the proposed micro network is sufficiently small, while its performance is almost same as the conventional multi-bus data transfer architecture. Therefore, more hardware resources can be contained in a chip size, and we can improve the total performance.

In the following discussion, we consider a single-chip VLSI processor composed of multiple PEs connected by micro network as shown in Fig.1. Assume that a processing algorithm is given, and it is represented by a control data graph (CDFG), so that the scheduling and allocation can be determined in advance. That is, static scheduling and allocation are effectively employed for the parallel processing including data transfer. Each node in the CDFG is allocated to a PE, and inter-PE data transfer corresponding to an edge is done through the micro network.

On the micro network, there are two transmission lines used for the packet data transfer: one is used for the direction from left to right; the other is used for the direction from right to left. Bit-parallel packet data transfer is done on the micro network. The packet data transfer between two points can be done through the routers directly connected to the PEs. As shown in Fig.1, a packet consists of a source address and a data address. Each router has a selection address which is used to determine whether the packet is received or not.

That is, the packet is received by the routers having the selection address equal to the source address. Then, the packet is transferred to the PE directly connected to the router. In the PDTS, one of the most important advantages is that the CCM size is almost proportional to the number of memory-access-related data transfer control operations. On the other hand, it is almost proportional to the number of LMEs in the conventional data transfer scheme. Therefore, the PDTS is suitable for the access control of the logic-in-memory VLSI. PDTS is applied to a multiple-valued fine-grain reconfigurable VLSI (MV-RVLSI) composed of DPCs. The complexity of interconnections and switch blocks can be reduced in comparison with the equivalent CMOS fine-grain reconfigurable VLSI. To reduce the power consumption of the MV-RVLSI, we propose current-source control, where current sources are turned OFF when the packet flag signal becomes invalid.

There are two hierarchies in the data transfer using the tree network. One is data transfer between LMEs, and the other is data transfer in an LME. We introduce packet data transfer between cell blocks, where a router is directly connected with each cell block instead of the switch node shown in Fig.2.Let us consider the data transfer in an LME as shown in Fig.3. The packet is composed of flag information which indicates whether a data is valid or invalid, a destination address and a data. Many small size CCMs are distributed over the local memory and a packet generator. Destination addresses without timing information are stored in the CCM for packet generators. Except for Read Enable of the local memory, timing information such as a clock step is replaced by the valid flag information. Load of the registers can be automatically generated after the destination address matches with the register ID address,

so that a CCM is not necessary to be provided for the registers. If the register receives a packet with the valid flag, the cell block operation becomes automatically started. The packet can be automatically received, so that the CCMs used to store receive timing information and write/load control information can be omitted.

In Table.1.bit size for the configuration/control information including Send Timing, Read Address of the local memory, Destination Address, Operation Mode of the cellblock and Write Address of the local memory becomes 39 bits. The control bits such as don't care and no-operation are not necessary to be stored in the CCM. A destination address is sent from the CCM to the packet generator. Simultaneously, a data with a valid flag is received from a local memory or a cell block. Then, the destination address and the data are combined together to form a packet. Assume that a processing algorithm is given, and it is represented by a control data flow graph(CDFG), so that the scheduling and allocation can be done advanced That is, static scheduling and allocation are effectively employed for parallel processing including data transfer

Table 1: Configuration control information control packet data scheme

DA: Destination Address
(00: LM, 01: REG1,10: REG2)

Packet Send No.	Send Timing	Read Address	PG1 DA
1	000	01010000 (80)	01
2	001	01010001 (81)	10

LM (Read) and PG1

Packet Input No.	Operation Mode
1	001 (Add)

Cell Block

Packet Input No.	PG2 DA
1	00

PG2

Packet Input No.	Write Address
1	01011010 (90)

LM (Write)

CCM size = 39(bit)

2. Literature Survey

In 1999, Sato T et.al developed a VLSI based technique 5-GByte/s data-transfer scheme suitable for synchronous DRAM memory systems [1]. To achieve a higher data-transfer frequency, the electrical properties were improved based on the frequency analysis of the memory system. Then, a bit-to-bit skew compensation technique that eliminates incongruent skew between the signals is described with a new, multi output controlled delay circuit to accomplish bit-to-bit skew compensation by controlling transmission timing of every data bit. To achieve a higher data-transfer frequency, such as 200 MHz, the electrical properties were improved based on the frequency analysis of the memory system. With the electric characteristic improvements to reduce stub-length, pin capacitance, and trace-length variations, the feasibility for 3.9-GByte/s data transfer was described. Furthermore, a bit-to-bit skew-compensating technique that eliminates incongruent skew between the signals, and the key controlled delay circuit REDD that achieves 30-ps resolution, were presented that extend the data-transfer-rate performance to over 5 Gbyte/s. The feasibility was also confirmed by the transient board-level timing simulation. The maximum data transfer rate resulted in 5.1 Gbyte/s even for the worst case.

In 2000, Sawchuk A et.al developed a smart pixel (SP) system for networking and image hide processing based on digital optoelectronic (DO) technology. DO technology enables 2-D optical data transfer to and from VLSI chips at a throughputs of >1 Tb/s, with very low latency (<lo ns) and very high speed *(>500* Mb/s) on each of many (>loo) parallel data channels [2]. Similar to most packets based networking schemes on serial interconnect links; the OPDPs contain data payload and source/destination node address information. The data pipe between nodes consists of a 2-D array of optical links each operating at on-chip clock rates. This data pipe between nodes is designed to accommodate the sum of all other smaller data pipes entering the network from individual nodes, thus- this system is an example of 'fire hose' architecture. Our goal is to demonstrate two features unique to SP systems: networking with 2-D spatial parallel channels and 2-D parallel pipeline image and video processing for applications such as compression and tracking.

In 2003, Hanyu T et.al developed a new asynchronous data transfer scheme using multiple-valued 2-color 1-phase coding, called a bidirectional data transfer scheme, is proposed for a high performance and low-power VLSI system. Valid data signals of "0" or "1" are represented by binary dual-rail complementary codes, (0,1) and (1,0), and "ODD" and "EVEN" colors are represented by binary dual-rail codes,(0,0) and (1,1), respectively [3]. Control signals from both a transmitter and a receiver are represented by dual-rail multiple-valued coding with superposition of data and color signals. The use of dual-rail coding makes it easy to detect EVEN and ODD information by calculating the sum of dual-rail codes, even when data and color information are mixed on the same wires in asynchronous data transfer. As a future prospect, it is also important to improve the circuit performance more and more in the bidirectional data transfer protocol. The performance of the proposed circuit is preliminarily dominated by the delay of current-mode comparators.

In 2005, Ito T et.al developed a VLSI based bit data transfer technique to achieve ultimate flexibility and a high-performance low-power operation equivalent to that of a full-custom VLSI. In this paper, a reconfigurable VLSI which realizes a high-performance sequential logic circuit based on a bit-serial operation is proposed [4]. A universal sequential logic module (USLM) suitable for local data transfer in a programmed sequential logic circuit is presented. A redundant multiple-valued sequential logic operation is also proposed, where linear summation of time-by-time adjacent bits is fully utilized to increase the input/output throughput of a sequential logic circuit. Moreover, packet data transfer scheme is introduced to make programmable interconnection possible in the bit-serial data transfer between cells composed of the multiple USLMs

.**In 2005, Homma Y et.al** proposed a VLSI based packet data transfer scheme for intra chip data transfer to solve an

interconnection problem [6]. Double transmission lines are provided as a platform of the micro network. A protocol suitable for intra-chip data transfer is proposed to make a router as simple as possible. An application to a parallel VLSI processor is also discussed. In comparison with a multi-bus architecture the parallelism can be greatly increased under the same chip size because of the compactness of the micro network reconfigurable VLSI processors. Thus, the new concept of packet data transfer will open up a new System-on-Chip technology.

In 2007, Gupta A et.al proposed a VLSI based technique for JPEG2000 is a new image compression standard known for its rich set of features, impressive compression performance as well as its complexity for efficient hardware implementation [7]. Discrete Wavelet Transform (DWT) and embedded Block Coder (BC) are two main modules in JPEG2000 compression system. Data transfer between the DWT and BC modules presents challenges due to difference in data format generated by the DWT and data format accepted by the BC module. In this paper, we investigate data transfer and storage techniques between the DWT and BC modules. We propose an efficient memory organization and a data transfer scheme to reduce the data bandwidth. A VLSI architecture for the proposed Data Transfer (DT) system is proposed and synthesized for TSMC 0.18 µm process. Simulation results show that our proposed techniques result in an aggregate reduction in the bandwidth requirement by a factor of four for the BC module while incurring an extra hardware cost of only 5%. Memory bandwidth is a main source of power consumption for data dominant applications such as JPEG2000. In this paper, we have proposed an efficient memory organization scheme based on 4-square unit for intermediate data storage between DWT and BC modules. Additionally SC and 4-SqC encoding schemes are proposed to reduce the memory bandwidth further. Simulations results show that a JPEG2000 system using our proposed memory organization and transfer techniques collectively result in a memory bandwidth requirement that is four time less than the existing techniques. A VLSI architecture is designed and synthesized using the ASIC TSMC 0.18 µm process. The results show that our proposed system has only 5% more hardware cost than the existing schemes.

In 2009, Okada N et.al proposed a multiple-valued reconfigurable VLSI useful for improving the utilization ratio of hardware resources [8]. Hybrid architecture based on wired programming and dynamic data-path control can be effectively employed for high utilization ratio of hardware resources with small overhead of additional hardware resources. A 2-to-1 multiplexer is provided in each cell. Accordingly, distributed control can be realized simply, so that interconnections between arithmetic logic modules and controllers become very short. Moreover, superposition of data and control signals is introduced to reduce not only complexity of interconnections but also switch block area. Hybrid architecture based on wired programming and dynamic data-path control contributes effective implementation of partially dynamically reconfigurable computation.

In 2012,Fujioka Y et.al proposed a register-transfer-level packet routing scheme is proposed to reduce a configuration memory size of a Dynamically Reconfigurable Processor (DRP) [9]. The RT(Register-Transfer)-driven concept makes the configuration memory size very small, because packets are not required to be provided at all the clock cycles. Buffer-less routers can be used to construct a compact DRP, if offline scheduling/allocation is effectively utilized to avoid packet collision. Dynamic reconfiguration of Local Memories (LMs) is also realized by the packet data transfer control. It is evaluated that the packet-routing configuration memory size can be reduced to about 1/10 under the Functional Unit (FU) utilization ratio of 10% in comparison with the conventional DRP. The compact router can be constructed based on the semiautonomous collision-free packet routing scheme, which will be useful for fine-grain packet data transfer, because a large number of the routers must be provided in the ultra-highly parallel processing. Thus, the larger number of PEs in the proposed routing network architecture can be put in a chip with the same size, and the parallel processing capability can be enhanced greatly.

In 2014, Harada s et.al proposed a new packet data transfer scheme (PDTS) is introduced to reduce a configuration/control memory (CCM) size of a multiple-valued dynamic reconfigurable VLSI based on a logic-in-memory architecture [10]. In the PDTS, the CCM size for memory access is proportional not to the number of distributed memory modules in the reconfigurable VLSI, but to the number of read operations in all the memories. Thus, remarkable reduction of the CCM size can be achieved in comparison with the conventional control scheme. Moreover, the PDTS contributes to fine-grain ON/OFF control of the current sources in Differential-Pair Circuits (DPCs) utilizing flag information which indicates whether the data is valid or invalid. The PDTS is introduced to not only inter-LME but also inter-cell data transfer. A packet data is transferred through data paths only when we make control signals changed. Therefore, the CCM size is proportional to the utilization ratio of the LMEs/cells. Specific control signals such as Load and Write can be automatically generated after a destination address matches with a register ID address, which also gives an advantage of the CCM size reduction. Moreover, power saving can be achieved based on the autonomous current-source control flag information. The CCM is distributed over each cell. However, the required CCM size is different each other between the cells.

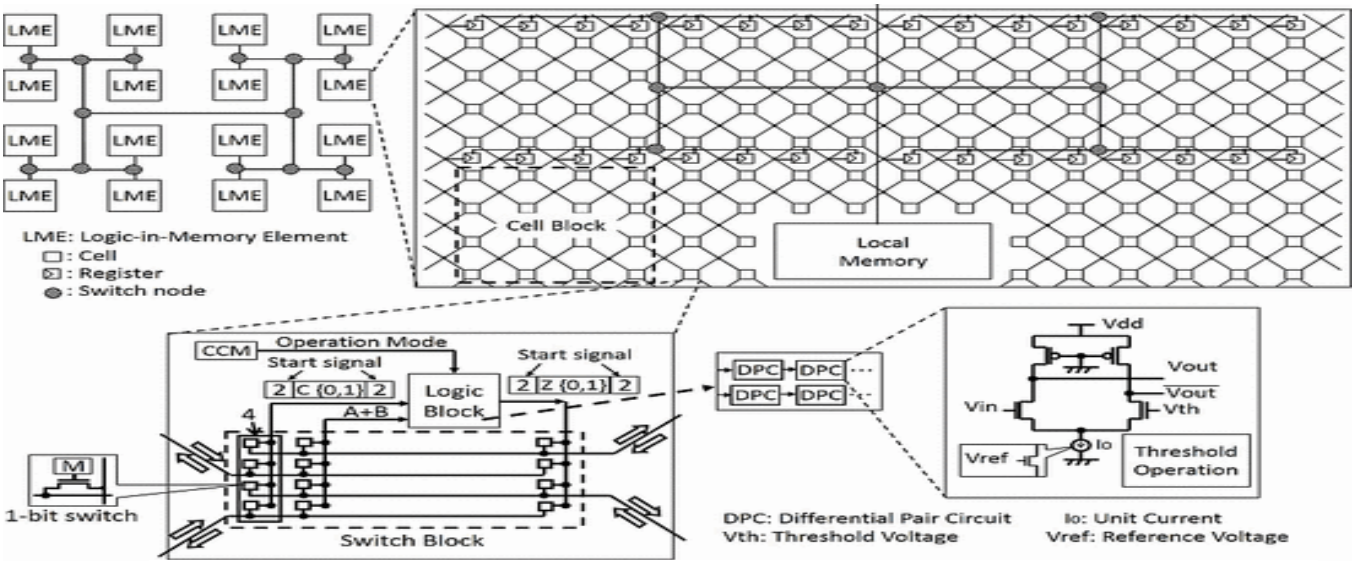

Figure 1: Logic-in-memory multiple-valued reconfigurable VLSI using a global tree network and a local x-net network

3. Comparative Analysis

Table 1: Comparative analysis on various methodologies for data transfer

Author	Year	Algorithm	Advantages	Disadvantages	Results
Harada s et al	2014	New packet data transfer scheme logic-in-memory architecture	1) Remarkable reduction of the CCM size can be achieved in comparison with the conventional control scheme. 2) Powersaving can be achieved based on the autonomous current-source controlflag	1) Increased area. 2) Increased power consumption during the pre-charge phase. 3) Delay in the evaluation phase.	1) Sharing of the CCM between multiple LMEs/cells will be effectively employed for achieving high utilization of the CCM 2) Analysed the effect of temperature variation in the security of the proposals.
Fujioka Y et.al	2012	Register-transfer-level packet routing scheme is proposed to reduce a configuration memory size of a Dynamically Reconfigurable Processor (DRP).	1) Balance the leakage of power consumption. 2) The concept makes the memory size very small	1) Impossible to detect source of attacker. 2) Both software as well as hardware complexities.	1) The power leakage is “eliminated” on the logic level and “masked” on the algorithmic level. 2) The timing of a packet send can be programmable in the packet generator, and register-transfer-driven packet send control can be done
Okada N et.al	2009	Hybrid architecture based on wired programming	1) For the first time, bottom pre-charge logic is used 2) Superposition of data and control signals is introduced to reduce complexity and area.	1) Additional circuits are needed. 2) High noise effect.	1) DPA resistance of the circuits developed using this cell. 2) Out-performing competing design.
Gupta A et.al	2007	Discrete Wavelet Transform (DWT) and embedded Block Coder (BC) are two main modules in JPEG2000 compression system.	1) Successfully repelled DPA attacks. 2) Reduction in data bandwidth. 3) Efficient memory organization scheme based on 4-square unit for intermediate data storage between DWT and BC modules	1) Do not have evenly distributed conditions. 2) Increased complexity of the circuit.	1) System has only 5% more hardware cost than the existing schemes. 2) Memory bandwidth requirement that is four time less than the existing techniques
Homma Y et.al	2005	Double transmission lines are provided as a platform of the micronetwork.	1) Security problem based on the ring oscillators is resolved. 2) The power consumption of cryptographic circuits will be independent of the predicted power consumption.	1) Corresponding mask should be used to recover the actual output data 2) Reset problem2.97-Gb/s throughput at an operating frequency of 255 MHz with a 0.104-mm2 cell	1. Parallelism can be greatly increased under the same chip size because of the compactness of the micro network reconfigurable VLSI processors.

Onizawa N et.al	2005	Asynchronous data-transfer scheme based on multiple-valued encoding	1) Area-efficient. 2) Since control signals and data from mutual nodes are multiplexed using a multi-level dual-rail codeword, the number of communication steps can be greatly reduced, which results in high-speed communication without any additional wires	1) Unable to meet performance requirements. 2) More and more modern embedded system. 3) An extensive comparison method.	1) A. duplex asynchronous data-transfer scheme based on multiple-valued encoding has been proposed. 2) Reduces 70.5% area of hardware accelerator based reference design.
Ito T et.al	2005	Reconfigurable VLSI which realizes a high performance sequential logic circuit based on a bit-serial operation	1) A balanced layout. 2) Can be applied to mesh architecture with different cluster sizes, different wire lengths and interconnect flexibilities.	1) WDDL may slow down the clock speed. 2) WDDL forbids the use of inverter cells. 3) WDDL requires 231.7% energy overhead.	1) The balance is drastically improved. 2) Differential delay is insignificant. 3) Programmableinterconnection possible in the bit-serial data transfer between cells composed of the multiple USLMs.
Hanyu T et.al	2003	Asynchronous data transfer scheme using multiple-valued 2-color 1-phase coding	1) The countermeasure circuit can be mounted onto different S-box implementations. 2) DPA-resistant AES chip can be proposed to maintain the same throughput with less than 2K extra gates.	1) The hardware cost is at least two times larger. 2) Throughput is degraded by at least 50%.	1) The area overhead to a single S-box is increased to 53.13% without lengthening the critical path delay. 2) The performance of the proposed circuit is preliminarily dominated by the delay of current-mode comparators.
Sawchuk A et.al	2000	Digital optoelectronic (DO) technology.	1) The data pipe between nodes consists of a 2-D array of optical links operating at on chip clock rates.This data pipe between nodes is designed. sum of all other smaller data pipes entering the network from individual nodes	1) Additive noise contribution. 2) Complex computations.	Good accuracy, as its error is always lower than 2%.
Sato T et.al	1999	Synchronous DRAM memory systems.	1) Simplicity 2) Simple Interfacing. 3) Algorithm independent.	1) Increase complexity 2) A shunt-shunt feedback loop hence the overall gain is decreased.	To achieve a higher data-transfer frequency, the electrical properties were improved based on the frequency analysis of the memory system.

4. Conclusion

This survey paper presents very simple packet data transfer architecture to solve the intra chip data transfer method to solve the interconnection problem developed to solve a SoC interconnection problem. Because arbitrary data transfer can be done by programming selection addresses, the flexibility of the data transfer scheme will give a solution for the interconnection problem also in dynamic reconfigurable VLSI processors. Thus, the new concept of packet data transfer will open up a new System-on-Chip technology

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