interconnection problem [6]. Double transmission lines are provided as a platform of the micro network. A protocol suitable for intra-chip data transfer is proposed to make a router as simple as possible. An application to a parallel VLSI processor is also discussed. In comparison with a multi-bus architecture the parallelism can be greatly increased under the same chip size because of the compactness of the micro network reconfigurable VLSI processors. Thus, the new concept of packet data transfer will open up a new System-on-Chip technology.

In 2007, Gupta A et.al proposed a VLSI based technique for JPEG2000 is a new image compression standard known for its rich set of features, impressive compression performance as well as its complexity for efficient hardware implementation [7]. Discrete Wavelet Transform (DWT) and embedded Block Coder (BC) are two main modules in JPEG2000 compression system. Data transfer between the DWT and BC modules presents challenges due to difference in data format generated by the DWT and data format accepted by the BC module. In this paper, we investigate data transfer and storage techniques between the DWT and BC modules. We propose an efficient memory organization and a data transfer scheme to reduce the data bandwidth. A VLSI architecture for the proposed Data Transfer (DT) system is proposed and synthesized for TSMC 0.18 µm process. Simulation results show that our proposed techniques result in an aggregate reduction in the bandwidth requirement by a factor of four for the BC module while incurring an extra hardware cost of only 5%. Memory bandwidth is a main source of power consumption for data dominant applications such as JPEG2000. In this paper, we have proposed an efficient memory organization scheme based on 4-square unit for intermediate data storage between DWT and BC modules. Additionally SC and 4-SqC encoding schemes are proposed to reduce the memory bandwidth further. Simulations results show that a JPEG2000 system using our proposed memory organization and transfer techniques collectively result in a memory bandwidth requirement that is four time less than the existing techniques. A VLSI architecture is designed and synthesized using the ASIC TSMC 0.18 µm process. The results show that our proposed system has only 5% more hardware cost than the existing schemes.

In 2009, Okada N et.al proposed a multiple-valued reconfigurable VLSI useful for improving the utilization ratio of hardware resources [8]. Hybrid architecture based on wired programming and dynamic data-path control can be effectively employed for high utilization ratio of hardware resources with small overhead of additional hardware resources. A 2-to-1 multiplexer is provided in each cell. Accordingly, distributed control can be realized simply, so that interconnections between arithmetic logic modules and controllers become very short. Moreover, superposition of data and control signals is introduced to reduce not only complexity of interconnections but also switch block area. Hybrid architecture based on wired programming and dynamic data-path control contributes effective implementation of partially dynamically reconfigurable computation.

In 2012,Fujioka Y et.al proposed a register-transfer-level packet routing scheme is proposed to reduce a configuration memory size of a Dynamically Reconfigurable Processor (DRP) [9]. The RT(Register-Transfer)-driven concept makes the configuration memory size very small, because packets are not required to be provided at all the clock cycles. Buffer-less routers can be used to construct a compact DRP, if offline scheduling/allocation is effectively utilized to avoid packet collision. Dynamic reconfiguration of Local Memories (LMs) is also realized by the packet data transfer control. It is evaluated that the packet-routing configuration memory size can be reduced to about 1/10 under the Functional Unit (FU) utilization ratio of 10% in comparison with the conventional DRP. The compact router can be constructed based on the semiautonomous collision-free packet routing scheme, which will be useful for fine-grain packet data transfer, because a large number of the routers must be provided in the ultra-highly parallel processing. Thus, the larger number of PEs in the proposed routing network architecture can be put in a chip with the same size, and the parallel processing capability can be enhanced greatly.

In 2014, Harada s et.al proposed a new packet data transfer scheme (PDTS) is introduced to reduce a configuration/control memory (CCM) size of a multiple-valued dynamic reconfigurable VLSI based on a logic-in-memory architecture [10]. In the PDTS, the CCM size for memory access is proportional not to the number of distributed memory modules in the reconfigurable VLSI, but to the number of read operations in all the memories. Thus, remarkable reduction of the CCM size can be achieved in comparison with the conventional control scheme. Moreover, the PDTS contributes to fine-grain ON/OFF control of the current sources in Differential-Pair Circuits (DPCs) utilizing flag information which indicates whether the data is valid or invalid. The PDTS is introduced to not only inter-LME but also inter-cell data transfer. A packet data is transferred through data paths only when we make control signals changed. Therefore, the CCM size is proportional to the utilization ratio of the LMEs/cells. Specific control signals such as Load and Write can be automatically generated after a destination address matches with a register ID address, which also gives an advantage of the CCM size reduction. Moreover, power saving can be achieved based on the autonomous current-source control flag information. The CCM is distributed over each cell. However, the required CCM size is different each other between the cells.

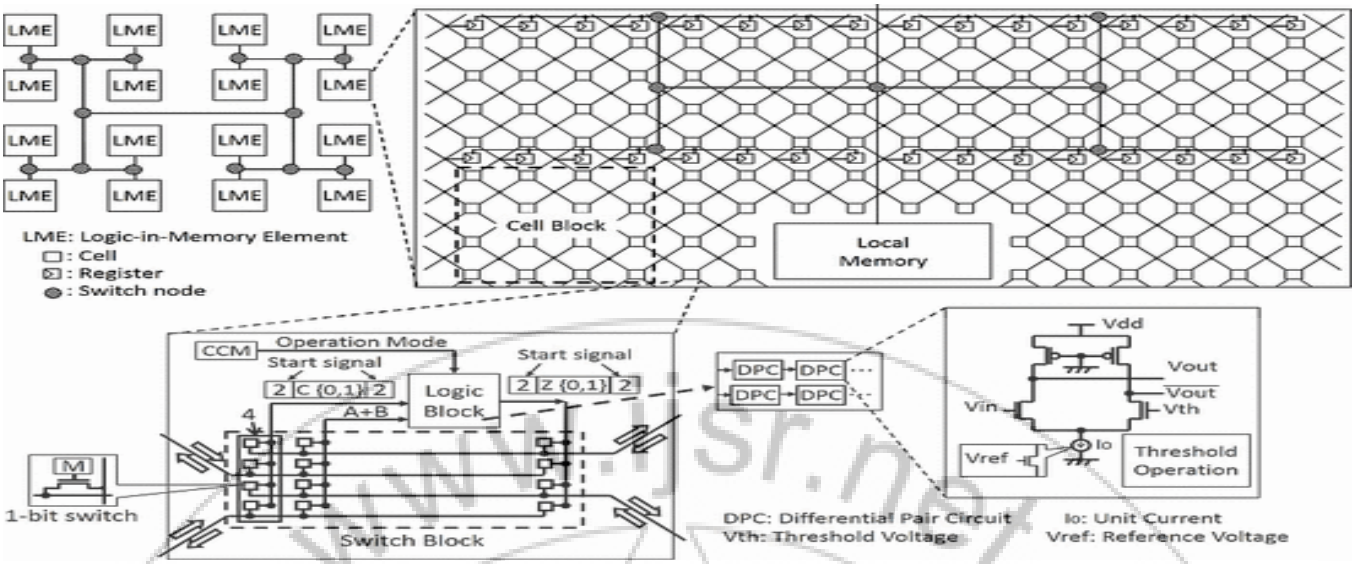

Figure 1: Logic-in-memory multiple-valued reconfigurable VLSI using a global tree network and a local x-net network

3. Comparative Analysis

Table 1: Comparative analysis on various methodologies for data transfer

Author	Year	Algorithm	Advantages	Disadvantages	Results
Harada s et al	2014	New packet data transfer scheme logic-in-memory architecture	1) Remarkable reduction of the CCM size can be achieved in comparison with the conventional control scheme. 2) Powersaving can be achieved based on the autonomous current-source controlflag	1) Increased area. 2) Increased power consumption during the pre-charge phase. 3) Delay in the evaluation phase.	1) Sharing of the CCM between multiple LMEs/cells will be effectively employed for achieving high utilization of the CCM 2) Analysed the effect of temperature variation in the security of the proposals.
Fujioka Y et.al	2012	Register-transfer-level packet routing scheme is proposed to reduce a configuration memory size of a Dynamically Reconfigurable Processor (DRP).	1) Balance the leakage of power consumption. 2) The concept makes the memory size very small	1) Impossible to detect source of attacker. 2) Both software as well as hardware complexities.	1) The power leakage is "eliminated" on the logic level and "masked" on the algorithmic level. 2) The timing of a packet send can be programmable in the packet generator, and register-transfer-driven packet send control can be done
Okada N et.al	2009	Hybrid architecture based on wired programming	1) For the first time, bottom pre-charge logic is used 2) Superposition of data and control signals is introduced to reduce complexity and area.	1) Additional circuits are needed. 2) High noise effect.	1) DPA resistance of the circuits developed using this cell. 2) Out-performing competing design.
Gupta A et.al	2007	Discrete Wavelet Transform (DWT) and embedded Block Coder (BC) are two main modules in JPEG2000 compression system.	1) Successfully repelled DPA attacks. 2) Reduction in data bandwidth. 3) Efficient memory organization scheme based on 4-square unit for intermediate data storage between DWT and BC modules	1) Do not have evenly distributed conditions. 2) Increased complexity of the circuit.	1) System has only 5% more hardware cost than the existing schemes. 2) Memory bandwidth requirement that is four time less than the existing techniques
Homma Y et.al	2005	Double transmission lines are provided as a platform of the micronetwork.	1) Security problem based on the ring oscillators is resolved. 2) The power consumption of cryptographic circuits will be independent of the predicted power consumption.	1) Corresponding mask should be used to recover the actual output data 2) Reset problem2.97-Gb/s throughput at an operating frequency of 255 MHz with a 0.104-mm2 cell	1. Parallelism can be greatly increased under the same chip size because of the compactness of the micro network reconfigurable VLSI processors.

Onizawa N et.al	2005	Asynchronous data-transfer scheme based on multiple-valued encoding	1) Area-efficient. 2) Since control signals and data from mutual nodes are multiplexed using a multi-level dual-rail codeword, the number of communication steps can be greatly reduced, which results in high-speed communication without any additional wires	1) Unable to meet performance requirements. 2) More and more modern embedded system. 3) An extensive comparison method.	1) A. duplex asynchronous data-transfer scheme based on multiple-valued encoding has been proposed. 2) Reduces 70.5% area of hardware accelerator based reference design.
Ito T et.al	2005	Reconfigurable VLSI which realizes a high performance sequential logic circuit based on a bit-serial operation	1) A balanced layout. 2) Can be applied to mesh architecture with different cluster sizes, different wire lengths and interconnect flexibilities.	1) WDDL may slow down the clock speed. 2) WDDL forbids the use of inverter cells. 3) WDDL requires 231.7% energy overhead.	1) The balance is drastically improved. 2) Differential delay is insignificant. 3) Programmableinterconnection possible in the bit-serial data transfer between cells composed of the multiple USLMs.
Hanyu T et.al	2003	Asynchronous data transfer scheme using multiple-valued 2-color 1-phase coding	1) The countermeasure circuit can be mounted onto different S-box implementations. 2) DPA-resistant AES chip can be proposed to maintain the same throughput with less than 2K extra gates.	1) The hardware cost is at least two times larger. 2) Throughput is degraded by at least 50%.	1) The area overhead to a single S-box is increased to 53.13% without lengthening the critical path delay. 2) The performance of the proposed circuit is preliminarily dominated by the delay of current-mode comparators.
Sawchuk A et.al	2000	Digital optoelectronic (DO) technology.	1) The data pipe between nodes consists of a 2-D array of optical links operating at on chip clock rates.This data pipe between nodes is designed. sum of all other smaller data pipes entering the network from individual nodes	1) Additive noise contribution. 2) Complex computations.	Good accuracy, as its error is always lower than 2%.
Sato T et.al	1999	Synchronous DRAM memory systems.	1) Simplicity 2) Simple Interfacing. 3) Algorithm independent.	1) Increase complexity 2) A shunt-shunt feedback loop hence the overall gain is decreased.	To achieve a higher data-transfer frequency, the electrical properties were improved based on the frequency analysis of the memory system.

4. Conclusion

This survey paper presents very simple packet data transfer architecture to solve the intra chip data transfer method to solve the interconnection problem developed to solve a SoC interconnection problem. Because arbitrary data transfer can be done by programming selection addresses, the flexibility of the data transfer scheme will give a solution for the interconnection problem also in dynamic reconfigurable VLSI processors. Thus, the new concept of packet data transfer will open up a new System-on-Chip technology

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