Analysis of Low Power Test Pattern Generator by Using Low Power Linear Feedback Shift Register (LP-LFSR)

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Abstract: *This paper proposes a low power Linear Feedback Shift Register (LP-LFSR) for Test Pattern Generation (TPG) technique with reducing power dissipation during testing of VLSI circuits through the built in self test (BIST) approach. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. This proposed test pattern generator reduces the switching activity among the test patterns at the most. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive–ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. The simulation and synthesis results were carried out with the modelsim-altera 6.5b (Quartus-II 9.1) version and Xilinx ISE design environment 12.1 version respectively. The simulation results show the comparison of reduced number of transitions between the test patterns, which are generated by the proposed and existing systems. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.*

Keywords: TPG. BIST, LP-LFSR, Switching activity

1. Introduction

In VLSI circuits, built in self test (BIST) are used for testing. The objective of the BIST is to reduce power dissipation without affecting the fault coverage [1].The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. For example, the platform FPGAs such as Xilinx Virtex II Pro and Altera Excalibur include custom designed fixed programmable processor cores together with millions of gates of reconfigurable logic devices. In addition to this, the development of Intellectual Property (IP) cores for the FPGAs for a variety of standard functions including processors, enables a multimillion gate FPGA to be configured to contain all the components of a platform based FPGA. Development tools such as the Altera System-On-Programmable Chip (SOPC) builder enable the integration of IP cores and the user designed custom blocks with the Nios II soft-core processor. Soft-core processors are far more flexible than the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test.

In general, the power dissipation of a system in test mode is more than in normal mode [2]. Four reasons are blamed for power increase during test [3].

- High switching activity due to nature of test patterns
- Parallel activation of internal cores during test
- Power consumed by extra design-for-test (DFT) circuitry
- Low correlation among test vectors

This extra average and peak power consumption can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product field and life time[4]. Thus special care must be taken to ensure that the power rating of circuits is not exceeded during test application. Different types of techniques are presented in the literature to control the power consumption. These mainly includes algorithms for test scheduling with minimum power, techniques to reduce average and peak power, techniques for reducing power during scan testing and BIST(built-in-self test) technique. Since off-chip communication between the FPGA and a processor is bound to be slower than on chip communication, in order to minimize the time required for adjustment of the parameters, the built in self test approach using design for testability technique is proposed for this case.

The rest of the paper is organized as follows. In section II, presents the literature survey i.e. previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, the proposed technique in the test pattern generator is discussed. In Section V describes the algorithm for the proposed LP-LFSR. In section VI, the implementation

details and the results are presented. Section VII summarizes the conclusion.

2. Literature Survey

Y.Zorian [3] presented that the power dissipation of a system in test mode is more than in normal mode. P.Girard [4] demonstrated that four reasons are blamed for power increase during test.

- Due to nature of test patterns, high switching activity occurs.
- During test mode, parallel activation of internal cores happens.
- Extra design-for-test (DFT) circuitry consumes power.
- Low correlation among test vectors.

Mechrdad Nourani [5] explained that this extra average power consumption and peak power consumption can create problems such as instantaneous power surge that cause formation of hot spots, circuit damage, difficulty in performance verification and reduction of the product field and life time. Thus, special care must be taken to ensure that the power rating of circuits is not exceeded during test application.

Different types of methods are stated to control the power consumption. These methods mainly includes algorithms for test scheduling with minimum power, techniques to reduce peak power and average power, techniques for reducing power during scan testing and BIST(built-in-self-test) technique. In order to minimize the time required for adjustment of the parameters, off-chip communication between a processor and the FPGA is bound to be slower than on-chip communication. The BIST (built-in-self-test) approach using design for testability technique is presented for this case.

Different techniques are available to reduce the switching activities of test pattern, which reduces the power in test mode. P. Giard proposed a modified clock scheme for linear feedback shift register (LFSR), in which only half of the D flip-flops works. Thus, only half of the test pattern can be switched. S.K.Guptha determined a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus, the test pattern generated by original LFSR is re-arranged to reduce the switch frequency. Mechrdad Nourani [5] presented low transition test pattern generator (LT-TPG) which reduces the average and peak power of a circuit during test. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

A better low power can be achieved by using Single input change pattern generators. Voyiatzis et al.,[8] and S.C.Lei et al.,[9] demonstrated that the combination of scan shift register and LFSR are used to generate random single input change sequences. S.C. Lei et al., [9] and R.H.He et al., [10] proposed that (2^m-1) single input change test vectors can be inserted between two adjustments Vectors generated by LFSR where m is length of LFSR. BOYE and Tian-Wang Li [11] proposed that 2^m single input changing data is inserted between two neighbouring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

3. Power Analysis for Testing

In CMOS technology, the power dissipation can be classified into static and dynamic. Static power dissipation is mainly due to the leakage current. Dynamic power dissipation is due to switching transient current and charging and discharging of load capacitances. Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E_i = 1/2 \ V_{dd}^2 C_0 F_i S_i \ (1)$$

Where V_{dd} is the supply voltage, C_0 is the load Capacitance. The product of F_i and S_i is called weighted switching activity of internal circuit node i. The average power consumption of internal circuit node i can be given by,

$$P_i = 1/2 \ V_{dd}^2 C_0 F_i S_i \ f \ (2)$$

Where f is the clock frequency. The summary of P_i of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.
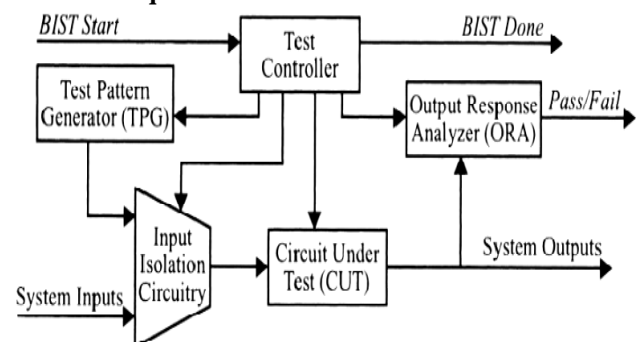
BIST Technique

Figure 1:.BIST Basic block diagram

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR].The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation[5].It causes excessive power dissipation and results in delay penalty into the design[6]

4. Proposed Method

A.LP-LFSR (Low Power Linear Feedback Shift Register)

LP-LFSR is a combining technique of random pattern generation called R-Injection (RI) and Bipartite LFSR for low-power BIST as shown in Fig.2 below. The new LP-LFSR generates three intermediate patterns. The RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI's activities and eventually switching activities in the circuit under test.
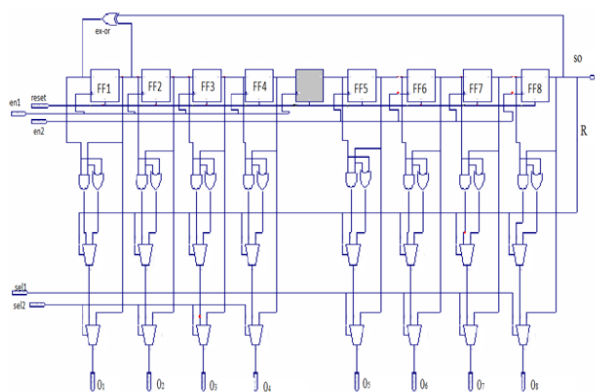
Figure 2: LP-LFSR

B. Low Power Test Pattern Generation Using LP-LFSR

Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns. In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LP-LFSR), m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.
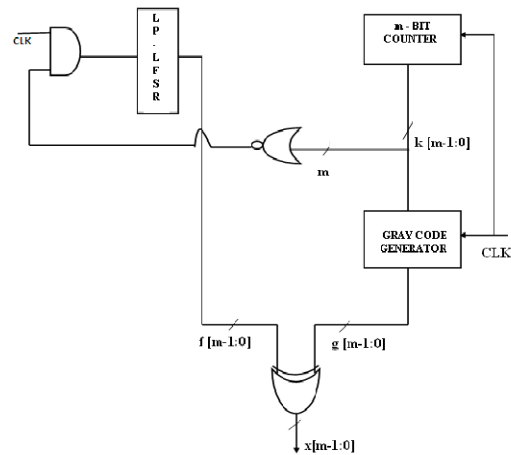

Figure 3:.Low Power Test Pattern Generator

5. Algorithm for LP-LFSR

The algorithm for LP-LFSR is given below.
- Consider an N-bit external (or) internal linear feedback shift register [n>2].
- For example n-bit, external LFSR is taken, which consists of n-flip flops in series. A common clock signal is applied as control signal for all flip flops.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the last stage flip flop output is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- If the last stage flip flop output is Zero, no swapping will be carried out.
- The output from other flip flops will be taken as such.
- If the LFSR is moved through a complete cycle of 2n states then the transitions expected are 2n-1.When the output of the adjacent flip flops are swapped, the expected transitions are 2n-2.Thus the transitions produced are reduced by 50% compared with original LFSR. The transition reduction is concentrated mainly on any one of the multiplexer output.
- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

$g[n-1] = k[n-1]$
$g[n-2] = k[n-1]$ XOR $k[n-2]$
.
.
$g[2] = k[2]$ XOR $k[3]$
$g[1] = k[1]$ XOR $k[2]$
$g[0] = k[0]$ XOR $k[1]$

In [12] it is stated that that the conventional LFSR's outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.
X [0] = f [0] XOR g [0]
X [1] = f [1] XOR g [1]
X [2] = f [2] XOR g [2]

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X [3] = f [3] XOR g [3]
X [4] = f [4] XOR g [4]
X [5] = f [5] XOR g [5]
.
.
.
X [n-1] = f[n-1] XOR g[n-1]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR. Fig. 3 is an example of counter and its respective gray value. It is shown that all values of g[2:0] are single input changing patterns.

Patterns:

K [2:0] g [2:0]
K0= 000 g0= 000
K1= 001 g1= 001
K2= 010 g2= 011
K3= 011 g3= 010
K4= 100 g4= 110
K5= 101 g5= 111
K6= 110 g6= 101
K7= 111 g7= 100

6. Implementation Details And Results

To validate the effectiveness of the proposed method, we select Test pattern generator (TPG) using conventional linear feedback shift register [LFSR] for comparison with proposed system.

A. Simulation Results Using Existing Conventional LFSR

The 8-bit pattern is generated using the LFSR configuration as shown in Fig.4 below. The schematic in the case of conventional pattern generation consists of 8 flip-flops connected in series. The outputs of the 8-bit LFSR are used as the inputs to the c432 ISCAS-85 interrupt controller design circuit.
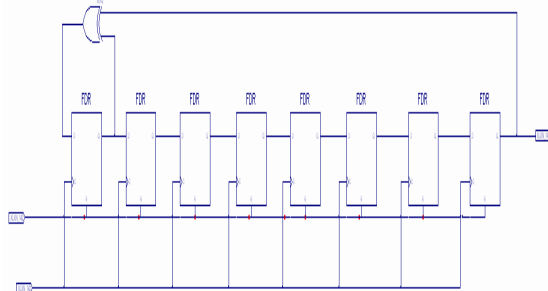

Figure 4: 8-bit LFSR

The 8-bit LFSR Designed Circuit Simulation is implemented using Mentor's **ModelSim tool 6.5b (Quartus II 9.1)** in the Xilinx ISE development environment. This simulation results generate multiple input changing test patterns i.e. more number of transitions present between the patterns as shown in the Fig.5 below.
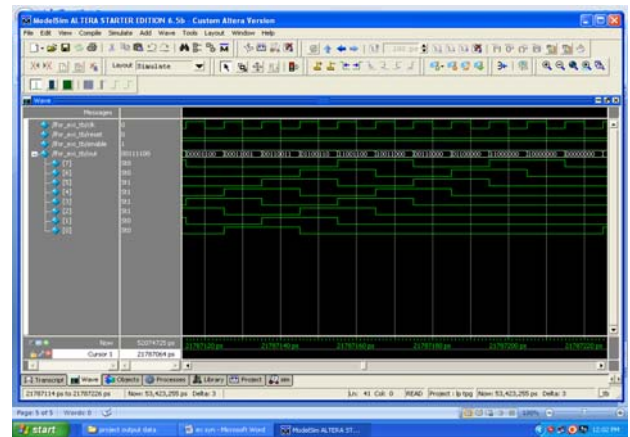

Figure 5:.Simulation Results of Existing LFSR

These LFSR test patterns consume high power during testing of VLSI circuits through BIST technique.

1. Disadvantages of Existing System

- Conventional LFSR (linear feedback shift register) Generates multiple input changing test patterns then High switching activity introduced while testing of a circuit
- power consumption is high during testing of circuits with using LFSR test patterns
- Ground noise is introduced between the patterns

These disadvantages are overcome by using proposed design of low power test pattern generation using low power linear feedback shift register (LP-LFSR)

B. Simulation Results Using Proposed LP-LFSR

LP-LFSR (8-bit) low power test pattern is generated by simulating the low power test pattern generator circuit. Designed circuit simulation was implemented by using Mentor's **ModelSim tool 6.5b (Quartus II 9.1)** in the Xilinx ISE development environment as shown in Fig.6 below.
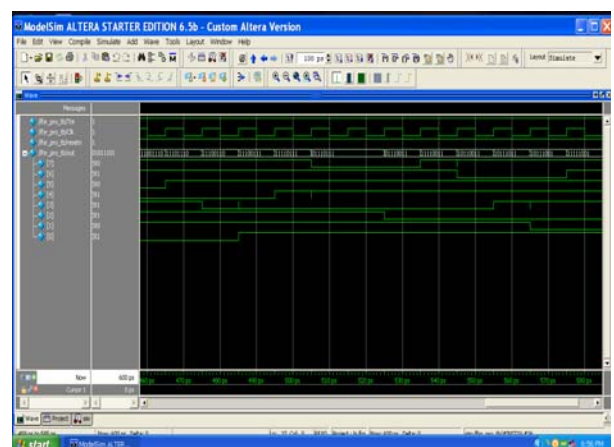

Figure 6: Simulation results of proposed LP-LFSR

This simulation report confirms the number of signal transitions between the bits of the successive vectors is reduced. This Proposed method generates single input changing test patterns. Then power consumption is reduced while using these test patterns in testing of a circuit through BIST technique.

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C. Synthesis Results of Existing System

The 8-bit existing LFSR Designed Circuit synthesis is implemented using **Xilinx ISE design environment 12.1** version and the results are shown in Fig's 7 to 9 below.
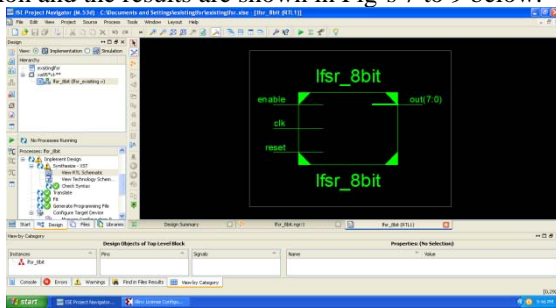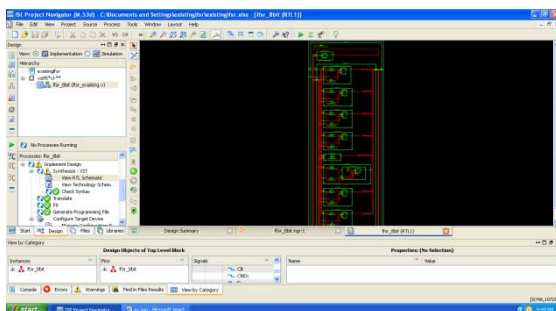

Figure 7: LFSR (8 bit) top module

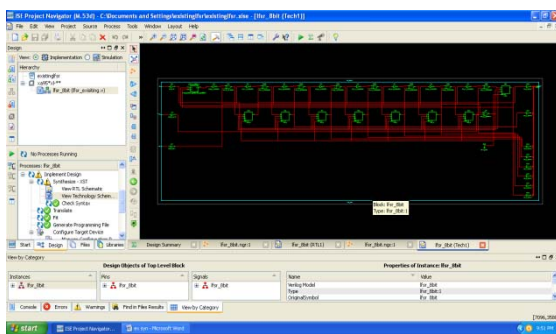**Figure 8:** LFSR RTL Schematic

Figure 9:.LFSR TECHNOLOGY Schematic

D.Synthesis Results of Proposed System

The 8-bit proposed LP-LFSR Designed Circuit synthesis is implemented using **Xilinx ISE design environment 12.1** version and the results are shown in Fig's 10 to 12 below.
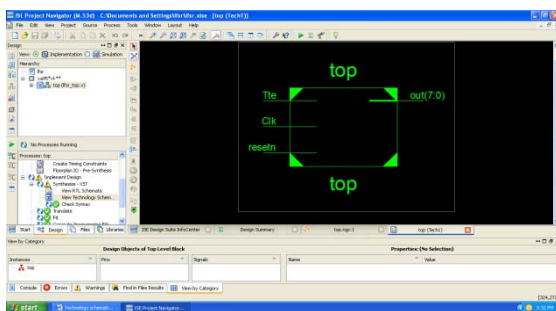

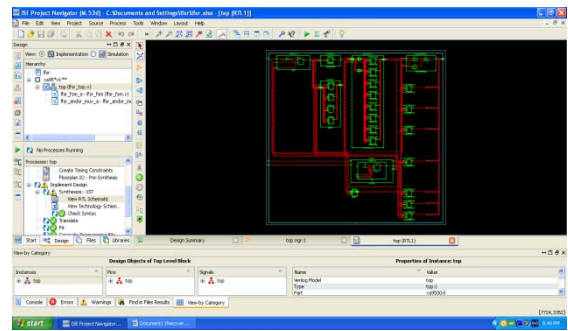**Figure 10:** LP LFSR (8 bit) top module
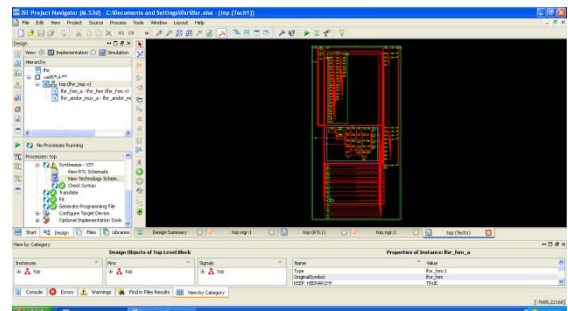

Figure 11:.LP LFSR RTL Schematic

Figure 12: LP LFSR TECHNOLOGY Schematic

Switching activities for multiple input changing sequence will be more than the single input changing sequence, thus the proposed method provides better test power reduction than any other low power method. From the implementation results, it is verified that the proposed method generates single input changing test patterns. Then power consumption is reduced while using these test patterns in testing of a circuit through BIST technique.

7. Conclusion

The low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

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