International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Impact Factor (2012): 3.358

Analysis of Zero Voltage Switching, Power Factor Correction for four switches Three Phase Three Level Boost Rectifier

Arpit Panchratan[1], Shobhit Jain[2]

[1] Master of Engineering (Power Electronics), SATI VIDISHA (M.P.), India

[2] Master of Engineering (Power Electronics), SATI VIDISHA (M.P.), India

Abstract: ***Analysis of zero voltage switching PFC (power factor correction) for four switch Three Phase Three Level Boost Rectifier introduced for achieving less input current and less respective total harmonic distortion (THD). By using four switches, phenomenon also achieved two low output nd one common output for the three different application at the same time using 340 volt V_{L-L} input voltage and also achieved unity power factor.***

Keywords: power factor correction, boost rectifier, ZVS, ZCS, EMI.

1. Introduction

Actually the analysis of the three phase boost rectification is typical, but after the analyzing of this simulation model technique it is easily done. Previously Zero voltage switching power factor correction for three phase three level boost rectifier introduced which gives the path to design this SIMULINK model.

For high voltage application, this model helps to easily analyze the changes in input current at full load and different switching states.

This model achieve less input current over high output voltage and also less correspondence THD ie. < 3% at over the 10 to 12% output voltage.

The balancing output achieved by using the balancing capacitive load, connects two capacitors in series at load for balancing the output voltage .this gives two lower output and single common high voltage. Hare also use the clamping diodes performance which clamp the output and help for the input power factor correction. Because of the clamping phenomenon the clamping noise occur which effect the input current , so eliminating this type noise EMI (Electromagnetic interference) filter use hare.

EMI filter is usually a capacitor inductor topology for handling this type of disturbances in input current.

Transformer of EMI actually uses for the dot convention performances so the same winding resistance and should be the same winding voltage of each winding use here

2. Proposed Block Diagram

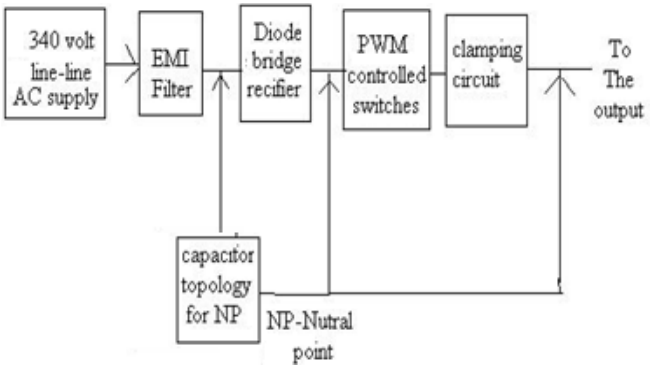

Figure 1: Proposed system for modal

The figure shows the three phase three level model of ZVS PFC BOOST rectifier proposed modal. In the circuit see the 3 phase input given to the EMI filter for avoiding the clamped noise. And then the input given to the Rectifier which is control by the four switches. Switches can be performed by the PWM method. Than the output of the rectifier is connected with the clamped capacitors' that connected in series. Connect the load across these capacitors and measure the output voltage.

3. Simulink Model and Analysis

The zvs pfc for three phase three level boost rectifier SIMULINK model present in figure 3 . C1,C2 and C3 are the three capacitors connected in Y (star connection) In this model and this connection create a neutral point . The nutral point once connected with middle of pairs of switches and middle of output capacitors also. Which helps the balancing the output voltage.

C_c (Clamping capacitor) connected across the switches. take two winding linear transformer having same winding voltage and same resistance of the winding For clamped inductor. C_R is the reset capacitor that use for reset the

inductor current connected with pair of switches serially. C_{O1} and C_{o2} the out put capacitors

By figure 4(a) saw when the switch S_1 and S_2 on inductor current i_{L1} flows from inductor L_1 , S_1 and S_2 the i_{o1} flows through V_{o1} and switches capacitor V_{cc} will charged. After some time switch S_2 will turned off then than the V_{cc} going to discharged and current flows from S_2 , S_3 . the measured current peak of i_{L1} is equal to V_{AN}/L_1.

When the diode D_{C1} is forward biased than the current i_{L1} decreases linearly then the current calculated by equation,

$$i_{L1} = \frac{V_{AN} - (1-2D)V_{o1}}{2L_1} T_S$$

After some time the switch S_1 also off. After some delay the switch S_3 and S_4 are on fig 4(b) . This phenomenon actually for the negative half cycle for the rectifier. At this time current i_{L2} and i_{L3} flows through to the inductor L_2 and L_3 and also the current going to the V_{o2}side.

When the diodes D_{C2} and D_{C3} are forward biased than the current i_{L2} and i_{L3} are simultaneously increases linearly.

$$i_{L2} = \frac{-V_{AN} + (1-2D)V_{o2}}{2L_2} T_S$$

4. Switching Operation MOSFET

In the modal take the PWM method for switching performance. The figure-4 shows the switching phenomenon of the MOSFET When the S1 is ON then the S2 also ON for some instantaneous of time, then it will OFF.

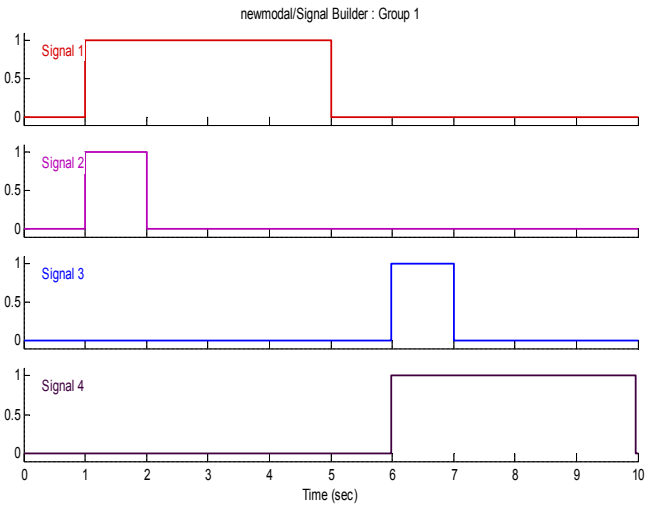

Figure 2: Switching pulses for the MOSFET switches

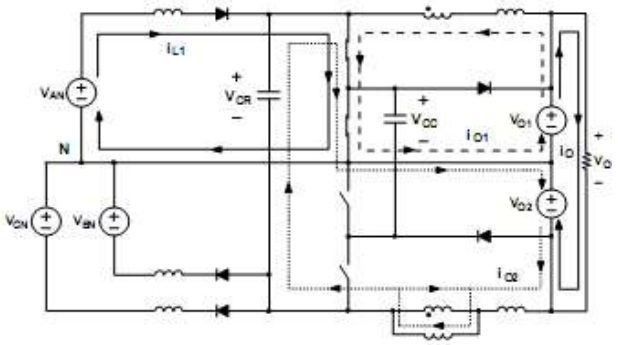

Figure 3(a)

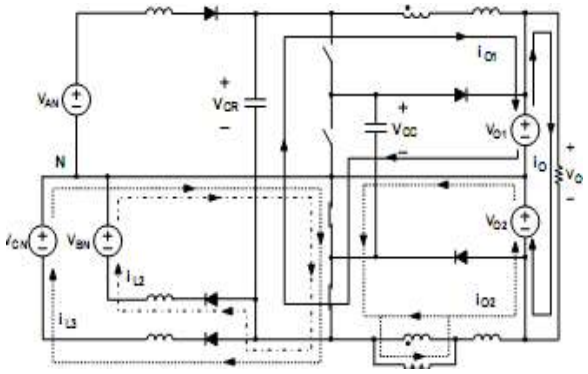

Figure 3(b)

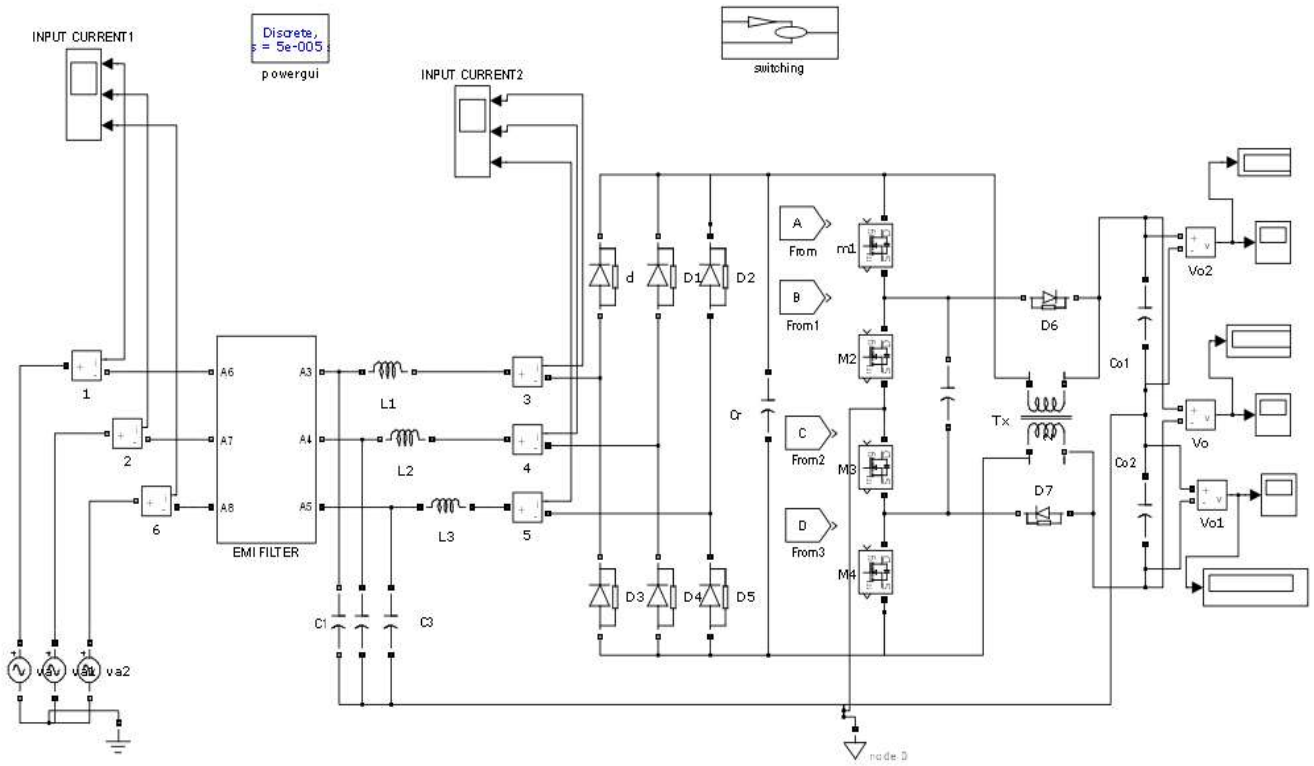

Figure 3: The Three Phase Three Level ZVS THD PFC Rectifier MATLAB Simulink Model

Fig 3- analysis of the modal fig-3(a) and 3(b) for the switch operation of S_1 ,S_2, S_3 and S_4 . figure 4 shows the simulation switching model for the MOSFET switches.

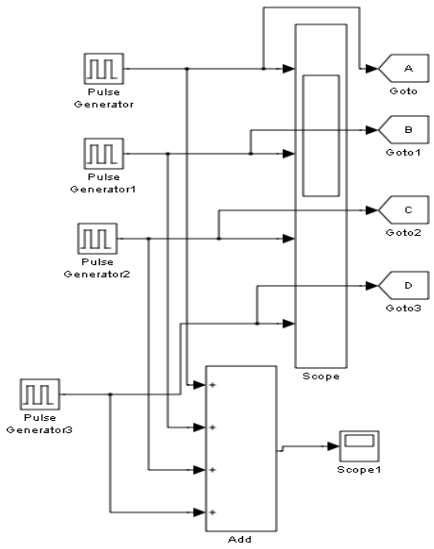

Figure 4: Switching model

5. Simulink Results

The results of the matlab simulink model was evaluated on 340V_{L-L} voltage where the C1,C2 and C3 are 2.2µF, L1 , L2 and L3 are 89µH.D1-D6 taking the simple ratings and the diodes D7 and D8 having high snubber value.

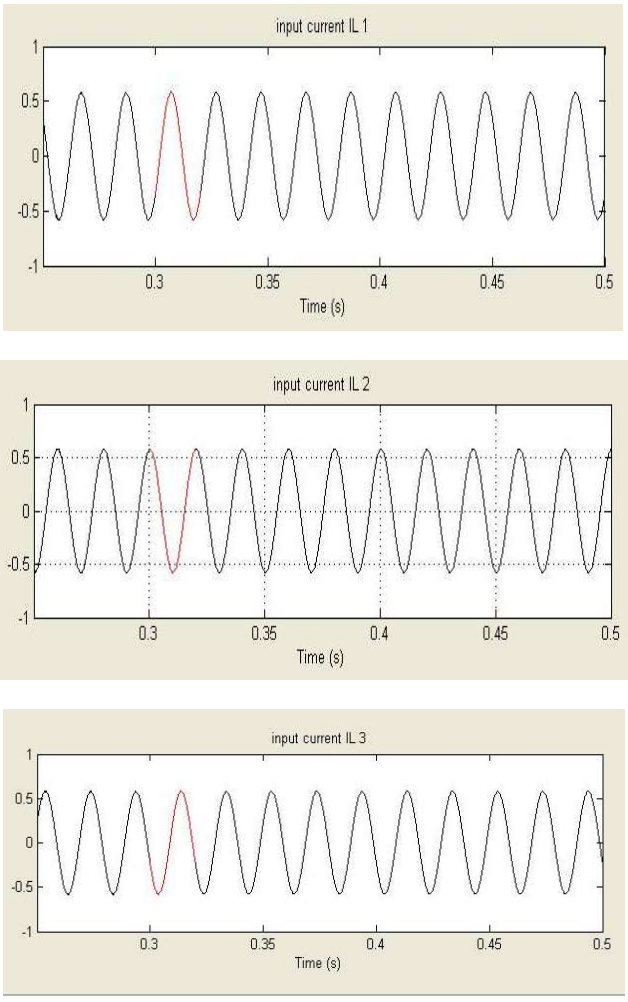

Figure 5: Input current waveforms at full load 340V_{L-L}

Figure-5 show the input current I_1, I_2, and I_3 waveforms of simulink result in scope at full power at 340V_{L-L} voltage.

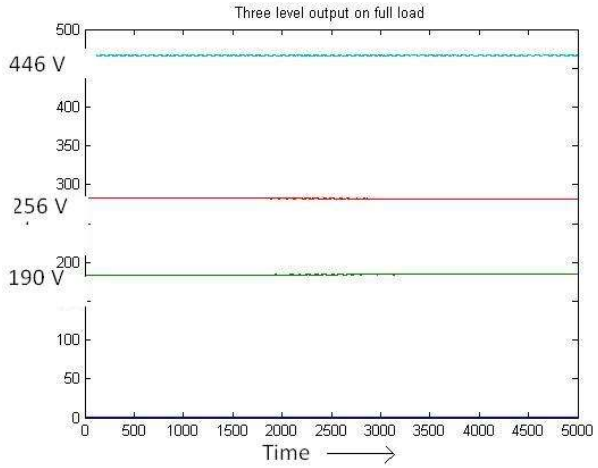

Figure 6: Measured DC out put at 340V_{L-L} input voltage.

Figure-6 shows the output power at full load in voltage 340$V_{L-L.}$ having 96% of efficiency . Figure shows the measured three level input voltage change by corresponding output voltage.

Figure 7 the three phase Input current (I_a , I_b ,and I_c) THD of the input current achieved less then 3% total harmonics reduction level by the SIMULINK modal shows by figure.

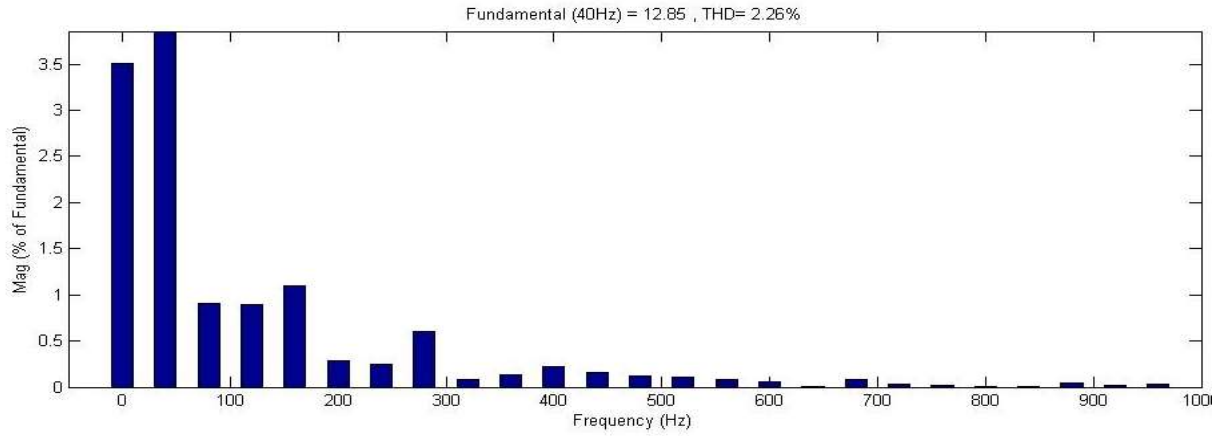

Figure 7: THD of the Input current

6. Conclusion

In this paper presented Analysis of Zero Voltage Switching, Power Factor Correction for four switches Three Phase Three Level Boost Rectifier using four switch (PWM) operation simulink modal. Voltage across the each switch measured one half of its value was clamped with output voltage. By SIMULINK results achieved less than 5% input current total harmonic distortion over the given input and achieved above 10-30% load. The total performance and assumption done by MATLAB new version at 340 line to line voltage. Achieved 94% efficiency with full load.

References

[1] J.R. Pinheiro and I.Barbi,"The Three Level ZVS-PWM dc-dc converters ,"IEEE Transaction on Power Electronics .Vol8.No.4.pp.486-492,Oct. 1993
[2] P Barbosa, F.canales and F.C.Lee "Analysis an evaluation of the Two Switch Three Level Boost Rectifier,"IEEE Power Electronics specialists' conf. (PESE) record, 2001, pp.1159-1164.
[3] M.H. RASHID POWER ELECTRONICS "ZERO VOLTAGE SWITCHING"
[4] Y.Jang and M.M. Jovanovic ,"The Taipei Rectifier –a new three phase two switch zvs pfc dcm boost rectifier "IEEE Transaction on Power Electronics Vol.28,No.2.pp.686-694,feb 2013

Author Profile

Arpit Panchratan received the B.E in Electronics & Instrumentation from TRUBA Institute Bhopal and M.E. degree in Power Electronics (Electrical Engineering) from Samrat Ashok Technological Institute vidisha (Since in 1960) in 2014,respectively.

Shobhit Jain received the B.E in Electronics & Communication from ACROPOLIS Institute Bhopal and M.E. degree in Power Electronics (Electrical Engineering) from Samrat Ashok Technological Institute vidisha (Since in 1960) in 2014, respectively.