

# 6-Bit Flash ADC for High speed Applications

N. Bharat Kumar Reddy<sup>1</sup>, Sri D. Sharath Babu Rao<sup>2</sup>

<sup>1</sup>Student of M.Tech in VLSI & EMBEDDED Systems, Electronics and Communication Engineering, GPREC (Autonomous), KURNOOL, JNTU-A, Andhra Pradesh, India

<sup>2</sup>Assistant Professor of Electronics and Communication Engineering, GPREC (Autonomous), KURNOOL, JNTU-A, Andhra Pradesh, India

**Abstract:** This paper shows the implementation of a 6-bit Flash Analog to Digital Converter in 130-nm technology CMOS logic functions at 2.5-GSamples/s, used in most of DSP-based receiver. The FLASH ADC is equipped by variable gain amplifier (VGA), track-and-hold (T/H) circuit, a comparator array consist of 63 comparators, D Flip-Flop's. A multiplexer logic is compared with the decoder using Full Adders in Wallace tree structure, with respect to hardware, critical path and power consumption. The Multiplexer logic is used to convert the 63-Bit Thermometer code into 6-Bit Binary code. Also integrated a on chip micro controller calibration, is used to monitor and compensate the nominal nonlinearity of the fine VGA and the resistor ladder. The ADC with 400mV of full scale voltage consumes 15-30 m W of power approximately from a 0.9V supply.

**Keywords:** 10G Ethernet, Digitally programmable resistor array, A/D conversion, Metastability errors, Wallace tree decoder; Multiplexer based decoder, Short critical path.

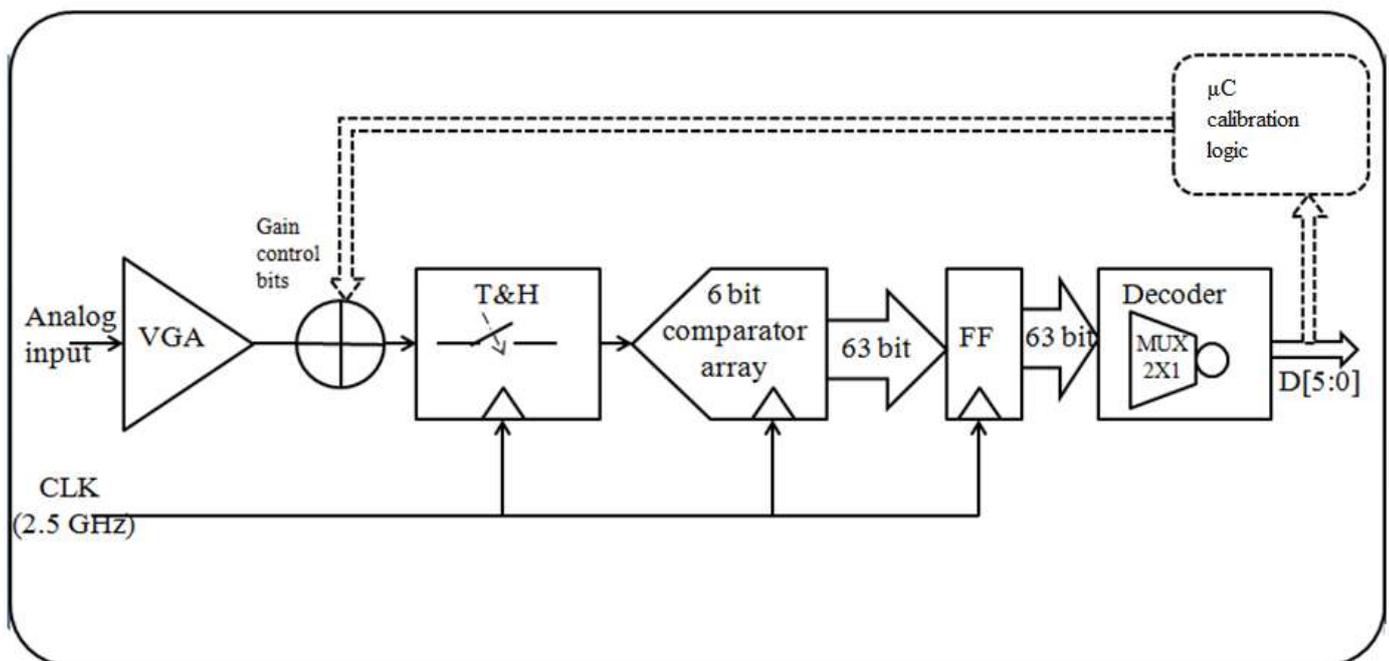


Figure 1: Top level plan of Flash ADC

## 1. Introduction

Since most of the physical signals are analog (i.e. continuous in both time and amplitude) in nature. In order to store or process those analog signals it is needed to be convert them into digital domain, in which the memorizing and processing is comfort to perform. The utilization of 10G Ethernet is tremendously increased to satisfy the demand for higher bandwidth.

Because of complications like physical media diversity, as well as the channel impairments of the fibres at 10.3 Gbps, the use of configurable DSP-based receivers that can be designed to meet the performance requirements of globalized standards of 10GE. ADC is the key functional element for such receiver which digitizes the incoming data. Converting at the standard data rate, the ADC has to provide optimal

resolution bandwidth under minimal power budget and area constraints.

This paper depicts a 2.5-GS/s, 6-bit Flash A-to-D Converter, which could be used in 4 way time interleaved parallel architecture of ADC for 10GE functionalities. The Flash architecture facilitates superior flexibility, minor latency, and lower predicted metastability error rate than remaining high-speed low-to-medium resolution ADCs. In addition, owing to the nature of the successive bit decoding, significant time-interleaving might be obligatory to ensure a better metastability error rate, which is one of typical requirement in such applications.

A complete top level block diagram of the Flash ADC is shown in Fig. 1. Implemented in 130-nm technology CMOS logic, the ADC depicted in this document is used as the core

for the 4 way interleaved analog frontend runs at 10GSamples/s for a DSP-based receiver that can be used the NRZ 10GE standards. While this paper focuses on the design and implementation of decoder for the ADC, and on comparative analysis of decoder implementation using Wallace tree adder and Multiplexer.

## 2. ADC Architecture

The on-chip micro Computer first calibrates the ADC upon receiver start-up, and then continuously compensates the non-linearities in VGA and inter-channel mismatch during the normal operation of the ADC. The ADC consists of a frontend Variable Gain Amplifier (G) which provides fine control of gain. Each instance of G drives a Track and Hold (T/H) circuitry that is clocked by a 2.5-GHz clock. The comparator array of 63 comparators is fed by the sampled analog signal and reference signals which are generated by a resistor ladder network with 400m V of full-scale voltage.

To prevent Metastability-related error propagation, the thermometer code goes through a sequence of flip-flops before arriving at the decoder inputs. Together with the comparator and the SR latch, this guarantees metastability error rate betterment. A multiplexer logic then converts the Metastability-hardened thermometer code into binary. Finally, the output is retimed to a single clock phase.

## 3. Circuit Implementation

### 3.1 Variable Gain Amplifier

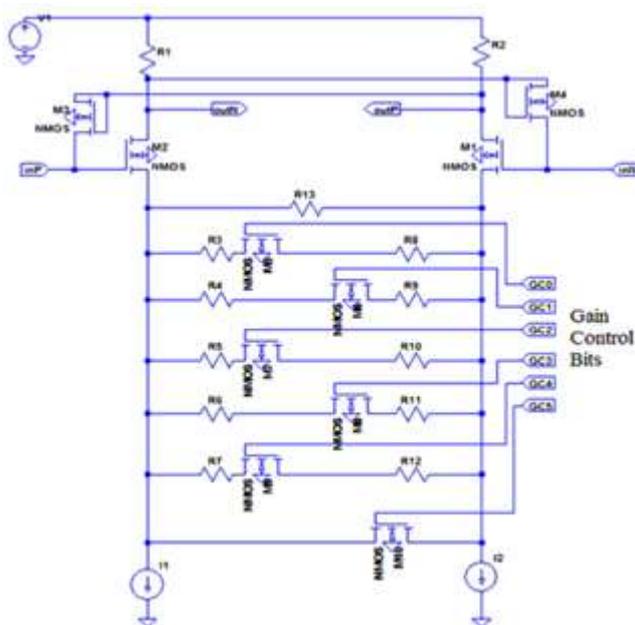


Figure 2: Source-degenerated variable gain amplifier (G)

The VGA adjust the input signal to provide an optimal swing of nearly 400 mV differential peak-to-peak (dpp) to the T/H. The amplifier G provides fine gain control at optimal bandwidth. Fig. 2 shows the design of the source-degenerated differential amplifier equipped with variable gain control. The purpose of source degeneration is to improve the linearity of the amplification. For the amplifier, source degeneration is implemented via a digitally

programmable resistor array that allows the gain to be varied. Over all transconductance of the source degenerative common drain amplifier is  $G_m = g_m / (1 + g_m * R_s)$ . Where  $R_s$  is equivalent resistance of resistor network at source. The programming of resistor array is continuously done by micro computer calibration.

The M3 and M4 helps in extending bandwidth during normal operation also disconnecting the input signal from the load during calibration. Charge feedback via gate-to-drain overlap capacitance of M1 and M2 can disturb circuit functionality. Cross-coupled devices M3 and M4 perform first-order cancellation of this effect.

### 3.2 Dynamic Comparator

The comparator array consists of 63 active comparators and a resistor ladder. The ladder range is 400 mVdpp, resulting in a nominal LSB value of 6.25 mV. To achieve a power-efficient design, the dynamic comparators in this ADC operate without any pre-amplifiers. To save power in the clock tree, each comparator uses a local clock buffer that can be disabled during individual comparator power down.

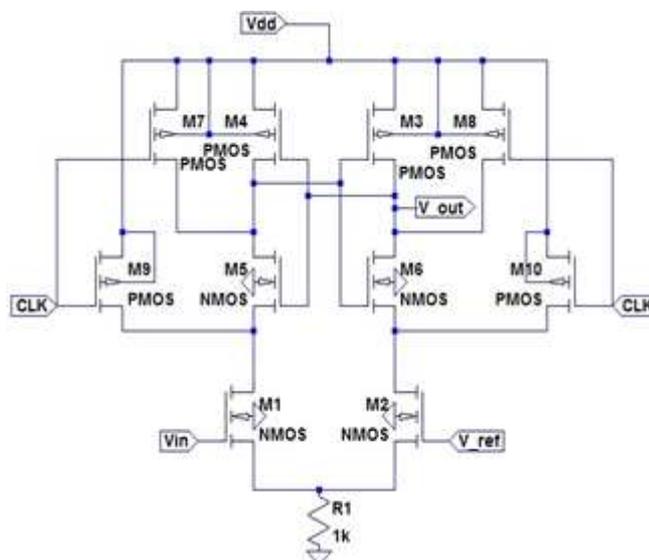


Figure 3: Schematic of Dynamic comparator

Fig. 3 shows the design of the comparator, which is based on a dynamic-sense amplifier latch incorporating several modifications. The comparator compares the sampled input signal with the reference generated by the resistor ladder. A voltage of 400 mV is provided to the resistor ladder as full-scale voltage of Flash ADC. This operation (i.e. comparing) is performed by pair M1–M2. This input device configuration accommodates the large signal range at the edges of the ladder.

The output of a comparator is HIGH if the input voltage is larger than the reference voltage at the input of the comparator, otherwise the output is inverted clock since the comparator is working in dual input and single output mode the inverted clock region will be cancelled and considered as LOW.

3.3 Decoders

3.3.1. The Wallace tree decoder

The output of a thermometer-to-binary decoder is the summation of digital ones on the input, represented in, e.g., gray or binary code. This will be chosen when using a ones counter as a decoder and gives the similar result as the bit swapping technique.

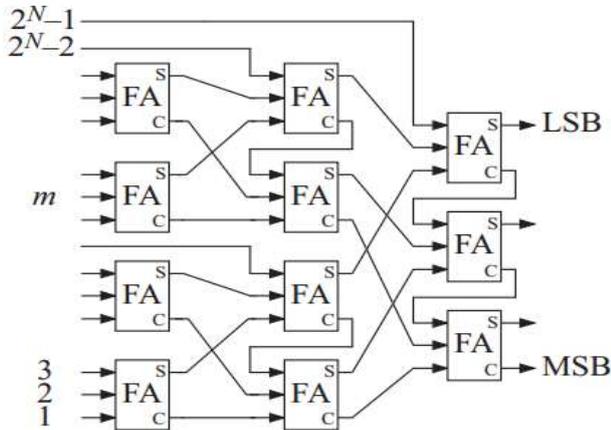


Figure 4: Wallace tree decoder for a 4-bit flash ADC

However, the bit swapping technique also needed a thermometer decoder, since the output is a bubble error rectified thermometer code. Using the ones-counter the output is the decoded binary code and it also performs global bubble error suppression. One more advantage of the approach of using the ones-counter as decoder is that based on the speed constraint on the ADC a suitable ones-counter topology may be selected by a speed for power trade-off. For high-speed applications the Wallace tree topology is shown in Fig. 4.

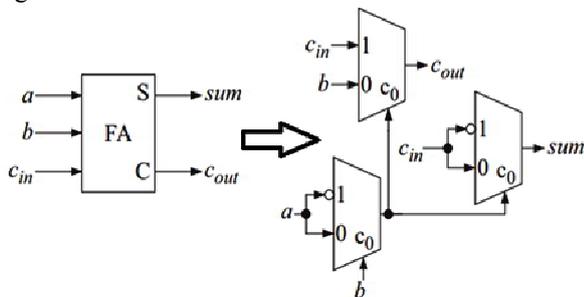


Figure 5: Realization of Full Adder using 2:1 Multiplexers

A full adder can be constructed from three 2:1 multiplexers with two multiplexers in the critical path as described in the fig. 5. The reason behind this realization is to simplify the comparative study of Wallace tree decoder with MUX based decoder. Hence, for N bit decoder, the number of 2:1 multiplexers needed ( $Y_N$ ) and the critical path ( $C_N$ ) for the Wallace tree decoder are formulated as:

$$Y_N = 3 * \left[ \sum_{i=1}^N (i - 1) \cdot 2^{(N-i)} \right] \quad (1)$$

$$C_N = 2 * [2N - 3] \text{ for } N > 1 \quad (2)$$

$$C_N = 2 * [N] \text{ for } N = 1$$

The units of  $C_N$  is equal to the propagation delay of a 2-input XOR gate ( $t_{XOR}$ ) which is similar to the propagation delay of a 2:1 multiplexer ( $t_{MUX}$ ).

3.3.2 The Multiplexer Based decoder

This subdivision will first illustrate the idea behind the presented multiplexer based decoder and second describe how it could be generalized. For an N-bit flash ADC the most significant bit (MSB) of the binary output is high if more than half of the outputs in the thermometer scale are logic one. Hence is the same as the thermometer output at  $2^{N-1}$  level. To find the value of the second most significant bit (MSB-1) the original thermometer scale is bifurcated into partial thermometer scales, separated by the output at  $2^{N-1}$  level as depicted as the flow diagram in Fig. 6.

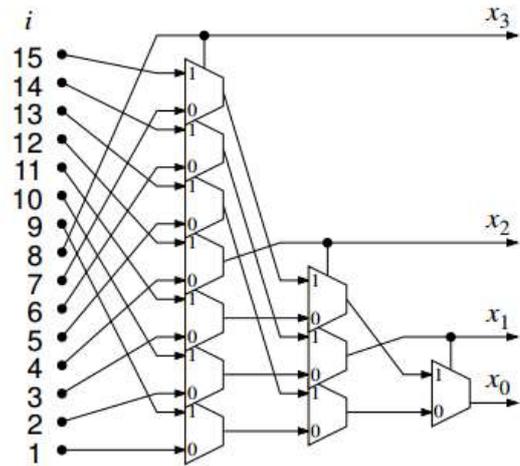


Figure 6: Implementation of 4 bit Multiplexer based decoder

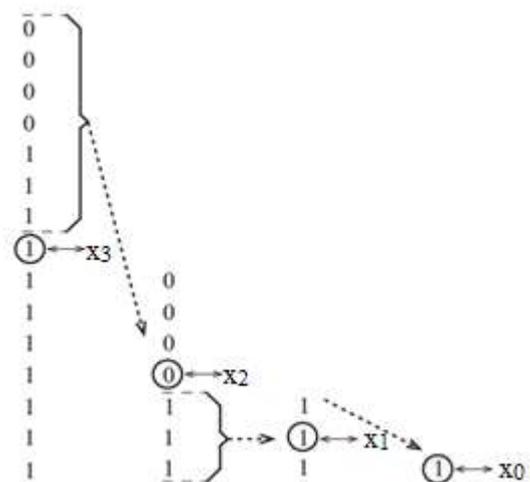


Figure 7: Flow of Multiplexer based decoding

The partial thermometer scale to decode is chosen by a set of 2:1 multiplexers, where the earlier decoded binary output is fed as the control input of the multiplexers. MSB-1 is then determined from the chosen partial thermometer scale in the identical fashion as was found from the full thermometer scale. The selected scale is thereby the scale that includes the information about MSB-1, i.e. the lower partial thermometer scale if the output at level is logic zero otherwise the upper partial thermometer scale is used.

This conversion is continued recursively until only one 2:1 multiplexer remains. Its output is the least significant bit (LSB) of the binary output. The decoder scheme is illustrated by the 4-bit multiplexer based decoder in Fig. 5. Due to the

regular architecture of this decoder it can easily be developed to function in a system of higher resolution than 4 bits, which is explained further below.

The regular structure should also be of profitable in the physical layout. The outputs  $x_q$  of the decoder is the equivalent binary value of the thermometer code, where  $q=0,1,2,\dots,N-1$ . The column  $q=1$  is the first multiplexer column. Hence the output  $i_q = 2^{N-q-1}$  is connected to the control inputs of the multiplexers in  $q+1$  column. This is also the output of the  $x_{N-q-1}$  decoder, where  $x_{N-1}$  is the most significant bit of the binary output. The output of the multiplexer in column  $q=N-1$  is the least significant bit of the binary output, i.e.  $x_0$ .

In general, for an  $N$ -bit flash ADC the thermometer output has  $2^N - 1$  levels ( $i_{q=0}$ ). The thermometer output  $i_q = 0$  or multiplexer output  $i_{q>0}$  is coupled to the '0' ( $i_q < 2^{N-q-1}$ ) or '1' ( $i_q > 2^{N-q-1}$ ) input of the multiplexer of level  $i_q \text{ modulo } 2^{N-q-1}$  and column  $q+1$ , where  $i_q = 1,2,3,\dots, 2^{N-q}-1$ . Hence for the presented decoder required number of 2:1 multiplexers  $Y_N$  and the critical path  $C_N$  in units of  $t_{MUX}$  can be formulated as:

$$Y_N = \sum_{i=1}^{N-1} [2^{(N-i)} - 1] \quad (3)$$

$$C_N = N - 1 \quad (4)$$

#### 4. Comparison of the Approaches

The Multiplexer based decoder seems to have capable and beneficial properties in terms of amount of hardware and critical path. If instead a ones-counter is used as the decoder it includes speed versus power trade-off not only by directly trading power for speed, but also in terms of choosing an appropriate ones counter/adder topology. A comparison of the performance between the Wallace tree decoder and the Mux based decoder is given in Table 1. The performance is considered in terms of amount of hardware and length of the critical path.

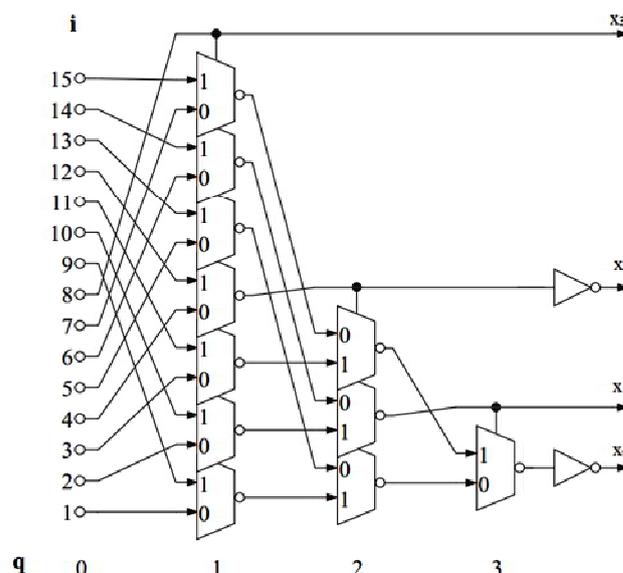
**Table 1:** Performance comparison of 6 bit flash ADC

Type of Decoder	N.of MUX's	Critical path
Wallace tree Decoder	171	18 $t_{MUX}$
MUX based Decoder	57	5 $t_{MUX}$

As seen in Table 1, the hardware is significantly reduced when using the MUX based decoder. For the MUX based decoder, the number of multiplexers is reduced by more than 60% compared to the Wallace tree decoder. This is likely to translate to a power saving. Table 1 also indicates that the suggested solution has the potential of being faster than the Wallace tree decoder, since its critical path is shorter.

#### 5. Improvizations

Since the MUXs are based on transmission gates a slow decoder circuit would be obtained if the MUXs are unbuffered. To improve the maximum operation frequency of the decoder an inverter is introduced as an output buffer in the MUXs. A single inverter is introduced to have a low output-buffer propagation delay. The use of a single inverter is only lead to a minor modification of the original MUX-based decoder circuit.



**Figure 8:** Buffered MUX based decoder for 4 bit ADC

Since the 2:1 MUXs used in the decoder are buffered with one inverter on their output, the decoder topology is slightly changed compared to the topology shown in Fig.6 for a resolution of four bits. The modified topology is shown in Fig. 8 for the same resolution. As seen in that figure, a number of inverters are added to the decoder outputs with zero or even indices. In addition, the MUX inputs in the even columns are interchanged, i.e., the input signals coming from upper half of previous stage are connected to the "0"-input instead of the "1"-input, of MUX and vice versa. Compare the MUXs in column one and two in Fig 8. And it is clear that a delay of 4 times propagation delay of inverter ( $t_{inv}$ ) is added to the critical path. Hence the critical path of  $N$  bit Buffered MUX based decoder will become:

$$C_N = [(N-1) * t_{MUX}] + [N * t_{inv}] \quad (5)$$

The critical path is one of the main factors that limit the maximum operating frequency  $f_{max}$  of the decoder. By inserting D-Flip Flops in feed forward cutest edges of decoder topology, the critical path will be further shortened. With the additional cost of Flip Flops, code conversion will be speeded up as:

$$f_{max} = 1 / C_N \quad (6)$$

where  $C_N = (t_{MUX} + t_{inv})$  is the critical path delay of the buffered Mux based decoder including the D Flip Flops at appropriate places. By this concept the decoder can convert thermometer code into binary at extremely high rate.

**Table 2:** Flash ADC (6 bit) performance summary.

Technology	130 nm
Supply Voltage	0.9V
Sampling frequency	2.5 GHz
Nominal resolution	0.1587
Nominal LSB size	6.25mV
Full scale voltage	400mV
Analog input frequency	200MHz
Power consumption	15-30 mW

As seen in Table 2, the Mux based decoder with buffering and proper reduction of critical path, will make the ADC as more economical

## 6. Conclusion

This work presents a 2.5-GS/s, 6-bit, 15- 30 mW, Flash ADC for a universal 10GE DSP-based receiver. Our study demonstrates that the multiplexer based decoder is an attractive approach for designing thermometer-to-binary decoder. The amount of hardware and area consumption is less than compared to the other existing decoders and the critical path is shorter. This should make it possible to design for lower power applications. In addition, it has a more regular structure than the other decoders, which is an advantage when doing the layout.

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