after it exceeds higher than half of given voltage i.e Vdd/2 but Schmitt trigger can be designed to have a threshold voltage less than Vdd/2 and thus can be made to respond faster and by this the delay can be reduced in cost of area.

Let us consider an input signal by a fast rising edge given to the input of the circuit. Ideally, the signal at the end of the circuit should be in the same shape but the delay produced by the interconnect due to parasitic capacitances leads to far-end signal being obtained only after certain time has been elapsed. This value can be high i.e a few nanoseconds depending on the values of resistance and parasitic capacitance. While a buffer is repeatedly used to restore the original signal and its output is obtained only after the input voltage signal crosses Vdd/2. But the Schmitt trigger can be designed to have a lower threshold voltage so that it can respond faster than a buffer. It compares the response of a buffer and a Schmitt trigger to a slowly varying input. The buffer is designed with 2 CMOS inverters placed back to back (figure 3). Buffer is designed with minimal lambda parameters for different technologies by keeping Wp = 2Wn to ensure equal rise and fall time of the signal. Schmitt trigger used in this approach has 4 MOS transistors which are comparable is size with the transistors used in buffer.

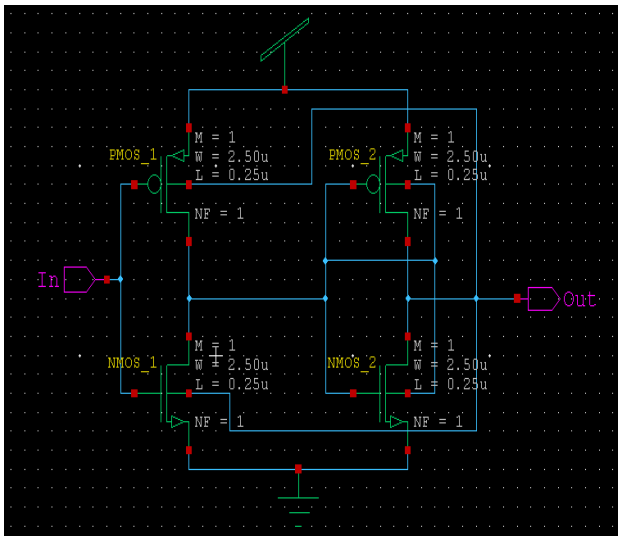


Figure 4: CMOS Schmitt trigger circuit using 4 MOS transistors.

All these factors are not in support of buffer insertion for interconnect modeling. Thus a major Breakthrough is needed to handle interconnects. Hence keeping in mind of all the problems being faced and to be coming with buffer insertion, in this thesis, an alternate to buffer is proposed and tried analyzing the results. In the new approach buffer is replaced by Schmitt trigger and analyzed all the above mentioned factor.

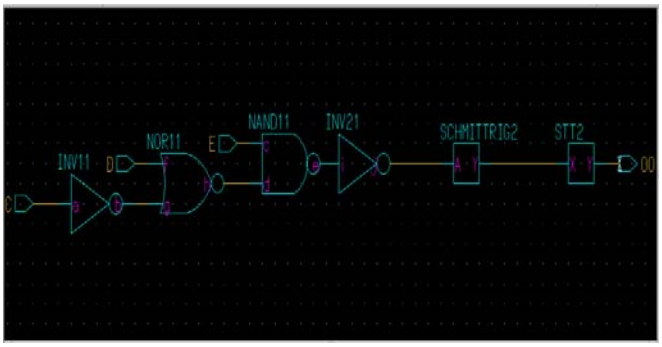


Figure 5: Sized logic with Schmitt trigger circuit

3.1 Delay Analysis

The main advantage of using Schmitt trigger in place of buffer is that we can control threshold voltage limits. Let us consider an input signal with a very slow rise time given to the input end of the interconnect. Ideally the signal obtained at the output should be in the same shape but the interconnect delay/RC delay (the delay produced by parasitic) will play a very important role in deep submicron technologies so the output signal gets delayed due to the parasitic capacitance and inductance and reaches to high voltage after a certain amount of time. This delay may be high i.e. in few nanoseconds when the values of resistance and parasitic capacitance are high. By this we get a delayed as well as a deformed output waveform. To rectify this deformed waveform we insert buffer at the output end of the interconnect. Now until the delayed signal reaches higher than Vdd/2 the output of the buffer will remain low i.e. at zero volts and whenever it reaches to a value less than Vdd/2 it will directly go to high within the switching time of a buffer as shown in figure1. So efficiently we saved half of the RC product in terms of delay.

In this we considered the interconnect as a linear structure ignoring the tree structure and also all interconnects are treated as RC models. Firstly the critical repeater length for each technology is calculated. Here repeater length is the minimum distance beyond which inserting an optimal-sized buffer makes the interconnect delay smaller than the corresponding unrepeated wire.

4. Simulation Results and Comparisons

The existing and proposed methods are performed on four different process parameters Viz. 180nm, 90nm, 65nm and 45nm using H-spice simulator at 27ºc. The supply voltages to be considered for the four process parameters (technologies) along with the threshold voltages for NMOS and PMOS in the respective technologies are as shown in Table 4.1.

Table **4.1:** Supply Voltages and Threshold Voltage values

Technology	*180nm*	*90nm*	*65nm*	*45nm*
Supply Voltage	1.8V	1.2V	1.1V	1V
NMOS V_T (V)	0.3999	0.2607	0.22	0.1711
PMOS V_T (V)	-0.42	-0.303	-0.22	-0.1156

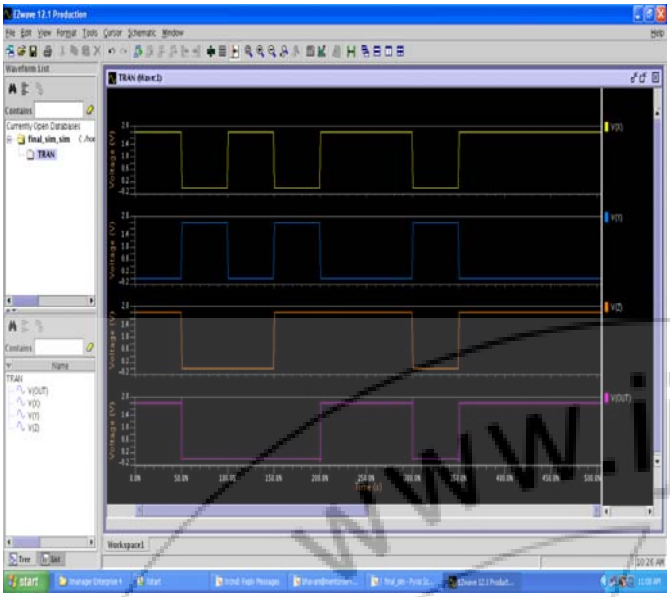


Figure 6: Simulation waveforms Schmitt trigger technique in logical sizing

4.1 Minimum Sized Logic Repeater Insertion, Cascaded Sized Logic With Uniform Repeater Insertion And Sized Logic With Non-Uniform Repeater Insertion

The four criteria are applied to a different CMOS technology (i.e 45nm, 65nm, 90nm, 180nm) to determine the optimum solution for different line lengths. All the above three methods delay and power are compared with different technologies. The optimum solution for each criterion is listed in Table 4.2, 4.3, 4.4 a clock signal with a 2ns transition.

A. Delay

Table4.2: Delay comparison with different methods

Technology (nm)	DELAY(Ps)		
	Minimum Sized Logic	Sized Logic	Non-Uniform Repeater
180	126.75	114.95	116.85
90	147	117.45	120.75
65	168.05	128.94	149.6
45	233.4	203.50	229.93

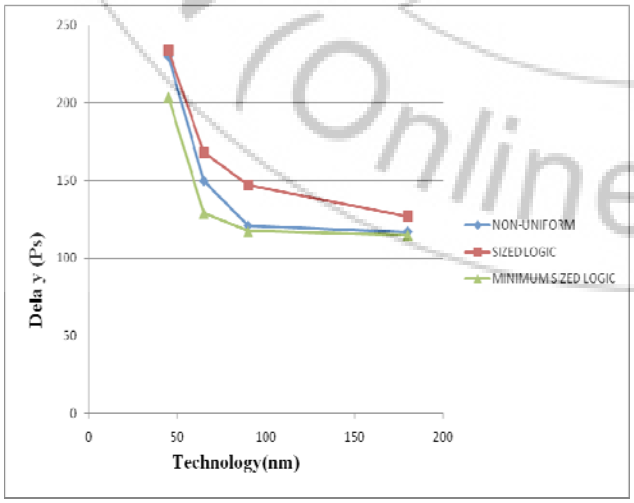


Figure 7: Delay vs Tecnology for sized logics with Buffer

B. Average Power

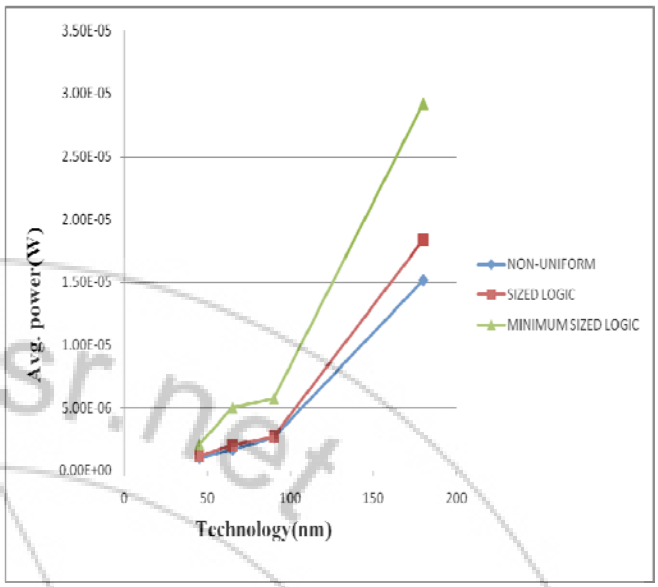


Figure 8: Avg power vs Technology for sized logics with buffer

Table 4.3: Delay comparison with different methods

Technology (nm)	Average Power(W)		
	Minimum Sized Logic	Sized Logic	Non-Uniform Repeater
180	2.9185E-05	1.8376E-05	1.5164E-05
90	5.7553E-06	2.7198E-06	2.6849E-06
65	5.022E-06	2.0900E-06	1.6804E-06
45	2.1431E-06	1.1458E-06	1.0515E-06

4.2 Power Delay Product(PDP)

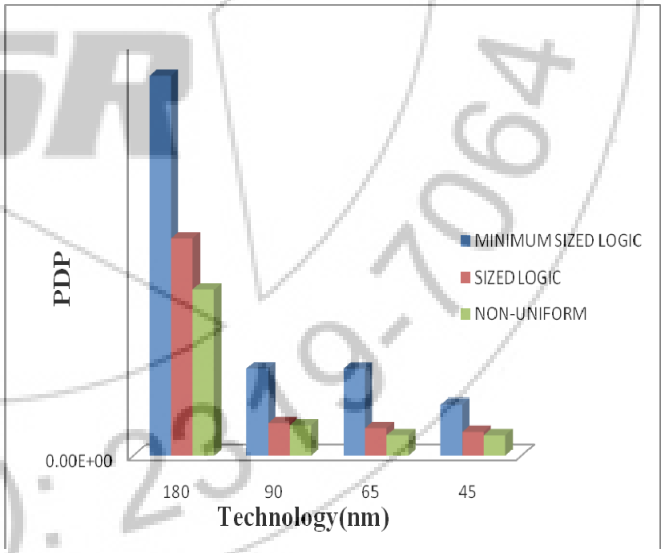


Figure 9: Power delay product vs Tecnology for sized logics with buffer

Table 4.4: PDP with different methods

Technology (nm)	*PDP*		
	Minimum Sized Logic	*Sized Logic*	*Non-Uniform Repeater*
180	3.699E-15	2.1123E-15	1.7719E-15
90	8.46E-16	3.1944E-16	3.2688E-16
65	8.439E-16	2.694E-16	2.5138E-16
45	5.001E-16	2.331E-16	2.4177E-16

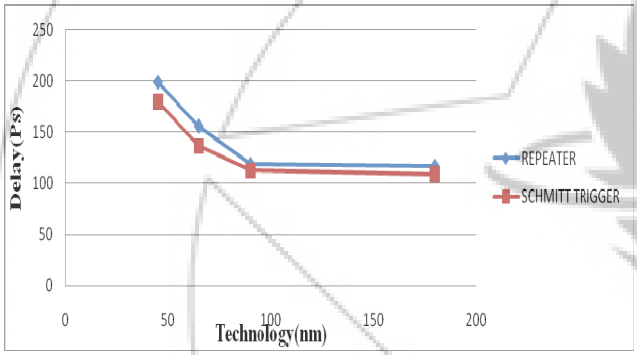
4.2 Comparison Of Sized Logic With Non-Uniform Repeater Insertion And Sized Logic With Schmitt Trigger Insertion Technique

The four criteria are applied to a different CMOS technology (i.e 45nm, 65nm, 90nm, 180nm) to determine the optimum solution for different line lengths. Comparison of non-uniform repeater insertion and Schmitt trigger insertion technique. The optimum solution for each criterion is listed in Table 4.5 a clock signal with a 2ns transition.

A. Delay

Table 4.5 Delay comparison between sized logics with buffer and Schmitt trigger

Technology (nm)	Delay(Ps)		Percentage Decrease In Delay (%)
	Repeater	Schmitt Trigger	
180	116.65	108.79	6.738
90	118.6	112.55	5.1011
65	155.8	136.4	12.45
45	198.55	179.55	9.5693



Figur10: Delay vs Technology for sized logics with buffer and Schmitt trigger

B. Average Power

Buffer consumes 5.09% more power per cycle than the proposed Schmitt trigger technique.

Table 4.6: Average power comparison between sized logics with buffer and Schmitt trigger

Technology (nm)	*Average Power(W)*		*Percentage Decrease In Average Power %*
	Repeater	*Schmitt Trigger*	
180	2.1127E-05	2.0854E-05	1.292 %
90	4.0455E-06	4.0102E-06	0.872 %
65	2.5667E-06	2.4883E-06	3.054 %
45	1.2828E-06	1.2175E-06	5.090 %

5. Conclusions

The delay introduced in interconnect is more when compared to the gate delay in DSM. In this we used the sized logic with buffer and Schmitt trigger. The proposed Schmitt trigger (depending on Sized logic) is used in place of buffers in between the interconnects for further reduction of delay and power. A four MOS transistor Schmitt trigger is implemented for this analysis. The simulation results shows that proposed technique exhibit less Delay and power when compared to the existing techniques. It is also proved here that the proposed technique works even at nanometer designs.

- Programmable dual threshold property of Schmitt trigger allows the designer to control lower thresholds for fast signal switching time.
- Lower thresholds are advantageous at the time of switching too, as it would not allow all the transistors to be in active or saturation mode.
- Noise immunity of Schmitt trigger is more than buffer because of larger band gap.

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