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A Review on Reversible Logic Gate Multipliers

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Abstract: ***The efficient low power and small area multipliers in the digital circuits for the emerging technology are of more interest these days. Hence designing of the multipliers with the factors of low power, area and delay is dominant. For this purpose the reversible logic multipliers are designed in advantage over that of conventional multipliers. This paper describes the comparative analysis of different reversible logic gate multipliers in terms of number gates, number of garbage inputs, garbage outputs and quantum cost. Each of the multipliers operation can be generalized for NxN bit multiplication of their advantages.***

Keywords: multipliers, reversible logic, garbage output, garbage input, quantum cost

1. Introduction

The heavily used algorithm in many of the computational unit is multiplication. The multiplication unit determines the performance of the system. Since the power consumption and processing is slow for multiplication in any computational unit, it is necessary to have a multiplier that consumes low area, power and delay. Recently the new methods of constructing multiplier using reversible gates are in existence. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one to one correspondence between its input and output assignments. In reversible logic gate circuits the number of input and output are identical.

The following are the design constraints for reversible logic circuit:

- Use minimum number of reversible gates.
- Should not allow fan-outs.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.
- Minimization of quantum cost.

Multiplier unit with reversible gate are gaining significant attention in recent years, which is also the best way out for reducing power consumption .The reversible logic appers to be promising in future low power application design.

2. Basic Multiplier Operation

A general 4X4 multiplier operation is as shown in the fig (1). It consists of two steps a) generation of partial products b) addition of partial products. It consists of sixteen partial products of the form XiYi where i varies from 0 to 3.

				x_3	x_2	x_1	x_0
			x	y_3	y_2	yx_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Figure 1: Basic multiplier operation

For the generation of the partial product we use peres gate, because of its low hardware complexity. The partial product generation is as shown in the fig 2.

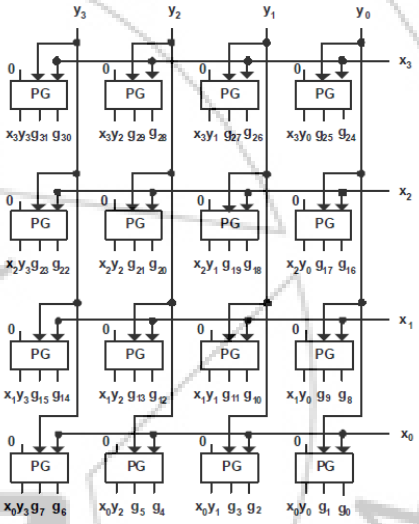

Figure 2: Generation of partial products using Peres gate

3. Comparison of Different Partial Product Addition Architecture

Once the partial product is being generated the step two, addition of the partial product is carried out using different ways. A brief description of the addition of the partial products is as given below.

A) 4X4 reversible multiplier using Peres Gate and HNG gates.

The architecture proposed in this paper contains 8 reversible HNG full adder in addition 4 reversible PG half adders as shown in the fig 3. One of the main factors of this circuit is less hardware complexity [1].

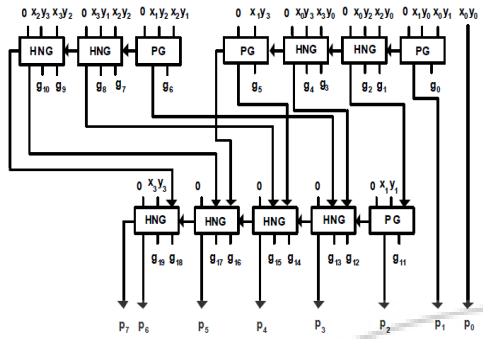

Figure 3: 4x4 reversible multiplier using peres gate and HNG gates.

B) 4X4 reversible multiplier using Peres Gate and DPG gates.

Here the partial product generation is done using RAM and Peres gate [2] as shown in the fig4. Addition of partial product in this architecture requires 3 input adder using DPG with one constant input and two garbage output and half adder using PG with one constant input and one garbage output as shown in the fig4.This reversible multiplier circuit uses 8 DPG gates, 4 PG gates, 16 PG gates for partial product generation and 4 RAM gate for fan out creation.

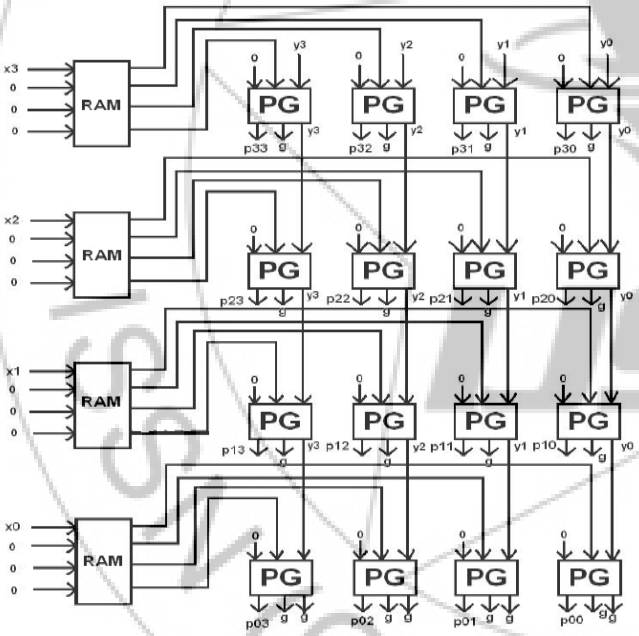

Figure 4: reversible partial product generator using PG and RAM gates.

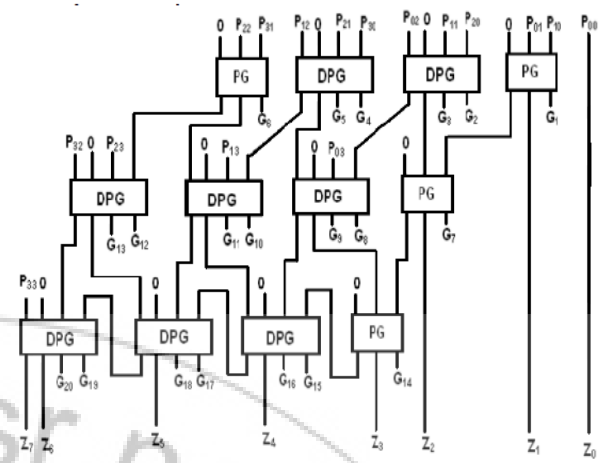

Figure 5: reversible addition circuit

C) 4X4 reversible multiplier using Peres Gate and Full adder.

In this paper the proposed architecture describes the addition of partial products using 9 full adder and 3 Peres gates as reversible half adder [3] as shown in the fig6.

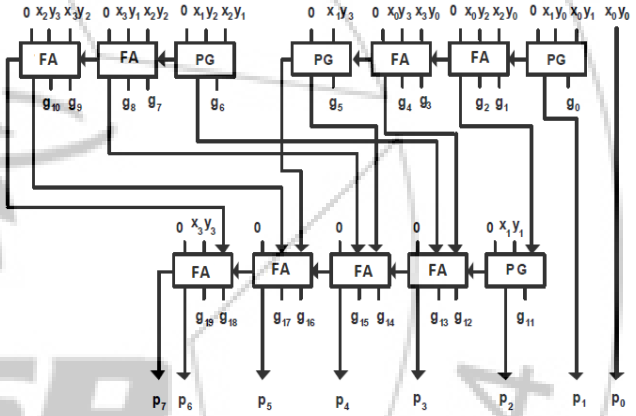

Figure 6: 4x4 reversible multiplier using Peres gate and Full adder

D) 4X4 reversible multiplier using Peres Gate and MHNG gates.

Addition of partial products requires 8 full adders and 4 half adders. Reversible MHNG gate and Peres gate can be used as a full adder and half adder respectively. The multiplier is as shown in fig7.

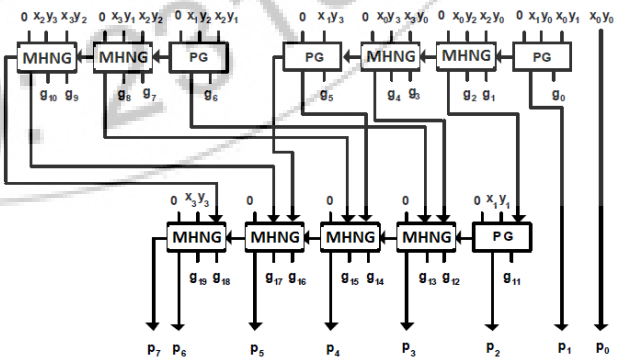

Figure 7: 4x4 reversible multiplier using Peres gate and MHNG gate

Table1: Comparison of existing multipliers

Partial product adder	*No of gates*	*Garbage inputs*	*Garbage output*	*Quantum cost*
PG and HNG	28	28	52	80a+36ß
PG and DPG	32	40	40	140
PG and full adder	28	20	20	80
PG and MHNG	28	28	22	80a+36ß

4. Conclusion

In this paper the different reversible multiplier circuits are studied. The multiplier using PG and full adder very efficient since the garbage input and outputs are reduced. Further these multipliers can be generalized for large number multiplication in different applications.

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