

Design of Loop Filter Using CMOS

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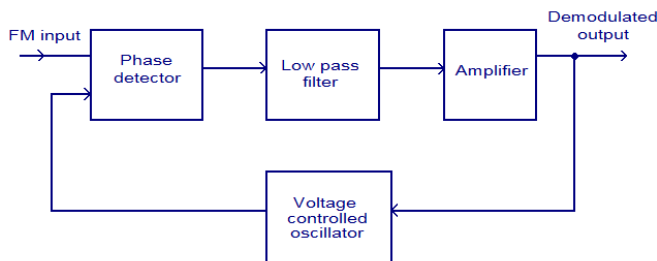
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Abstract: An important task for a digital communications receiver is to remove any frequency/phase offsets that might exist between the transmitter and receiver oscillators. The use of a Phase Locked Loop enables the receiver to adaptively track and remove frequency/phase offsets. The pll consists of loop filter, VCO and amplifier. The paper describes the designing of this loop filter using CMOS. The use of this element reduces cost drastically and has a good response. An experiment was conducted through this component which provided better result. The main advantage of designing low pass filter by CMOS is that it offers improvements in design simplicity and programmability when compared to op-amp based structures as well as reduced component count. It has high noise immunity and low static power consumption. Hence the overall efficiency increases as well producing the desired effect.

Keywords: Loop filter, CMOS, Low Pass Filter, VCO, Gain

1. Introduction

A simple PLL FM demodulator circuit using IC XR2212 is shown here. XR2212 is a highly stable, monolithic PLL (phase locked loop) IC specifically designed for communication and control system applications. The IC has 0.01 Hz to 300 KHz frequency range, 4.5 to 20V operating voltage range, 2mV to 3Vrms dynamic range, high temperature range, TTL / CMOS compatibility and adjustable tracking range. The block diagram of a typical PLL FM demodulator circuit is shown below.



PLL FM demodulator circuit

Figure 1: PLL FM Demodulator Circuit

A PLL consists of three basic elements: a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The block diagram in Figure 1 shows how these elements are connected in order to form a PLL.

The goal of this PLL is to produce a locally generated sinusoid $y(t)$ whose instantaneous angle is equal to the instantaneous angle of the received signal $x(t)$. The following paragraphs will briefly describe these three key elements.

1.1 The Phase Detector

The purpose of the phase detector is to generate an error signal that drives the PLL. This error should be proportional to the phase difference between the signals $x(t)$ and $y(t)$.

1.2 The Loop Filter

The purpose of the loop filter is to filter the phase error signal $\varepsilon(t)$ in order to provide a better signal to the VCO.

The values of the gain parameters chosen for the loop filter control the loop bandwidth of the PLL. The size of the loop bandwidth determines the range of error signal frequencies that the loop filter will pass. The value for this bandwidth has a direct impact on the performance of the PLL. If the value of the loop bandwidth is large, the loop filter can pass a wide range of frequencies for the error signal. In contrast, a small value for the loop bandwidth will limit the amount of noise that passes through the filter. In addition to the loop bandwidth, another important design criterion for the loop filter is the order of the filter. A first-order loop filter simply multiplies the error signal by a proportional gain Kp .

A PLL with a first-order loop filter cannot track out a frequency offset. The first-order PLL will converge to a non-zero value in the presence of a frequency offset. In order for the PLL to also track out a frequency offset, a PLL with a second-order loop filter is needed.

1.3 Voltage Controlled Oscillator

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage.

1.4 Design of Loop Filter

The loop filter is basically an active low pass filter. The circuit diagram for the low pass filter is shown below. It consists of an op-amp, resistor and capacitor.

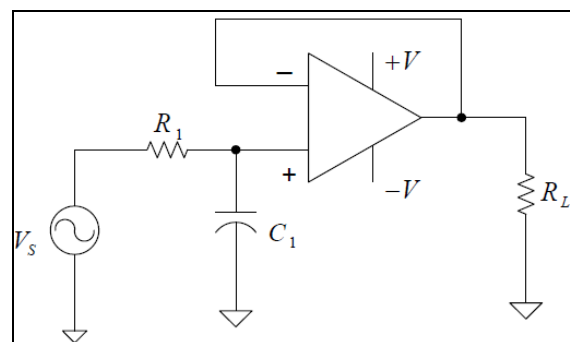


Figure 2: Low Pass Filter

A low-pass filter is a filter that passes low-frequency signals and attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design.

The **order** of the filter determines the amount of additional attenuation for frequencies higher than the cut off frequency. The break frequency, also called the turnover frequency or cutoff frequency (in hertz), is determined by the time constant:

$$f_c = 1/2\pi RC$$

or equivalently (in radians per second):

$$\omega_c = 1/RC$$

1.5 CMOS-Complementary Metal-Oxide-Semiconductor

The term 'Complementary Metal-Oxide-Semiconductor', or simply 'CMOS', refers to the device technology for designing and fabricating integrated circuits that employ logic using both n- and p-channel MOSFET's. CMOS is the other major technology utilized in manufacturing digital IC's aside from TTL, and is now widely used in microprocessors, memories, and digital ASIC's.

The input to a CMOS circuit is always to the gate of the input MOS transistor, which exhibits a very high resistance. This high gate resistance is due to the fact that the gate of a MOS transistor is isolated from its channel by an oxide layer, which is a dielectric. As such, the current flowing through a CMOS input is virtually zero, and the device is operated mainly by the voltage applied to the gate, which controls the conductivity of the device channel.

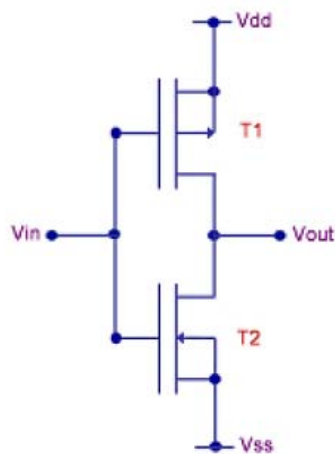


Figure 3

2. Proposed Work

The method proposed over here is the designing of low pass filter using CMOS. A first order low pass filter using CMOS is shown below-

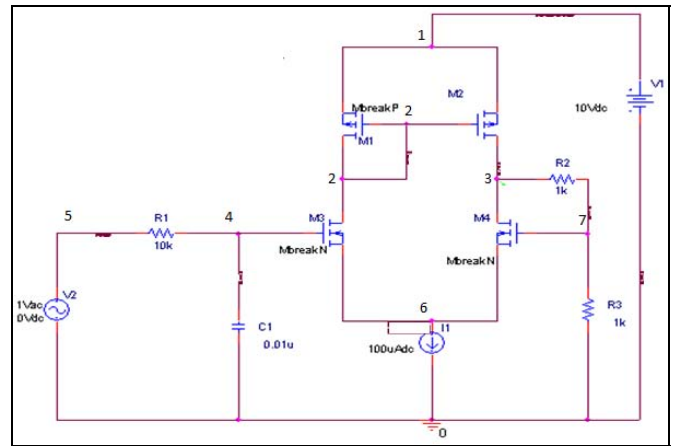


Figure 4: Magnitude plot for the 1st order filter

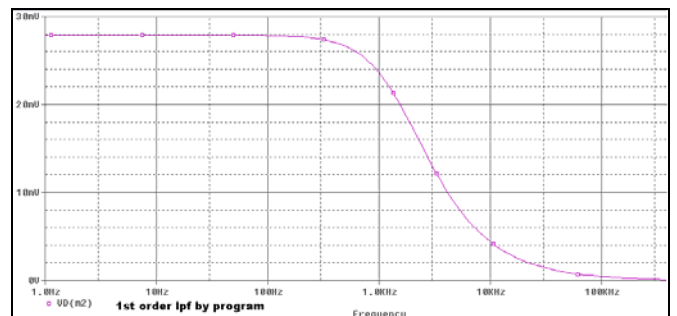


Figure 5: Magnitude plot for the 1st order filter

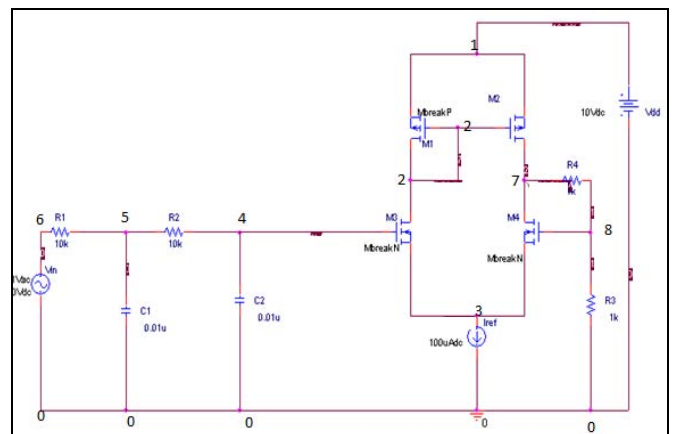


Figure 6: Second order low pass filter

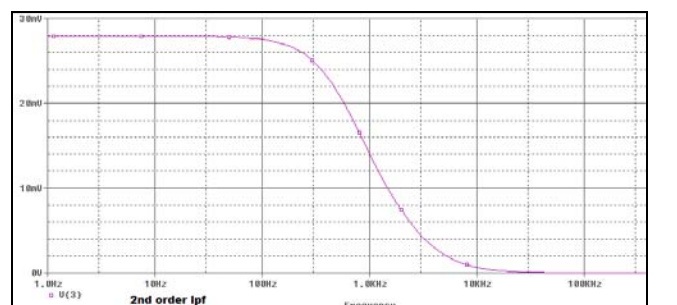


Figure 7: Magnitude plot for the 2nd order filter

3. Advantages of CMOS

1. The conventional operational amplifier (op-amp) is used as the active device in the vast majority of the active filter literature. A host of practical filter designs have evolved following this approach. It has also become apparent, however, that operational amplifier limitations preclude

the use of these filters at high frequencies, attempts to integrate these filters have been unsuccessful (with the exception of a few no demanding applications), and convenient voltage or current control schemes for externally adjusting the filter characteristics do not exist.

2. These structures offer improvements in design simplicity and programmability when compared to op-amp based structures as well as reduced component count.
3. All transistors in the circuit are operated in the weak inversion region so that the low supply voltage and very low power consumption is also achieved.
4. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states.
5. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state.

4. Observations and Result Analysis

4.1 Gain Plot of 1st order Low Pass Filter

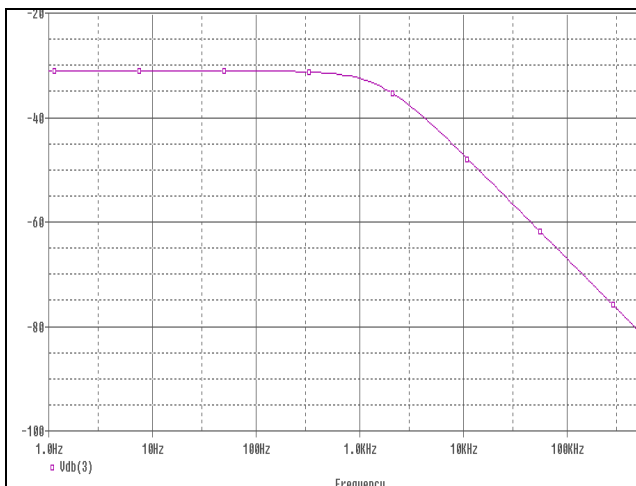


Figure 8: Gain Plot of 1st order Low Pass Filter

4.2 Theoretical Result

cut-off frequency $f_c = 1/(2\pi R_1 C_1)$.

So, the theoretical value of cut-off frequency of 1st order low pass filter is $f_c = 1/(2\pi * 10K * 0.01\mu F)$

$f_c = 1.59KHz$

4.3 Gain Plot of 2nd Order LPF

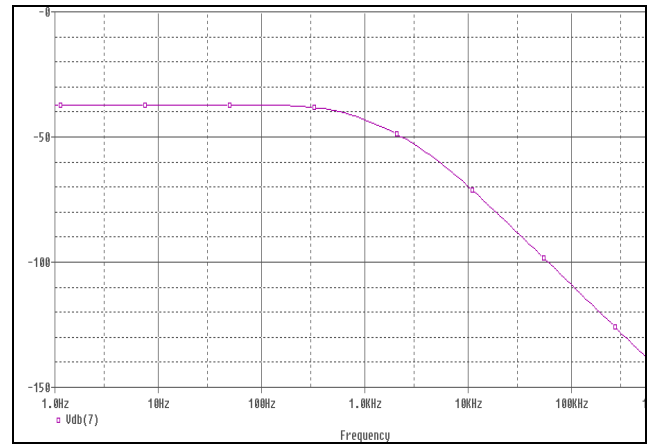


Figure 9: Gain Plot of 2nd Order LPF

4.3 Theoretical Result

Cut-off frequency $f_c = 1/2\pi \sqrt{(R_1 R_2 C_1 C_2)}$. So, from the practical circuit diagram the cut-off frequency of 2nd order low pass filter is $f_c = 1/2\pi \sqrt{(10K * 10K * 0.01\mu F * 0.01\mu F)} = 1.59KHz$.

5. Conclusion

The MOS transistors in the designed Operational Transconductance Amplifier (OTA) operate in sub-threshold or weak inversion region, such that their drain currents are exponentially related to gate-to-source voltages, in the nA and even pA level. Sub-threshold CMOS circuit design is very difficult, since the governing equations that model the behavior of the MOS transistor in weak inversion are so complicated. The most advantageous aspect of sub-threshold design is that the supply voltage can be decreased below 1 V. Using minimum number of transistors and other active elements, the sub-threshold design leads to very low-power operation of the devices. These structures offer improvements in design simplicity and programmability when compared to op-amp based structures as well as reduced component count.

6. Future Work

Due to the nature of wide screen topic, there are still several areas of Improvement for future work on this op-amp. One of the applications is described below:

6.1 CMOS as voltage controlled oscillator

If you have a resistor that is referenced to the virtual ground of an operational amplifier, then it is easy to use a CMOS to make that resistance voltage controlled. The resistor is replaced by a voltage divider to the real ground so that the divider puts out about 5 mV, which gets connected to the positive input of the CMOS. The negative input is connected to ground as well, while the output of the CMOS goes into the virtual ground of the operational amplifier. The apparent resistance can then be controlled by adjusting I0 accordingly.

Moreover it provides high noise immunity and low static power consumption.

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Author Profile



Sanchita Basu is currently pursuing B. Tech in Electronics & Communication Engineering at Future Institute of Engineering & Management under West Bengal University of Technology. Her research interest includes Control System and Radar Engineering.