A Repetitive Sparce Matrix Converter with Z-Source Network to having less Current THD

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Abstract: ***This paper proposed a new sparce matrix converter with Z-source network to provide unity voltage transfer ratio. It is an ac-to-ac converter with diode-IGBT bidirectional switches. The limitations of existing matrix converter like higher current THD and less voltage transfer ratio issues are overcome by this proposed matrix converter by inserting a Z-source. Due to this Z-source current harmonics are totally removed. The simulation is performed for different frequencies. The simulation results are presented to verify the THD and voltage transfer ratio and compared with the existing virtual AC/DC/AC matrix converter. The experimental output voltage amplitude can be varied with the variable frequencies.***

Keywords: Matrix converter, Z-source, Total Harmoni Distirsion(THD), Voltage Transfer Ratio,SVM.

1. Introduction

The most familiarised converter in the family of ac–ac direct converters is the matrix converter introduced by Venturini and Alesina [1-2]. In recent years, Enormous publications have illustrated with modulation schemes [3], load voltage generation issues, semiconductor device technology, gate drive issues [4], and the vibrant commutation procedure [5] for bi-directional switches . Matrix Converter technology has enhanced the household, industrial applications, aerospace applications and military electric vehicle applications with the availability of faster and efficient switching devices such as IGBT's , RB-IGBT's and GTO'[12]. The drawback is overcome by the analysis of Conduction and Switching losses of Matrix -Z-Source converter in recent studies [6]. Number of switching elements, more current THD, low voltage transfer ratio is inherent drawbacks observed from many publications [7-9]. The limitations of traditional matrix converters are overcome by inserting ac-ac Z-source network in m phase to n sparce matrix converters [10]. This is an impedance network consists of split inductors and capacitors connected in X-shape. This also provides high voltage conversion ratios and improving input and output currents quality. The existing virtual AC/DC/AC matrix converter is shown in fig.01 and the proposed sparce matrix converter with z-source network is shown in fig.02.

The matrix converters has the advantages such as bi-directional power flow, better sinusoidal input and output waveforms, minimum reactive energy storage components requirement ,it has the disadvantage of maximum output voltage limited to 86.6% of the input voltage. In the proposed converter due to voltage transfer ratio the maximum output can be improved to 91% for any type of modulation and the input/output current total harmonic distortion (THD) can be reduced to 5.54% to 4.47% when compared to virtual AC/DC/AC based matrix converter. One more advantage of this proposed circuit is that it is reducing the total number of semiconductor devices.

At first, this paper describes the system based on the virtual AC/DC/AC conversion with z-source in section.2.Second,the operational principle and equivalent circuit of the proposed MC is presented in section.3&.4 and in section.5 the modulation control is described. Finally, the experiment using a1. 2-kW prototype is demonstrated to confirm the validity of the proposed MC. As these results, it is confirmed that the proposed MC can reduce the switching loss in the entire load power.

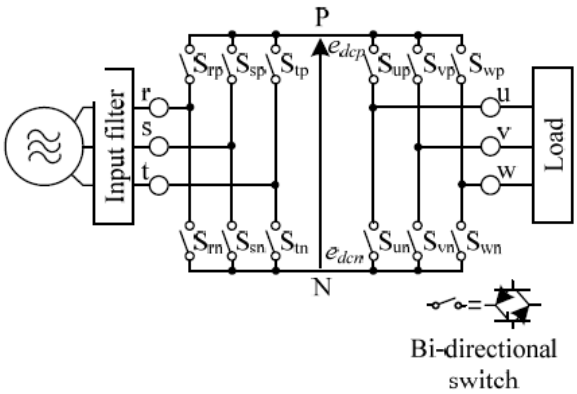

Figure 1: Virtual AC/DC/AC matrix converter

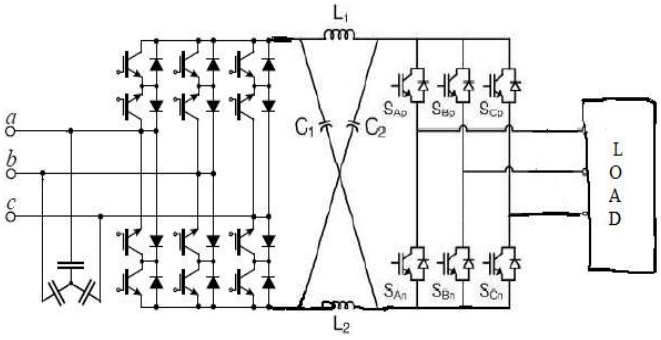

Figure 2: Proposed sparce matrix converter with z-source network

2. System Description

This section proposes the topology of sparse matrix converter. The three-phase sparse matrix converter with z-source topologies are developed based on virtual AC/DC/AC conversion of an indirect matrix converter. It can be classified according to a number of switches: sparse matrix converter (SMC), very sparse matrix converter (VSMC), and ultra sparse matrix converter (USMC). In this paper, the sparse matrix converter with z-source network is considered as a repetitive sparse matrix converter. It can be observed that the rectifier stage is connected to the inverter stage via

Z-source network. To decouple the converter from the utility grid, an LC filter is inserted between the converter and utility grid to attenuate high harmonics generated by the switch. In the rectifier stage, bi-directional switches are used to provide bi-polar blocking capability, each combination of two semiconductor device and four diodes functions as a bidirectional switch. The inverter stage is having only one semiconductor device as a switch. This is done because to reduce the semiconductors and its cost [14].

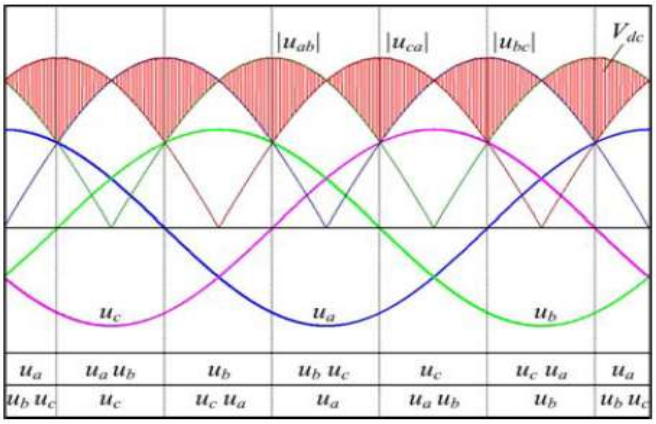

Figure 3: The dc-link voltage and input voltage

The aim of the modulation in rectifier stage is to produce maximum voltage in the dc-link as well as to maintain the sinusoidal input current and unity input power factor. The converter synthesizes a positive voltage in dc-link stage by selecting a switching state in the rectifier stage. Through the switching state, one phase of input sources is connected to the point P and the other phase to the point N in Fig.03. For example in the interval from $-\pi/6$ to $\pi/6$, the instantaneous input voltage u_a is positive and the upper switch of phase a stays on, while the input voltages u_b and u_c are negative and the lower switches of phase b and c are modulated to achieve the maximum voltage of dc-link. All other switches keep in off state in this region. Therefore, the dc-link voltage is formed by switching the rectifier stage between the largest and the second largest line-to-line input voltages. If the phase angle between the space vector of the input voltage and current is set to zero, a unity displacement factor is achieved. The inverter stage of the sparse matrix converter utilizes six-switch inverter. The inverter stage should be switched into a free-wheeling state and then the rectifier stage could commutate with zero current in dc-link stage. Therefore the commutation sequence of the power switches is very important for the sparse matrix converter topologies. If the current is flowing from the dc-link stage to the load, the switching state of the rectifier stage cannot be changed. Thus a commutation sequence is necessary to avoid shorting the input phases and safely changing from one state to another. In the inverter stage, the output voltage formation of traditional inverter space vector pulse width modulation (SVPWM) technique is achieved. In addition, it can be seen that the inverter switching frequency is twice of the rectifier switching frequency as a full switching cycle of the inverter is contained in each rectifier pulse half interval.

3. Operational Principle and Equivalent Circuits

The main reason that the Z-source network is employed to the sparce matrix converter (SMC) is to utilize its boosting feature for the wide range of obtainable voltage transfer ratio. Because of high switching frequency, the Z-source inverter stage can be regarded as a voltage source inverter fed by a constant dc voltage. The Z-source inverter can theoretically have any value between zero and infinity as an output voltage. To utilize the boosting feature of Z-source network, this SMC operates in two different states, which are referred to as a shoot-through state and a nonshoot through state (or a normal operating state), respectively. If it is assumed that the Z-source inverter stage is fed by a constant dc-link voltage, two equivalent circuits for each operating state can be achieved as shown in Fig.04.

In the equivalent circuits the series inductances are L_1 and L_2 and the shunt capacitances are C_1 and C_2 of the Z-source network. The voltage transfer ratio and current harmonics can be smoothen by adjusting the proper values of the series inductances and the shunt capacitances of the Z-source network.

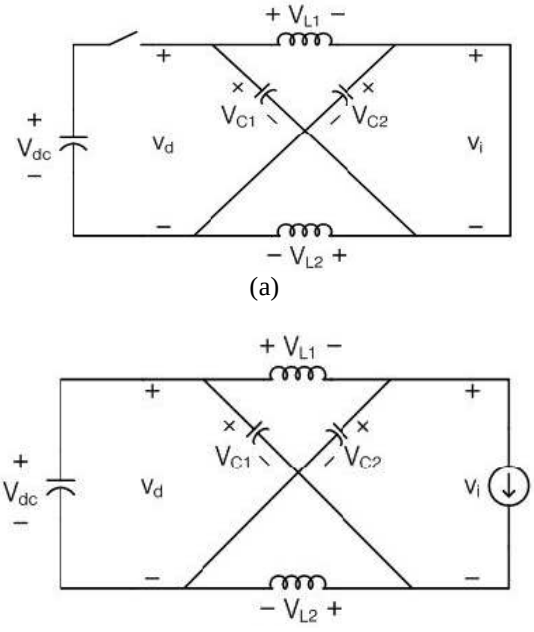

Figure 4: Equivalent circuits of the Z-source inverter stage during (a) shoot through state and (b) non shoot-through state.

Assuming that the inductors L_1 and L_2 have the same inductance (L) and capacitors C1 and C2 also have the same capacitance (C), the Z-source network becomes symmetrical.

From symmetry, we have

$$V_{L1}=V_{L2}=V_L$$
$$V_{C1}=V_{C2}=V_C \qquad (1)$$

The equivalent circuit during the shoot-through state can be configured as shown in Fig.04 (a). In the shoot-through state for an interval of T0, during a switching period, T, the Z-source inverter stage of the ZSMC is intentionally short-circuited and the dc-link switch S1 is opened, which

produces a shoot through zero state. The shoot-through can be achieved by 7 different ways: short-circuit of any one phase leg, any two phase legs or all three phase legs. This shoot-through zero state provides the unique buck-boost feature to the Z-source inverter stage. From the equivalent circuit, it is obvious that

$V_L=V_C$, $vd=2V_C$, $vi=0$ (2)

Now consider that the Z-source matrix converter is in the non shoot-through state for an interval of T_1, during the switching period, T. The equivalent circuit during the non shoot-through state can be configured as shown in Fig. 04(b). From the equivalent circuit during the nonshoot-through state, we have,

$V_L=V_{dc}-V_C$,$v_d=V_{dc}$,$v_i=V_L-V_C=2V_L-V_{dc}$ (3)

4. Theoretical Calculation of Voltage Transfer Ratio

To derive the theoretical equation of the overall voltage transfer ratio, a current in the inductor is firstly considered. During the shoot-through state, the current can be expressed as

$I_L=\frac{1}{L}\int_0^{T0} V_L dt + I_{L0}$ (4)

where I_{L0} is the initial current in the inductor. On the other hand, during the nonshoot-through state, the current is expressed as

$I'_L=\frac{1}{L}\int_{T0}^{T0+T1} V_L dt + I'_{L0}$ (5)

where I'_{L0} is the initial current in the inductor. Assuming that the inductance (L) and capacitance (C) are large enough and using (2) and (3), the change of current can be calculated from (4) and (5) as

$\Delta I_L = \frac{V_L}{L}\times T_0 = \frac{V_C}{L}\times T_0$ (6)

$\Delta I'_L = \frac{V_L}{L}\times T_1 = \frac{V_{dc}-V_C}{L}\times T_1$ (7)

The average voltage of the inductor over one switching period ($T=T_0+T_1$) should be zero in a steady state. In other words, the change of current over one switching period should be 0. Therefore, one has

$\Delta I_L + \Delta I'_L = \frac{V_C}{L}\times T_0 + \frac{V_{dc}-V_C}{L}\times T_1 = 0$ (8)

$\frac{V_C}{V_{dc}} = \frac{T_1}{T_1-T_0}$ (9)

From (3) and (9), the dc-link voltage across the inverter bridge can be expressed as

$v_f = 2V_C - V_{dc} = 2(\frac{T_1}{T_1-T_0})V_{dc} - V_{dc} = \frac{T}{T_1-T_0}V_{dc} = B.V_{dc}$dc

Where

$B = \frac{T}{T_1-T_0} = (0\sim\propto)$ (11)

is a boosting factor. With the dc-link voltage across the inverter bridge in (10), the output peak phase voltage of the ZSMC using the space vector pulse width modulation (SVPWM) can be expressed as

$\hat{v}ac = m_i.\frac{v_i}{\sqrt{3}} = m_i B.\frac{V_{dc}}{\sqrt{3}}$ (12)

where m_i is the modulation index of the inverter.

5. Control Modulation Strategy

The modulation concept derived in this section facilitates the zero dc-link current commutation with a shoot-through capability

5.1 Rectifier Stage

The required operating condition for the Z- source sparce MC is $v_{dc}>0$, positive unipolar dc-link voltage. In order to make a maximum voltage available for the formation of the output voltage, the input phase with the highest absolute value is clamped to the positive or negative dc-link bus in $\pi/3$ wide intervals as shown in Fig.05.

For example, let us consider the interval from 0 to $\pi/6$. In this interval, the input phase a,va is positive and has the highest absolute value. Hence, the upper switch in the phase a, S_{ap} stays on. On the other hand, S_{bn} and S_{cn} are modulated to achieve the positive maximum dc-link voltage and sinusoidal input current. The dc-link voltage v_{dc}, therefore, is determined by the segments of the input line-to-line voltages v_{ab} and v_{ac} according to the rectifier switching state. Assuming that the dc link current has a constant average value i for each rectifier switching state, we have

$\hat{i_a} = (d_{ab}+d_{ac}).\hat{i}$,
$\hat{i_b} = -d_{ab}.\hat{i}$,
$\hat{i_c} = -d_{ac}.\hat{i}$ (13)

where $d_{ab}+d_{ac}=1$ and dab and dac are the relative on-time of the switching states.

In order to achieve the unity input power factor, a proportional relationship between the local average value of an input phase current and the corresponding input phase voltage has to be guaranteed. That is,

$d_{ab} = -\frac{\hat{i_b}}{\hat{i}_a} = -\frac{v_b}{v_a}$,
$d_{ac} = -\frac{\hat{i_c}}{\hat{i}_a} = -\frac{v_c}{v_a}$ (14)

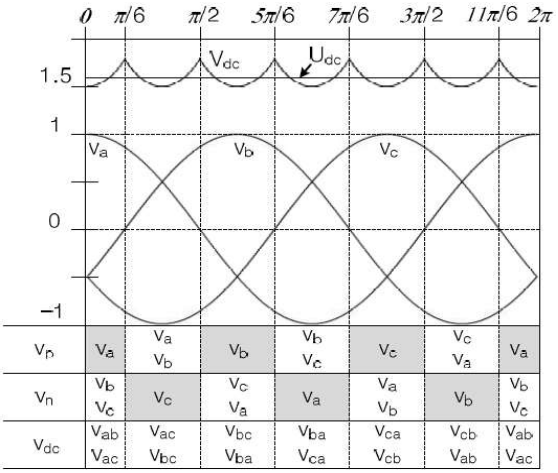

Figure 5: Rectifier switching states according to the input phase voltages va, vb and vc; Vdc denotes the local average value of the dc-link voltage and Udc denotes the global average value of the dc-link voltage.

Therefore, the local average value of the dc-link voltage is

$$V_{dc} = v_{ab}.d_{ab} + v_{ac}.d_{ac} \quad (15)$$

Assuming that the input three-phase voltage is balanced as

$$v_a = V_m \cos(\theta_a) = V_m \cos(wt)$$
$$v_b = V_m \cos(\theta_b) = V_m \cos(wt - 120°)$$
$$v_c = V_m \cos(\theta_c) = V_m \cos(wt + 120°) \quad (16)$$

the average value of the dc-link voltage of (13) can be derived. It is worth to note that the local average value of the dc-link voltage shows a variation with six times the input frequency.

5.2 Z-Source Inverter Stage

A modified SVPWM algorithm with a shoot-through capability can be utilized for the Z-source inverter stage, as shown in Fig. 6.

In order to ensure the zero dc-link current switching, the inverter stage should be switched into a freewheeling state (or a zero state) and then the rectifier stage commutates with zero dc-link current. During a free-wheeling state, a shoot-through zero state is inserted by opening the dclink switch S1 and short-circuiting any one phase leg, any two phase legs or all three phase legs of the inverter, which is forbidden in the traditional inverter. It should be noted that each phase leg still switches on and off once per switching period without changing the total time of a free-wheeling state.

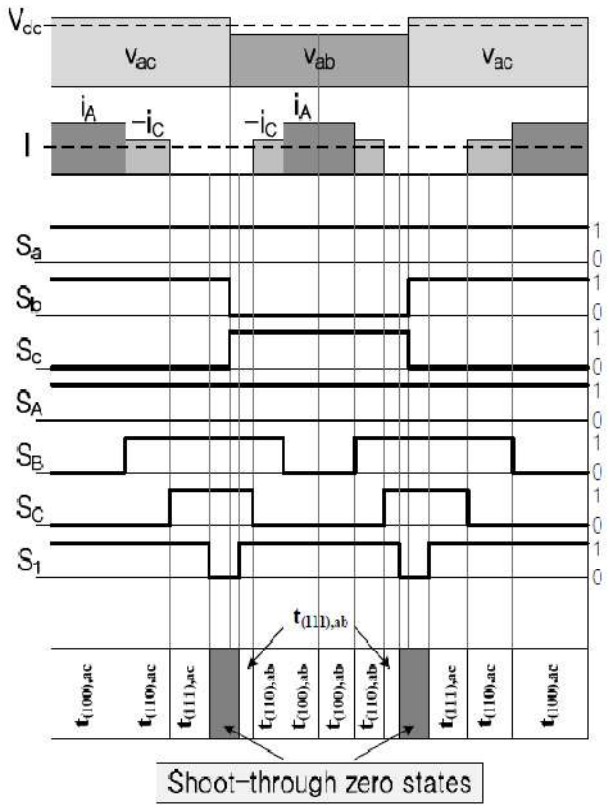

Figure 6: Example of a switching sequence of the ZSMC

That is, the active states are unchanged. However, the equivalent dc-link voltage to the inverter is boosted because of the shoot-through state. Let us consider the output voltage phase from 0 to π/6 to analyze the output voltage formation. The output voltage of this interval is formed by using the active voltage space vectors V1(100) and V2(110) and the free-wheeling state vectors (zero vectors) V0(000) or V7(111). The modulation of the active vectors generates the angular placement of the averaged output vector, while the zero vector is used to adjust the amplitude of the output vector. The duty cycles d(100), d(100) and d0 for the active vectors V1(100), V2(110) and zero vector can be achieved from

$$d_{(100)} = m_i.\sin\frac{\pi}{3} - \theta_{inv}$$
$$d_{(110)} = m_i.\sin(\theta_{inv})$$
$$d_0 = 1 - (d_{(100)} + d_{(110)} \quad (17)$$

where θ_{inv} indicates the angle of the voltage reference vector within the actual hexagon sector. Therefore, we have

$$d_{(100)ab} = d_{ab}.d_{(100)}, d_{(100).ac} = d_{ac}.d_{(100)},$$
$$d_{(110)ab} = d_{ab}.d_{(110)}, d_{(110).ac} = d_{ac}.d_{(110)},$$
$$d_{(111)ab} = d_{ab}.d_{(0)}, d_{(111).ac} = d_{ac}.d_{(0)} \quad (18)$$

For the convenience of achieving a shoot-through zero state, only V7 (111) is utilized as a zero vector. The actual zero state switching periods over one rectifier stage switching period can be achieved as

$$t_{(111).ab} = T.d_{(111).ab} - T_0.d_{ab}$$
$$t_{(111).ac} = T.d_{(111).ac} - T_0.d_{ac} \quad (19)$$

The voltage formations for the other output voltage phase intervals can be derived from symmetry considerations.

6. Simulation and Results

Simulations have been performed to confirm the theoretical calculation of the overall voltage transfer ratio and the current THD to verify the feasibility of the repetitive sparce matrix converter with z-source. The balanced three-phase input voltage of 100V/47Hz is supplied and the load is a 1.2kW.The simulation parameter is given in Table. I

Table 1: Simulation Parameters

Input filter parameters	L=75µH per phase C=125mF per phase
Z-source parameters	L=25mH C=10µF
Input supply	100v/47Hz
Load	1.2kW/50Hz

Using above simulation parameters the simulation circuit is constructed and it is shown in fig.07 and subsystem of rectifier is shown in fig.08. The rectifier is consists of three bi-directional switches. Fig.09 shows the waveforms of the input phase voltage and input current respectively. Fig.10 shows the waveforms of the output voltage and output current respectively when the overall voltage transfer ratio is 1 by selecting 0.9 for the modulation[11], [13] index and 0.268 for the shoot-through duty ratio.

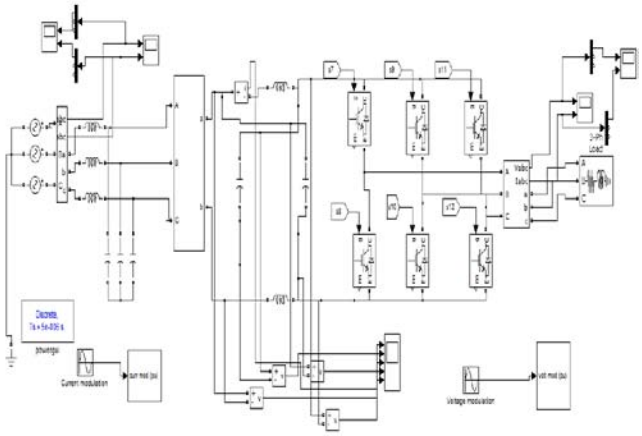

Figure 7: Simulation circuit of sparce MC

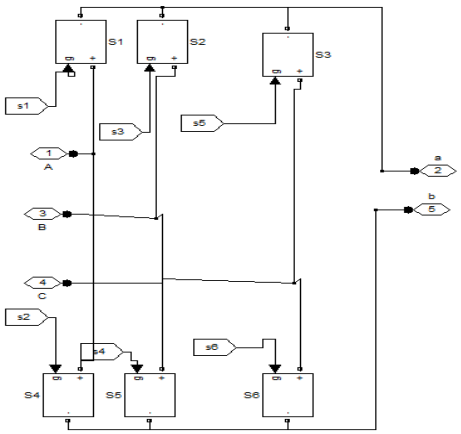

Figure 8: Rectifier circuit

The input current Total harmonic distorsion(THD) and output current THD is shown in fig.11 and fig.12.It is observed that the input current THD is 5.56% and the output THD is 4.67%.These THDs are are compared with the THDs of the existing virtual AC/DC/AC AC matrix converter[15].

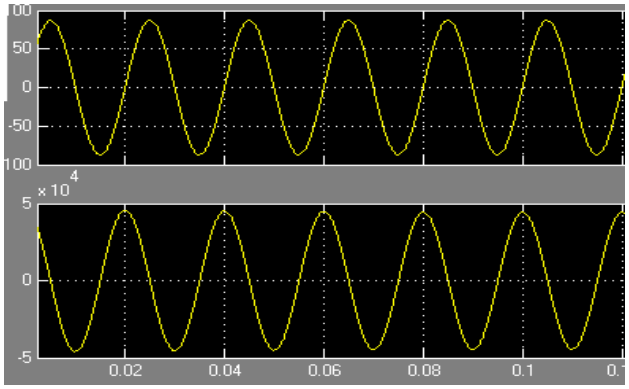

Figure 9: Input voltage and current waveforms

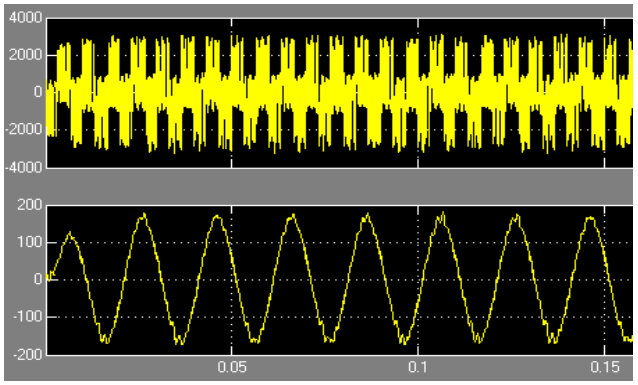

Figure 10: Output voltage and current waveforms

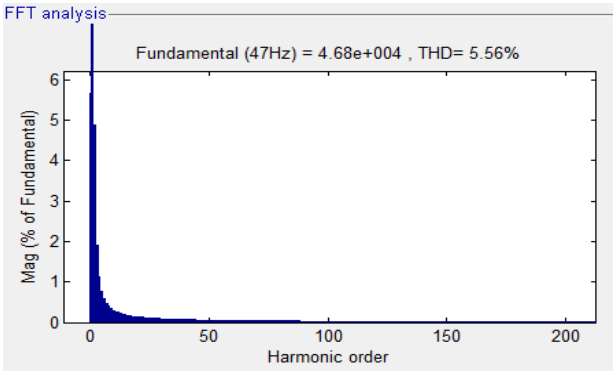

Figure 11: the THD of input current

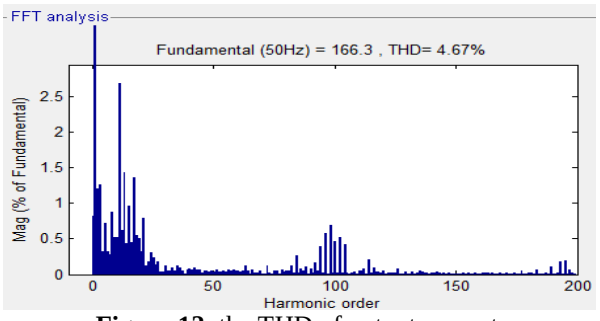

Figure 12: the THD of output current

7. Conclusion

This paper has presented a repetitive sparse matrix converter with z-source network which overcomes the inherent limitation of the reduced voltage transfer ratio more current harmonics of the virtual AC/DC/AC matrix converter and reduces the number of power semiconductor devices by employing the circuit structure of a sparse matrix converter. The proposed circuit employs impedance source network coupling the rectifier stage with the inverter stage at the dc-link to utilize its boosting feature. From the simulation results it is clear that this repetitive sparce matrix converter can decrease the currents THD, which means it, reduces the converter losses up to 38.3% and increases the efficiency to 96%.

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