# High Speed 8-bit Counters using State Excitation Logic and their Application in Frequency Divider

**Ranjith Ram. A[1], Pramod. P[2]**

[1]Department of Electronics and Communication Engineering
Government College of Engineering, Kannur, Parassinikkadvu, Kerala, India

[2]Department of Electronics and Communication Engineering
Lal Bahadur Shasthri College of Engineering, Kasaragod, Kerala, India

**Abstract:** ***Two innovative high-speed low power parallel 8-bit counter architectures are proposed. Then, High speed 8-bit frequency divider circuits using the proposed architectures are realized. The proposed parallel counter architectures consist of two sections – The Counting Path and the State Excitation Module. The counting path consists of three counting modules in which the first module (basic module) generates future states for the two remaining counting modules. The State Excitation Module decodes the count states of the basic module and carries this decoding over clock cycles through pipelined DFF to trigger the subsequent counting modules. The existing 8-bit parallel counter architecture [1] consumed a total transistor count of 442 whereas the proposed parallel counters consumed only 274 transistors. The power dissipation of the existing parallel counter architecture and the proposed parallel counter architecture were 4.21mW ($P_{INT}$) and 3.60mW ($P_{INT}$) respectively at 250MHz. The worst case delay observed for the 8-bit counter using existing parallel counter architecture [1] and the proposed parallel counter architectures were 7.481ns, 6.737ns and 6.677ns respectively using Altera Quartus II. A reduction in area (transistor count) by 27.45% and a reduction in power dissipation by 16.28% are achieved for the frequency dividers using proposed counter architectures. Also a reduction in delay by 10.75% and 7.62% is achieved for the 8-bit frequency divider circuits using proposed counter methods I & II respectively.***

**Keywords:** Counter, divide-by-m, frequency divider, high speed, low-power, modules, modulus

## 1. Introduction

A frequency divider is a modulo-m binary counter that provides an output pulse for every m clock pulses. A frequency divider is expected to have the following features: 1) A very short time between clock pulses, i.e., fast occurrence of clock pulses; 2) It should be programmable using external modulus select input, 3) It should be simple both in implementation and in use and 4) It should consume only a small area and a regular implementation should be possible. The counter circuits we introduce here have all these features.

Frequency dividers are basic blocks in numerous applications like generation of clock pulses of desired frequency, synchronization and data recovery and frequency synthesis in satellite communication systems. An innovative design of a frequency divider is carried out here. This unique circuit sequences through its states which ranges from 0 to the state determined by the external input 'm'. It consists of a high speed parallel counter with state excitation logic, a sequence restarter logic and a sequence termination logic with external programmable input 'm' for frequency select. The counting path of the 8-bit Parallel counting architecture [1] consists of four 2-bit modules separated by DFFs. Though the performance of the counter was found to be attractive, it consumed comparatively higher number of transistors thereby increasing total area required for the circuit realization. Therefore to negate these drawbacks of the counter architecture [1] alternative counter design strategies are proposed here. In the proposed architecture all the counting blocks are designed by using JK flip flops which reduces the number of gates required for its implementation. Also in place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of state excitation module.

A simple implementation of frequency divider is proposed by S. Abdel-Hafeez *et al.* However, the counter section of the frequency divider consumed more area and the circuit had dissipated more power because of the increased number of flip-flop used. In order to reduce high counter power consumption, Alioto *et al.* [3] presented a low power counter design with a relatively high operating frequency. Alioto's design was based on cascading an analog block such that each counting stage's input frequency was halved compared to the previous counting stage. However, Alioto's counter design's carry chain rippled through all counting stages, resulting in a total critical path delay equal to the sum of all counting stage delays. Subsequently, Alioto's design was not well suited for large counter widths because the carry chain limited operating frequency even though the carry chain voltage was not rail-to-rail. A dual-modulus prescaler constructed with two parts-a synchronous counter and an asynchronous counter was proposed by B.Chang *et al.* [4]. But the advantage of reduction power consumption was negated by reduction in speed. Though it was a dual modulus divider, it won't provide the option of selecting two modulus values externally.

Therefore a novel design of a frequency divider which sequences from 0 to the count value entered through the external frequency select input 'm' is proposed here. The remainder of the paper is organized as follows. Section 2 discusses about the proposed high speed parallel counter architectures. Section 3 provides an insight into the proposed frequency divider architecture. Section 4 provides a detailed discussion of the results and finally the conclusion is given in section 5

## 2. The Proposed 8-bit Parallel Counter Architectures

The major advantages of the proposed parallel counter architectures are listed below.

1) All the individual blocks in the counting path are designed by using JK flip-flops which reduces the number of gates required for its implementation. Therefore, the transistor count of the counting path is reduced.
2) In place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state excitation module. This also reduces the transistor count and thereby the area required for the realization of the counter.
3) The proposed counter has an operating frequency that is almost independent of counter width as a single clock input triggers all counting modules simultaneously.
4) The counter output is in radix-2 representation so read on-the-fly of the count value is possible with no additional logic decoding.

### 2.1 Method I

Figure 1 shows the functional block diagram of the proposed high speed parallel counter using method I. It consists of two sections – The *Counting Path* and *State Excitation Module*.

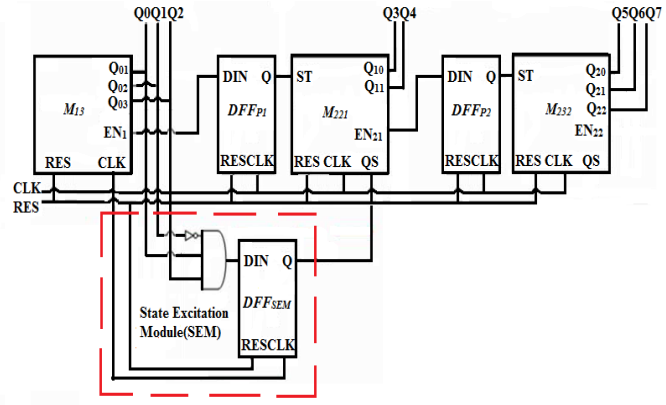


**Figure 1:** Functional block diagram of the proposed high speed parallel counter (method I)

#### 2.1.1 Counting Path:

The counting path consists of four different modules. They are $M_{13}$, $DFF_{PS}$, and two subsequent counting modules ($M_{2KS}$). In the counting path the counting modules are separated by the pipelining flip-flops $DFF_{PS}$.

#### (a) Module- $M_{13}$

The module $M_{13}$ is a parallel synchronous 3-bit up counter using JK flip-flops. The schematic is shown in Figure 2. Here the J and K inputs of all the flip flops are shorted and thus its operation is equivalent to a T flip-flop. The logic expressions of the outputs of the basic module $M_{13}$ are given by,

$$Q_{00}(t+1) = J_0 Q'_{00}(t) + K'_0 Q_{00}(t) \quad (1)$$
$$Q_{01}(t+1) = Q_{00}(t) Q'_{01}(t)) + Q'_{00}(t) Q_{01}(t) \quad (2)$$
$$Q_{02}(t+1) = Q_{01}(t) Q_{00}(t) Q'_{02}(t) + [Q_{01}(t) Q_{00}(t)]' Q_{02}(t) \quad (3)$$
$$EN_1 = Q_{02}\, Q_{01}\, Q'_{00} \quad (4)$$

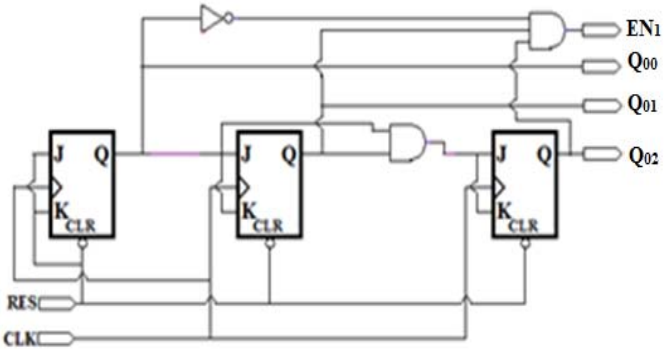


**Figure 2:** The Schematic diagram of Module- $M_{13}$ of the proposed high speed parallel counter (Method I)

The module $M_{13}$ is responsible for low-order bit counting and these three LSBs generate future states for all remaining modules in the counting path. In the counting path the enable output signal of module $M_{13}$ is pipelined through flip-flop $DFF_{P1}$ to enable the counting operation of the first subsequent counting module. Whenever the module $M_{13}$ output $Q_{02}Q_{01}Q_{00}$ =110, the input ST of the first subsequent counting module will be '1' after a single clock pulse. The counting module will change its state only if ST='1'. The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module.

#### (b) Module- $M_{2KS}$

The counting modules other than the basic module are represented here as $M_{2KS}$, where K represents the counter width of the counting module and S represents the position of the counting module after the basic module. The $M_{2KS}$ counting module will change its state only if ST='1'. The two $M_{2KS}$ modules shown in Figure3 are modules $M_{221}$ and $M_{232}$ respectively. Here module $M_{221}$ is a two bit counting module and module $M_{232}$ is a three bit counting module. Figure3 depicts the schematic diagram of module $M_{221}$ and the output expressions are given by

$$Q_{10}(t+1) = ST \text{ xor } Q_{10}(t) \quad (5)$$
$$Q_{11}(t+1) = [ST\ Q_{10}(t)] \text{ xor } Q_{11}(t) \quad (6)$$
$$EN_{21} = Q_{11}\, Q_{10} \quad (7)$$

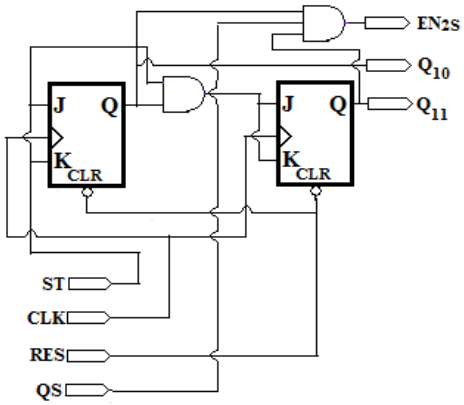


**Figure 3:** The Schematic diagram of Module- $M_{221}$ of the proposed high speed parallel counter (Method I)

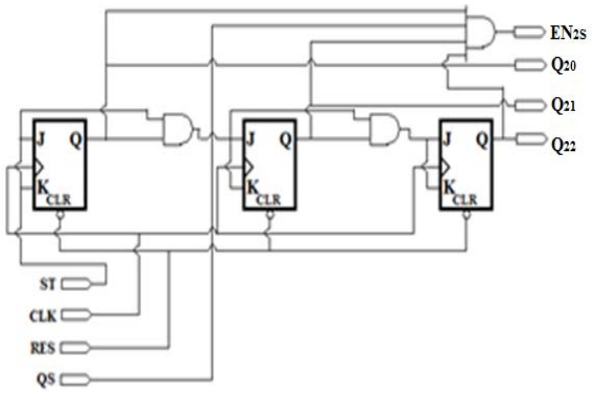


**Figure 4:** The Schematic diagram of Module- $M_{232}$ of the proposed high speed parallel counter (Method I)

Figure4 depicts the schematic diagram of Module- $M_{232}$ of the proposed high speed parallel counter (Method I) and the output expressions are given by

$Q_{20}(t+1)= ST \text{ xor } Q_{20}(t)$ (8)
$Q_{21}(t+1)= [STQ_{20}(t)] \text{ xor } Q_{21}(t)$ (9)
$Q_{22}(t+1)= [STQ_{21}(t)Q_{20}(t)] \text{ xor } Q_{22}(t)$ (10)
$EN_{22}= Q_{22}Q_{21}\,Q_{20}$ (11)

### (c) State Excitation Module (SEM)

The State Excitation Module consists of a D flip-flop $DFF_{SEM}$, a three input AND gate and an inverter. It decodes the count states of module $M_{13}$. This decoding is carried over two clock cycles through two DFFs ($DFF_{SEM}$ of SEM and the second pipelining flip-flop $DFF_{P2}$ of the counting path) to trigger the second subsequent module $\boldsymbol{M_{232}}$. In Figure 1, the counting path's first D flip-flop ($DFF_{P1}$) decodes the low-order state $\boldsymbol{Q_{02}Q_{01}Q_{00}}$ =110 and carries this decoding across one clock cycle and enables $\boldsymbol{Q_{11}Q_{10}}$ =01 at module $\boldsymbol{M_{221}}$ on the next rising clock edge. The State Excitation Module decodes the low-order state $\boldsymbol{Q_{02}Q_{01}Q_{00}}$ ==101 and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for $\boldsymbol{Q_{11}Q_{10}}$ =10 and a two-cycle mechanism for $\boldsymbol{Q_{02}Q_{01}Q_{00}}$ =101, $\boldsymbol{Q_{22}Q_{21}Q_{20}}$ can be enabled. Thus all modules are triggered concurrently on the clock edge, avoiding any rippling or long frequency delay.Figure 5 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.

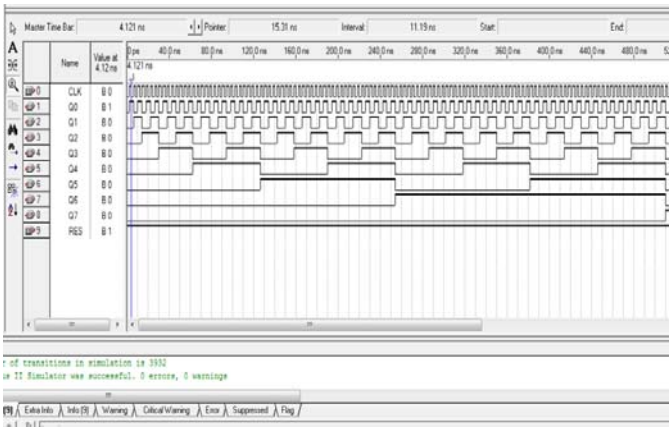

**Figure 5:** Measured waveforms of the proposed High Speed Counter using Altera Quartus II simulator at 250MHz

### 2.2 Method II

Figure 6 shows the functional block diagram of the proposed high speed parallel counter using method II. Similar to the parallel counter in figure 1, it consists of two sections – The Counting Path and State Excitation Module.

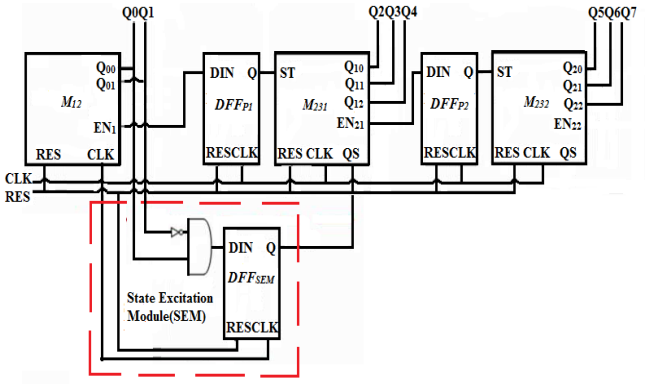


**Figure 6:** Functional block diagram of the proposed high speed parallel counter (method II)

### 2.2.1 Counting Path

The counting path consists of three different modules. They are $M_{13}$, $DFF_{PS}$, and two subsequent counting modules ($M_{2KS}$). Similar to method I, here also the counting modules are separated by the pipelining flip-flops $DFF_{PS}$ in the counting path.

### (a) Module- $M_{13}$

The module $M_{13}$ is a parallel synchronous 2-bit up counter using JK flip-flops. The schematic is shown in Figure 7. Here the J and K inputs of the flip flops are shorted and thus its operation is equivalent to a T flip-flop. The logic expressions of the outputs of the basic module $M_{13}$ are given by,

$Q_{00}(t+1) = J_0Q'_{00}(t) + K'_0Q_{00}(t)$ (12)
$Q_{01}(t+1) = Q_{00}(t)Q'_{01}(t)) + Q'_{00}(t)Q_{01}(t)$ (13)
$EN_1= Q_{01}\,Q'_{00}$ (14)

The module $M_{13}$ is responsible for low-order bit counting and these two LSBs generate future states for all remaining modules in the counting path.

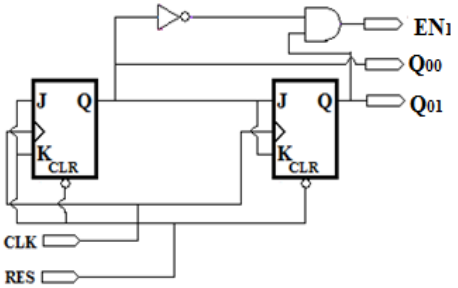


**Figure 7:** The Schematic diagram of Module- $M_{13}$ of the proposed high speed parallel counter (Method II)

**(b) Module- $M_{2KS}$**

Figure8 depicts the schematic diagram of module $M_{2KS}$. The two $M_{2KS}$ modules shown in figure8 are modules $M_{231}$ and $M_{232}$ respectively. The output expressions of module $M_{231}$ are given by,

$Q_{10}(t+1)= ST \text{ xor } Q_{10}(t)$ (15)
$Q_{11}(t+1)= [ST\ Q_{10}(t)] \text{ xor } Q_{11}(t)$ (16)
$Q_{12}(t+1)= [STQ_{11}(t)\ Q_{10}(t)] \text{ xor } Q_{12}(t)$ (17)
$EN_{21}= Q_{12}Q_{11}\ Q_{10}$ (18)

Similarly, the output expressions of module $M_{232}$ are given by,

$Q_{21}(t+1)= [STQ_{20}(t]) \text{ xor } Q_{21}(t)$ (19)
$Q_{22}(t+1)= [STQ_{21}(t)\ Q_{20}(t)] \text{ xor } Q_{22}(t)$ (20)
$EN_{22}= Q_{22}Q_{21}\ Q_{20}$ (21)

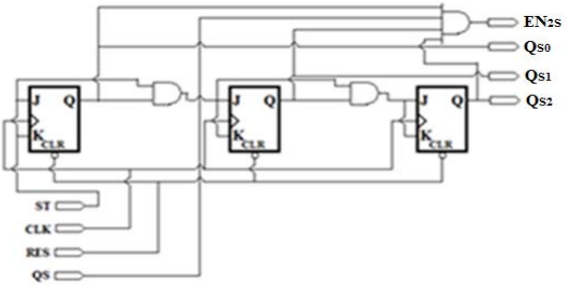


**Figure 8**: The Schematic diagram of Module- $M_{2KS}$ of the proposed high speed parallel counter (Method II)

**(c) State Excitation Module (SEM)**

The State Excitation Module consists of a D flip flop $DFF_{SEM}$, a two input AND gate and an inverter. It decodes the count states of module $M_{13}$. The State Excitation Module of the proposed high speed parallel counter of figure6 decodes the count states of its basic module, $M_{13}$. This decoding is carried over two clock cycles through two DFFs ($DFF_{SEM}$ of SEM and the second pipelining flip-flop $DFF_{P2}$ of the counting path) to trigger the second subsequent module $M_{232}$. In figure 6, the counting path's first D flip-flop ($DFF_{P1}$) decodes the low-order state $Q_{01}Q_{00}$ =10 and carries this decoding across one clock cycle and enables $Q_{12}Q_{11}Q_{10}$ =001 at module $M_{231}$ on the next rising clock edge. The State Excitation Module decodes the low-order state $Q_{01}Q_{00}$ ==01 and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for $Q_{12}Q_{11}Q_{10}$ =110 and a two-cycle mechanism for $Q_{01}Q_{00}$ =01, $Q_{22}Q_{21}Q_{20}$ can be enabled. Thus all modules are triggered concurrently on the clock edge, avoiding any rippling or long frequency delay. Figure 9 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.

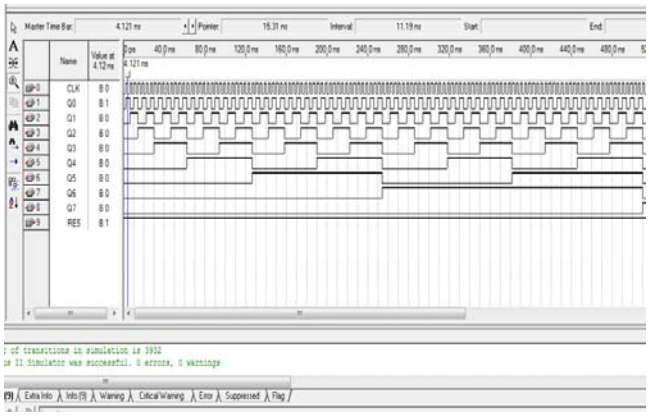

**Figure 9:** Measured waveforms of the proposed High Speed Counter (method II) using Altera Quartus II at 250MHz

## 3. The Proposed 8-bit Frequency Divider

It consists of a high speed parallel counter with state excitation logic, a sequence restarter logic and a sequence termination logic with external programmable input 'm' for frequency select.

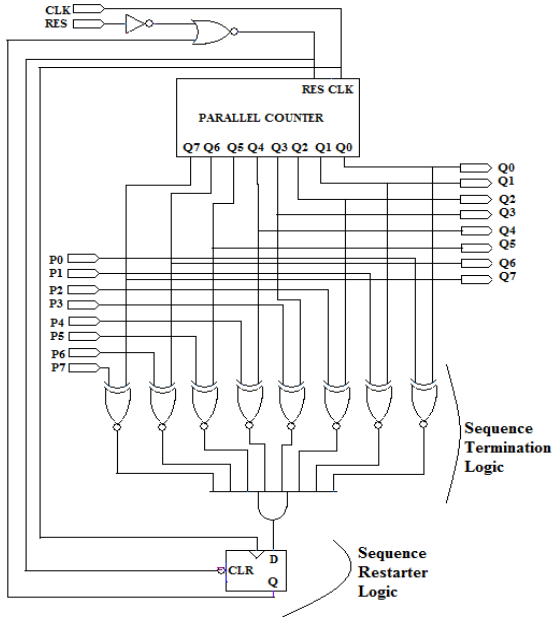


**Figure 10** The proposed 8 bit frequency divider circuit.

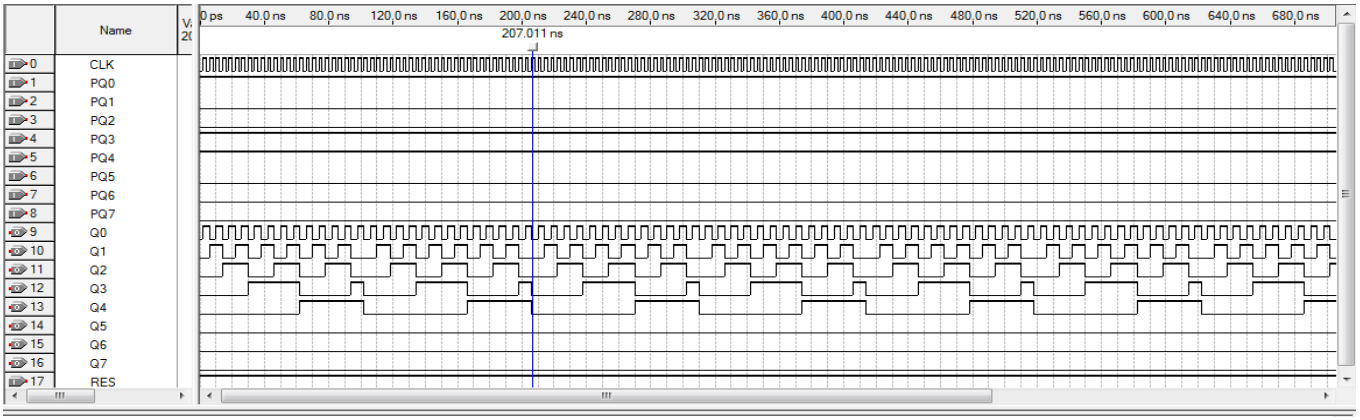


**Figure 11:** Measured waveforms of the proposed Frequency Divider using Altera Quartus II at 250MHz

**Table 1**: Comparison of performance parallel counter architectures

| *Parameter* | *Power* $P_{INT(mw)}$ | *Delay (ns)* | *Power Delay Product (PDP)* $X10^{-12}$ *Joules* | *Area in transistor count* |
|---|---|---|---|---|
| 8-bit Counter- S. Abdel-Hafeez et al.,[1] | 3.54 | 7.481 | 26.48 | 442 |
| The proposed 8-bit parallel counter (method I) | 2.91 | 6.737 | 19.6 | 274 |
| The proposed 8-bit parallel counter(method II) | 2.91 | 6.677 | 19.43 | 274 |
| conventional 8-bit synchronous counter | 2.3 | 8.648 | 19.89 | 196 |
| conventional 8-bit synchronous counter | 2.2 | 18.78 | 41.32 | 172 |

**Table 2:** Comparison of performance of frequency divider circuits

| *Parameter* | *Power* $P_{INT}$ *(mw)* | *Delay (ns)* | *Power Delay Product (PDP) X10-12Joules* | *Area in transistor count* |
|---|---|---|---|---|
| Proposed Frequency Divider using the proposed( method I) 8-bit parallel counter | 3.24 | 6.75 | 21.86 | 444 |
| Proposed Frequency Divider using the proposed( method II) 8-bit parallel counter | 3.24 | 7.02 | 22.73 | 444 |
| Frequency Divider using 8-bit parallel Counter of- S. Abdel-Hafeez et al.,[1] | 3.87 | 7.6 | 29.39 | 612 |
| Frequency Divider using the conventional 8-bit synchronous counter | 2.72 | 8.24 | 22.5 | 386 |
| Frequency Divider using the conventional 8-bit asynchronous counter | 2.62 | 18 | 47.22 | 342 |

Figure 10 shows the architecture of the proposed 8 bit frequency divider circuit. Here P7P6P5P4P3P2P1P0 indicates the external programmable inputs and Q7Q6Q5Q4Q3Q2Q1Q0 represents the output bit pattern of the frequency divider. The Sequence termination logic consists of 8 XNOR gates in a row followed by an AND gate. The sequence restarter logic consists of a DFF, an inverter and a two input NOR gate. The operation of the 8-bit frequency divider circuit can be summarized as follows. The counter starts its counting from the initial count state '00000000', provided that the reset input RES='1'.When the counter output pattern becomes equal to the select input combination, all the XNOR outputs become equal to '1' and thereby the output of the AND gate also becomes equal to the logic'1'. This logic '1' output triggers the sequence restarter logic and RESETs the counter such that the counter always sequences through the number of states determined by the external select input.

Figure 11 depicts the measured waveforms of the proposed Frequency Divider using Altera Quartus II at 250MHz. It can be noted that for the given input '00011001' the frequency divider circuit starts its cycle from '00000000'. The sequence termination logic compares current counting state with the given input. When both values become equal the sequence termination logic terminates the present counting sequence and the sequence restarter thereafter causes the commencement of a fresh counting cycle.

## 4. Results and Discussion

In this section at first the performance of the proposed high-speed low power parallel 8-bit counter architectures are analyzed and compared with Abdel-Hafeez's counter [1], conventional synchronous and asynchronous counters. Then 8-bit frequency divider circuits were realized using the five different types of counter circuits(two proposed counter architectures, Abdel-Hafeez's counter [1], conventional synchronous and asynchronous counters) and the results were compared.Note that for all the observations the device cyclone EP1C20F400C7 is used.

Table 1 show that a reduction in area (transistor count) by 38% and a reduction in power dissipation by 17.80% are achieved for the proposed counter architectures. A reduction in delay by 0.1% and 0.107% is achieved for proposed methods I & II respectively. When compared with existing Digital CMOS Parallel counter [1], the proposed Parallel counters show improved performance in terms of power consumed, delay and area. Table 2 shows that a reduction in area (transistor count) by 27.45% and a reduction in power dissipation by 16.28% are achieved for the 8-bit frequency divider using proposed counter architectures. A reduction in delay by 10.75% and 7.62% is achieved for proposed methods I & II respectively.

## 5. Conclusions

In this paper, performance of the proposed high-speed low power parallel 8-bit counter architectures are analyzed and compared with the existing parallel counter architectures. Then the frequency divider circuits are realized using all possible types of counter circuits (conventional synchronous,

conventional asynchronous, existing [1] and two proposed counter architectures). The performance of the frequency divider circuits so formed are analyzed and compared. The existing 8-bit parallel counter architecture [1] consumed a total transistor count of 442 whereas the proposed parallel counters consumed only 274 transistors. The power dissipation of the existing parallel counter architecture [1] and the proposed parallel counter architecture were 4.21mW (PINT) and 3.60mW (PINT) respectively at 250MHz. The worst case delay observed for the 8-bit counter using existing parallel counter architecture [1] and the proposed parallel counter architectures were 7.481ns, 6.737ns and 6.677ns respectively using Altera Quartus II. A reduction in area (transistor count) by 38% and a reduction in power dissipation by 17.80% is achieved for the proposed counter architectures. The delay has been reduced by 10% and 10.7% respectively for proposed methods I & II. A reduction in area (transistor count) by 27.45% and a reduction in power dissipation by 16.28% are achieved for the frequency dividers using proposed counter architectures. Also a reduction in delay by 10.75% and 7.62% is achieved for the frequency dividers using proposed counter methods I & II respectively.

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## Author Profiles

**Dr. A. Ranjith Ram** received his B. Tech. degree in Electronics and Communication Engineering from NSS College of Engineering Palakkad, under the University of Calicut in 1995, M. Tech. degree in Applied Electronics and Instrumentation from College of Engineering Thiruvananthapuram, under the University of Kerala in 1998 and Doctorate in Video Analysis from IIT Bombay in 2011. He started his professional career as an ad-hoc Lecturer at the Department of Electronics and Communication Engineering at Government Engineering College Thrissur in 1996. Then he was a faculty of the Department of Electronics and Communication Engineering, LBS College of Engineering, Kasaragod, Kerala until 2001. Currently he works as Assistant Professor in the Department of Electronics and Communication Engineering, Government College of Engineering, Kannur, Kerala. He is having 16 years of experience in teaching in various Engineering Institutes and is a life member of Indian Society of Technical Education. He has published many papers in National as well as International Conferences and written a book on Video Analysis published by Springer. His research interests include Digital Systems Design, Digital Signal Processing, Image Processing, Computer Vision, Video Analysis and Multimedia.

**Pramod P** received his Master of Engineering degree in VLSI DESIGN from Anna University, Chennai. He is presently working as Assistant Professor in the Department of Electronics and Communication Engineering, Lal Bahadur Shasthri College of Engineering, Kasaragod, India. He has 13 years of teaching experience in both undergraduate and postgraduate programs in engineering. He has published many papers in the International & National Journal and Conferences. His current interest includes Digital System Design, Low Power Techniques, VLSI Design & Testing, and VLSI Signal Processing. He is a life member of Indian Society of Technical Education. He has completed Executive Program for Young Professionals from IIM Calcutta and Master of Business Administration from ICFAI University.