Low Power Area Efficient Parallel Counter Architecture

Lekshmi Aravind

M-Tech Student, Dept. of ECE, Mangalam College of Engineering, Kottayam, India

Abstract: ***Counters are specialized registers and is considered as essential building blocks for a variety of circuit operations such as programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Since many applications are comprised of these fundamental operations, much research focuses on efficient counter architecture design. This paper proposes an 8-bit high speed parallel counter architecture. The counter consists of two main sections- the counting section and the state Anticipation Module.The total equivalent gate count for our proposed counter is 164 whereas the existing counter architecture consumes 266.The delay of the proposed counter architecture is 3.968ns and that of existing counter is 4.952ns. The Power consumption is 28.80mW for our proposed counter and 29.24mW for the existing one.***

Keywords: parallel counter design, high speed, state anticipation module.

1. Introduction

Fast counter is a key element in most of the circuit operations such as frequency dividers, shifters and arithmetic operations such as multipliers. Basic properties preferred for a fast counter includes high count rate, read on the fly and implementation suitable for VLSI. As the speed of operation is determined by the propagation delay time of the count enable signal from the LSB to the MSB, most of the counters cannot satisfy the speed requirements. Therefore, the counter's size is considered to be the main limiting factor of the counting rate [I]. Some traditional approaches enhanced the counting speed by improving the circuit implementation of various gates and flip-flops, [2], [3], [4]. But these techniques are not well suited for counters employed in arithmetic circuits. As a substitution to the carry chain, Kakarountas et al. [10] used a carry look-ahead circuit [9]. With the expense of an extra detector, the carry look-ahead

Circuit used a prescaler technique with systolic 4-bit counter modules using T-type flip-flops. The detector circuit output is used to enable counting in the higher order bits. Kakarountas‟s design used DFFs between the counter modules to improvise the operating frequency. As the counter design was limited by control signal broadcasting, Kakarountas‟s design was not practical for large counter widths. S. Abdel-Hafeez et al. [6] proposed a simple implementation of frequency divider. However, the circuit operation is confined to frequency division operation and has no provision for multiple arithmetic functionalities. In order to reduce the power consumption, Alioto et al. [7] presented a low power counter design with a relatively high operating frequency. Alioto‟s design was based on cascading an analog block such that each counting stage‟s input frequency was halved compared to the previous counting stage. However, Alioto‟s counter design‟s carry chain rippled through all counting stages, resulting in a total critical path delay equal to the sum of all counting stage delays. Subsequently, Alioto‟s design was not well suited for large counter widths because the carry chain limited operating frequency even though the carry chain voltage was not rail-to-rail. A dual-modulus prescaler constructed with two parts-a synchronous counter and an asynchronous counter was proposed by B. Chang et al. [8].But the advantage of reduction power consumption was negated by reduction in speed.

The counting path of the 8-bit Parallel counting architecture [5] consists of four 2-bit modules separated by DFFs. Though the performance of the counter was found to be attractive, it consumed comparatively higher number of transistors thereby increasing total area required for the circuit realization. Therefore to negate these drawbacks alternative counter design strategies are proposed here. In the proposed architecture all the counting blocks are designed by using JK flip-flops which reduces the number of gates required for the overall implementation of the circuit. Also in place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state anticipation module.

2. Parallel Counter Architecture

Figure 3 shows the functional block diagram of the proposed high speed parallel counter. It consists of two sections – The Counting Section and State Anticipation Module.

2.1 Counting Section

The counting section consists of three different modules. They are BCM, SCM1, and SCM2. The module BCM represents the Basic Counting Module. SCM1 and SCM2 represent the first and second Subsequent Counting Modules respectively.

2.1.1 Module-BCM

The basic module BCM is a parallel synchronous 3-bit up counter using JK flip-flops. The schematic is shown in Figure 1. Here the J and K inputs of all the flip flops are shorted and thus its operation is equivalent to a T flip-flop. The output expressions of the basic module BCM is given by,

$$Q0(t+1) = 1 \oplus Q0(t)$$

$$Q1(t+1) = Q0(t) \oplus Q1(t)$$

$$Q2(t+1) = [Q1(t)Q0(t)] \oplus Q2(t)$$

The module BCM is responsible for the three low-order bit counting and these three LSBs generate future states for counting modules SCM1 and SCM2 in the counting section. Whenever the module BCM output Q2Q1Q0 =110, the input TR of the first subsequent counting module will be „1" after a single clock pulse. The counting module will change its state only if TR="1". The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module SCM1.

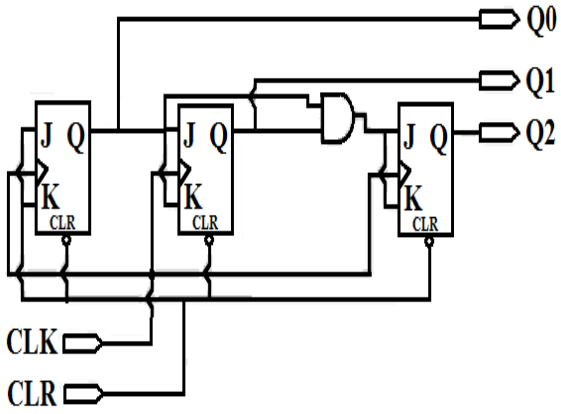


Figure 1: The Schematic diagram of Module- BCM of the proposed high speed parallel counter

2.1.2 Module - SCMK

The counting modules other than the basic module are represented here as SCMK**,** where K is equal to „1" for the first subsequent module and equal to "2" for the second subsequent module. The SCMK counting modules will change its state only if TR="1". The first and second SCMK modules are shown in Figure 2 and Figure 4 respectively. Here SCM1 is a two bit counting module and SCM2 is a three bit counting module. Similar to module BCM, JK flip-flops are used to realize the circuits of modules SCM1 and SCM2.

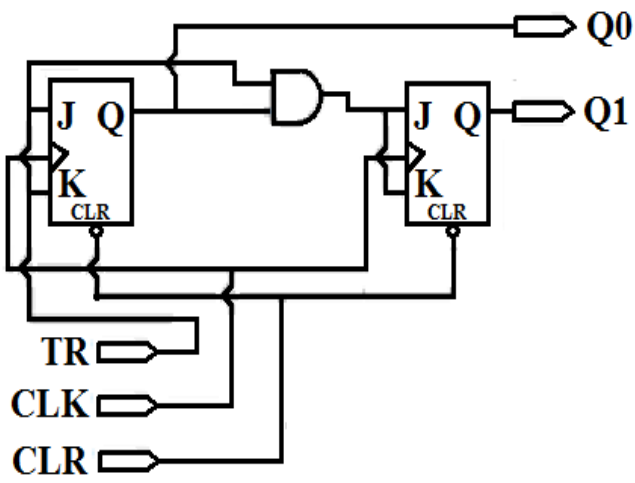


Figure 2: The Schematic diagram of Module- SCM1 of the proposed high speed parallel counter

The output expressions of SCM1 are given by,

$$Q0(t+1) = TR \oplus Q0(t)$$

$$Q1(t+1) = [TR\,Q0(t)] \oplus Q1(t)$$

The output expressions of SCM2 are given by,

$$Q0(t+1) = TR \oplus Q0(t)$$

$$Q1(t+1) = [TR\,Q0(t)] \oplus Q1(t)$$

$$Q2(t+1) = [TR\,Q1(t)\,Q0(t)] \oplus Q2(t)$$

2.2 State Anticipation Module (SAM)

The State Anticipation Module consists of three D flip-flops, three 3-input AND gates and two inverters. It decodes the count states of basic counting module BCM. This decoding is carried over two clock cycles through two DFFs to trigger the second subsequent module, SCM2. In Figure 3, the first row consisting of a D flip-flop, a 3-input AND gate and an inverter decodes the low-order state Q2Q1Q0 =110 and carries this decoding across one clock cycle and enables Q4Q3 =01 at module SCM1 on the next rising clock edge. The second row of the State Anticipation Module decodes the low-order state Q2Q1Q0 =101 and carries this decoding over two cycles. By Combining the one cycle action in the counting section for Q4Q3 =10 and a two-cycle action for Q2Q1Q0 =101, Q7Q6Q5 can be enabled. The propagation delay can be considerably reduced by this type of simultaneous triggering of all the modules

3. Block Diagram of Proposed Parallel Counter

The architecture consists of mainly two sections;

(a) Counting section
(b) State anticipation module

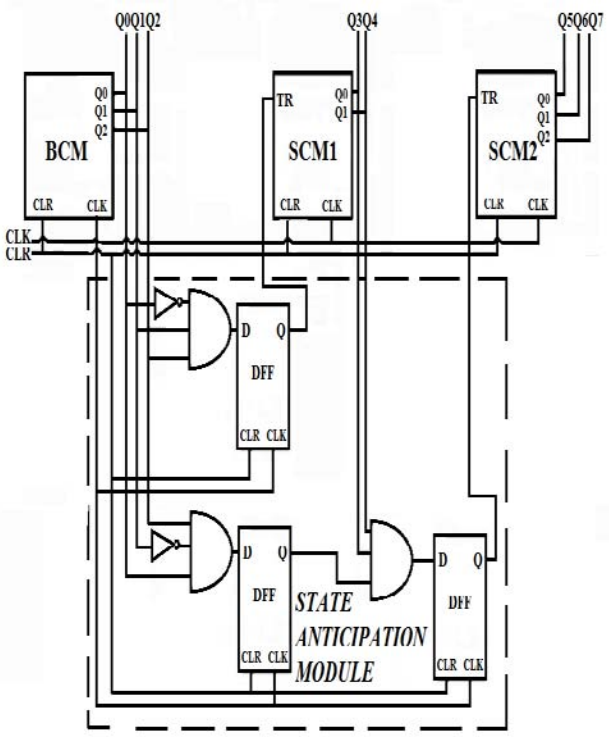


Figure 3: Functional block diagram of the proposed high speed parallel counter

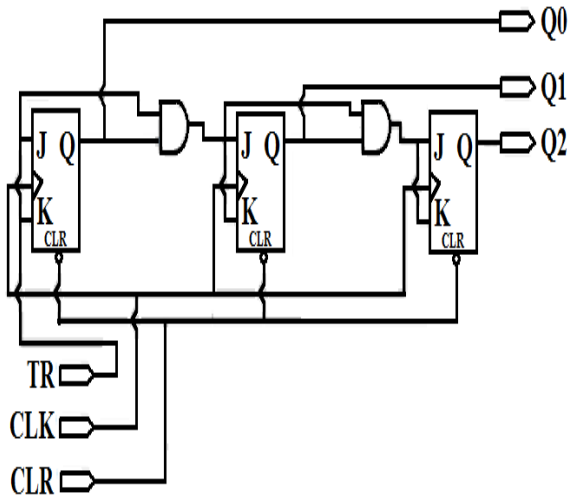
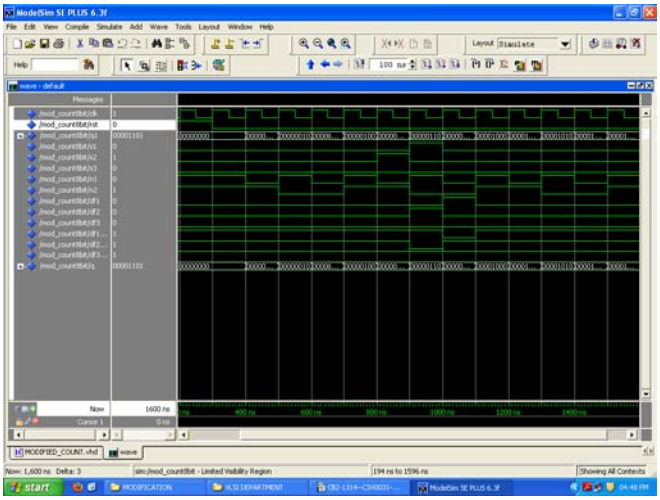


Figure 4: The Schematic diagram of Module- SCM2 of the proposed high speed parallel counter

4. Area, Power and Delay Measurements



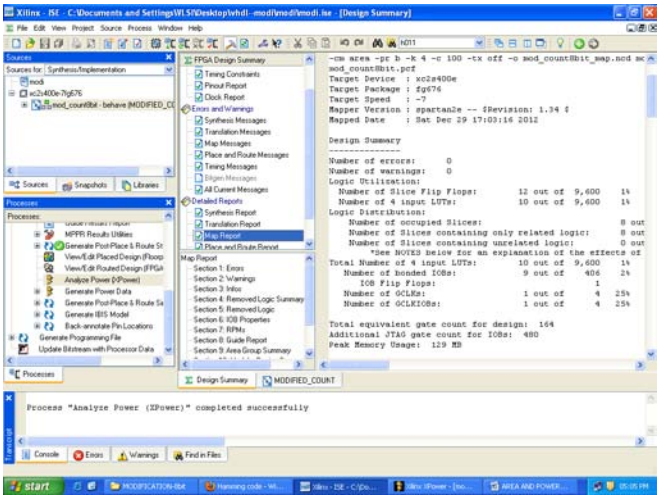


Figure 5: Total equivalent gate count for design=164

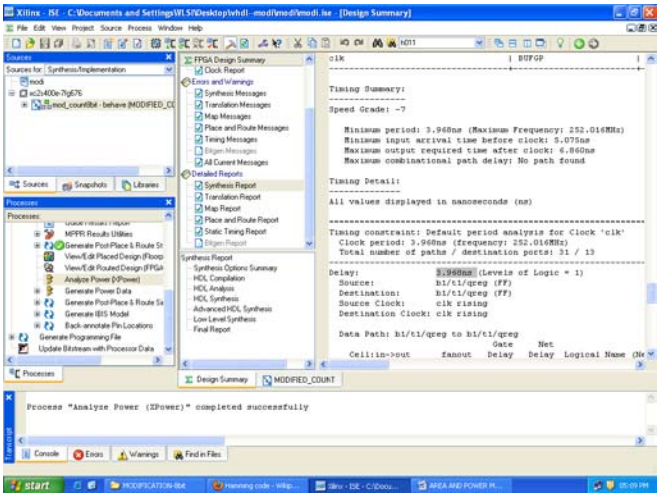


Figure 6: Total delay=3.968ns

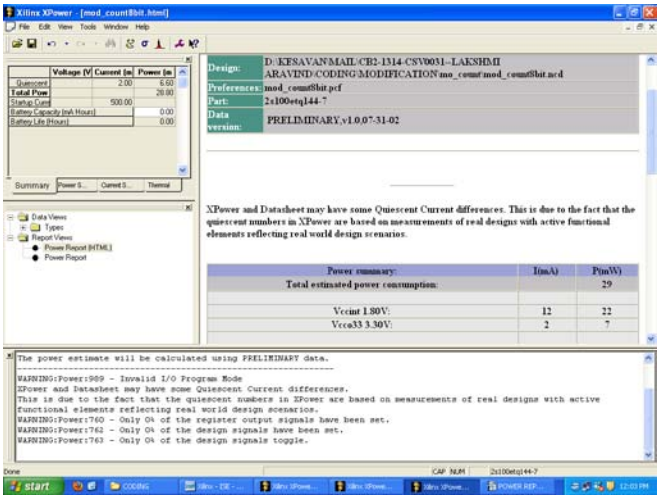


Figure 7: Total power consumption=28.80mW

5. Results and Discussions

The performance analysis of the proposed high-speed low power parallel 8-bit counter architecture and the existing counter architecture is provided in this section.

6.1 Existing Counter Architecture

It is a high-speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology (a counting path and state look-ahead path), using only three simple repeated CMOS-logic module types: an initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path, simple D-type flip-flops, and 2-bit counters. The state look-ahead path prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously, thus concurrently updating the count state with a uniform delay at all counting path modules/stages with respect to the clock edge.

The counting path of the 8-bit Parallel counting architecture [5] consists of four 2-bit modules separated by DFFs. Though the performance of the counter was found to be attractive, it consumed comparatively higher number of transistors thereby increasing total area required for the circuit realization

6.2 Comparison of Performance of Parallel Counter Architectures

Table 1: Comparison of performance of parallel counter architectures

Parameter	*Area*	*Power(mW)*	*Delay(ns)*
The 8-bit parallel counter using existing method	266	29.24	4.952
The 8-bit parallel counter using proposed method	164	28.80	3.968

6.3 Proposed Counter Architecture

In the proposed architecture all the counting blocks are designed by using JK flip-flops which reduces the number of gates required for the overall implementation of the circuit. Also in place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state anticipation module.

6. Conclusions

In this paper we presented a high speed parallel counter architecture.Our counter design consist of mainly two sections (a)Counting section (b)state anticipation module. The AND gate rippling that results in reduction in speed in conventional counters has been eliminated by the proposed counter methodology. The tabulated results demonstrate the better performance of the proposed parallel counter in terms of delay, power and area compared to previous work. The total equivalent gate count for our proposed counter is 164 whereas the existing counter architecture consumes 266.The delay of the proposed counter architecture is 3.968ns and that of existing counter is 4.952ns. The Power consumption is 28.80mW for our proposed counter and 29.24 for the existing one.

References

[1] Chu, D. "Phase digitizing sharpens timing measurements," IEEE Spect., pp. 28-32, July 1988
[2] Yuan, J.R. "Efficient CMOS Counter Circuits," Electronics Letters, vol. 24, pp. 1,311-1,313, Oct. 1988.
[3] Yuan, J.R. and Svensson, C. "Fast CMOS Nonbinary Divider and Counter," Electronics Letters, vol. 29, pp. 1,222-1,223, June 1993.
[4] Rogenmoser, R., Huang, Q and Piazza, F "1.57 GHz Asynchronous and 1.4 GHz Dual-Modulus 1.2 mm CMOS Prescalers," Proc. Custom Integrated Circuits Conf., pp. 387-390, May 1994.
[5] Abdel Hafeez, S and Ann Gordon Ross,"A Digital CMOS Parallel Counter Architecture Based on State Look-Ahead Logic", IEEE Transactions on Very Large Scale Integration(VLSI) Systems, vol.19, no. June2011
[6] Abdel-Hafeez, S Harb.S, and Eisenstadt.W, "High speed digital CMOS divide-by-N frequency divider," in Proc. IEEE Int. Symp. Circuits Syst., pp. 592–595,2008
[7] Alioto, M. Mita. R, and Palumbo. G,"Design of high-speed power-efficient MOS current-mode logic frequency dividers," IEEE Trans. Circuits Syst. II, Expr. Briefs, vol. 53, no. 11, pp. 1165–1169, 2006
[8] Chang, B Park. J and Kim. W, "A 1.2 GHz CMOS dual-modulus prescalar using new dynamic D-type flip-flops," IEEE J. Solid-State Circuits, vol. 31, no. 5, pp. 749–75, 1996
[9] Hendry. D. C, "Sequential lookahead method for digital counters," IEEE Electron. Lett. vol. 32, no. 3, pp. 160–161, 1996.
[10] Kakarountas, A.P., Theodoridis, G., Papadomanolakis K. S. and C. E. Goutis, "A novel high-speed counter

with counting rate independent of the counter‟s length," in Proc. IEEE Int. Conf. Electron., Circuits Syst. (ICECS), UAE, Dec. 2003, pp. 1164–1167.

[11] Pramod.P®, "A High Speed Parallel Counter Architecture and its Implementation in Programmable Square Finder cum Frequency Divider Circuit," International Journal of Computer Applications (0975 – 8887) Volume 46– No.12, May 2012

Author Profile

Lekshmi Aravind was born in Kayamkulam, Kerala, India. She has received her B. Tech degree in Electronics and Communication Engineering from Anna University, Tamil Nadu, India and pursuing M. Tech in VLSI &Embedded System from Mahatma Gandhi University, Kerala, India.