ECG QRS Complex Detector

Chinchu Venu Gopal

M. Tech Student, Mangalam College of Engineering Ettumanoor, Kerala, India

Abstract: ***This paper aims to present a very-large-scale integration (VLSI) friendly electrocardiogram (ECG) QRS detector for body sensor networks. Baseline wandering and background noise are removed from original ECG signal by mathematical morphological method. The performance of the algorithm is evaluated with standard MIT-BIH arrhythmia database and wearable exercise ECG Data. Corresponding power and area efficient VLSI architecture is reduced by replacing the one of the Ripple Carry Adder in the Carry select adder with Binary to Excess 1 converter***

Keywords: Networks, mathematical, physiological, sensor, detectors, ECG

1. Introduction

As one of the important physiological sensor nodes in BSN, wearable electrocardiogram (ECG) sensor is dedicated to measuring the rate and regularity of heartbeats as well as the size and position of the chambers, the presence of any damage to the heart and the effects of drugs or devices used to regulate the heart. In ECG signal processing, all the extensive analysis need the information of QRS positions as a basic. QRS detectors have been regarded as a mature topic until the BSN is introduced, where; unfortunately, the ECG sensor requires real-time, miniature form factors and long lifetimes that push the limits of ultra low power circuit and system design. Among the noises plaguing the ECG are the power-line interference: 50/60 Hz pickup and harmonics from the power cord; electrode contact noise: baseline drift due to variable contact between the electrode and the skin; motion artifacts: shifts in the baseline caused by changes in the electrode-skin impedance; muscle contraction: electromyogram -type signals electromagnetic interference and noise coupled from other electronic devices. While the BSN devices are generally restricted by size, power consumption, and computational load, it will be worthwhile exploring a simple and accurate QRS detection algorithm based on morphology, instead of frequency, for the BSN ECG devices. In this paper, we utilize two most fundamental morphological operators (erosion and dilation) in mathematical morphology technology to reduce the computational complexity for wearable ECG QRS detector.

Also the power and area can be reduced by using a BEC. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers (mux). the basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption . The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

This remainder of paper is organized as follows. In Section II, a brief introduction of mathematical morphology filtering is given, which serves as a basis for the proposed algorithm. Section III presents the new algorithm and section 1V and V describes the delay and area evaluation of modified and regular CSLA.

2. Theory of Mathematical Morphology

Mathematical morphology is a set-theoretic method of image analysis providing a quantitative description of geometrical structures. And it provides an effective way to analyze signals using nonlinear signal processing operators incorporating shape information for extracting image components that are useful for representation and description. A morphological operation is actually the interaction of a set or function representing the object or shape of interest with another set or function of simpler shape called structure element. The geometry information of the signal is extracted by using the structure element to operate on the signal. The shape of the structure element determines the shape information of the signal that is extracted under such an operation. Such operators serve two purposes, i.e., extracting the useful signal and removing the artifacts.

There are two most basic morphological set transformation operators: dilation and erosion, which all other mathematical morphology operations are based on. The operators for 1-D signal f (n) and structure element g(n) are listed below for easy reference.

DIALATION= max [(f (n-i) +g(i))]
EROSION = max [(f (n-i) -g(i))]

Where *i* indicates *ith* element in a length structure element, and is a predefined structure element. Opening and closing are two extended morphological operators based on dilation and erosion. In mathematical morphology, opening is the dilation of the erosion of a set by a structuring element; the closing of a set by a structuring element is the erosion of the dilation of that set. Opening and closing operations could also work as morphology filters with clipping effects, i.e., cutting down peaks and filling up valley

OPENING= f g =(f⊖g)o⊕ $g(n)$
CLOSING= f*g(n) =(f ⊕ g) ⊖ g(n)

3. QRS Detection Algorithm

Mathematical morphological technology extracts the effective information based on shapes in the image, not pixel intensities like conventional methods. A fundamental advantage of mathematical morphology applied to signal processing is that it is intuitive since it works directly on the spatial domain: the structuring elements considered as the "basic bricks" play the same role as frequencies do in the analysis of the frequently used frequency filters. Another advantage is that it leads to better reproducible results because of the strong mathematical foundation. The simplicity in terms of computation and hardware implementation is also one of its main advantages. The last point that is worth noting lies in its capability in allowing easy customization of the program for the choice of every parameter according to physical measurements if necessary.

The diagram of the proposed algorithm is shown in Fig. 1. The proposed morphology operator filtering plays the most critical role in the proposed algorithm which removes the noise and baseline drift and suppresses the P/T waves in ECG signal. Then the multi pixel modulus accumulation is used to enhance the QRS complex. Finally, the threshold is applied to decide the heart rate. The detailed discussions on each section in Fig. 1 are presented in the following subsections. The standard MIT/BIH ECG database and our own wearable ECG data are used to demonstrate the superiority of proposed QRS detector.

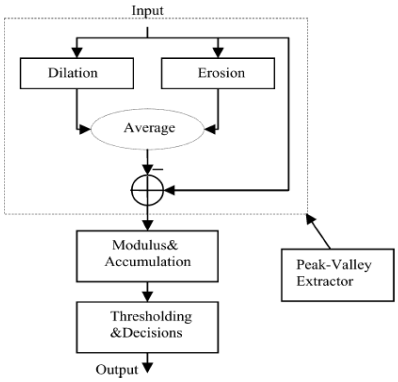


Figure 1: QRS Detection Algorithm

3.1 Morphological Filter

Now intuitively, dilation expands an image object and erosion shrinks it. The opening smoothes a contour in an I mage, breaking narrow isthmuses and eliminating thin protrusions. Closing tends to narrow smooth sections of contours, fusing narrow breaks and long thin gulfs, eliminating small holes, and filling gaps in contours. In most applications, opening is used to suppress peaks while closing is used to suppress pits. Here, in order to detect QRS complex accurately and quickly, a peak extractor is defined only based on basic dilation and erosion morphological operators, instead of a series of advanced openings and closings as in existing literature. It can be written as

$$h(n)=\frac{1}{2}[f\oplus g(n)+f\ominus g(n)]$$

$$v(n)=f(n)-h(n)$$

For the ECG signal that processed by this morphology filter, the QRS complex will be enhanced and others waves that change smoothly will be mapped in horizontal axis after the cancellation of dc components. The least significant item is the amplitude of the structure item, which the filter performance is the least sensitive to. Hence, in our selections, more considerations are given in terms of the tradeoff between computational complexity, effectiveness, and amplitude of resulted signal when determining the parameters of structure element. Considering the simplicity and similar shape, we select the triangle structure element by the optimization, defined as

$$G(K)=\begin{cases} 2A*\frac{K}{L+1}, & K<L/2 \\ 2A*(1-\frac{K}{L+1}) & K\geq L/2 \end{cases}$$

Here we choose L=11 and hence the G(k) = [0.2,0.4,0.6,0.8,1,1.2,1,0.8,0.6,0.4,0.2]

3.2 Modulus and Combination

The absolute value of the above output is then combined by multiple-frame accumulation, which is much like an energy transformation. The energy accumulation process is expressed as

$$S(n)=\sum_{i=n-\frac{\omega}{2}}^{n+\frac{\omega}{2}} v(i)$$

The value of should correspond to the possible maximum duration of normal QRS complex. This step further enhances the filtered ECG signal to make QRS peaks easy to identify.

3.3 Threshold and Decisions

An adaptive threshold is used as the decision function in connection with the proposed transformation for QRS detection. Usually, the threshold levels are computed signal dependent such that an adaption to changing signal characteristics is possible. The guideline in selecting the threshold, is given by

$$T=\begin{cases} .1\,Max, Max<3 \\ .3Max, 3\leq Max\leq 7 \\ .13\,Max, Max>7 \end{cases}$$

where Max is determined from the current signal segment which is within the range of mill ivolts. The upper and lower bounds of Max will be subject to the selection of structure elements.

4. Delay and Area Evaluation Methodology of Regular CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 2. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 3. in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

1) The group2 [see Fig. 3(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the

arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than s3[time(t)=8] and later than s2[t=6] Thus, sum3 [t=11] is summation of s3 and mux[t=3] and sum2[t=10] is summation of c1 and mux.

Table 1: Delay and Area Count Of Basic Blocks Of CSLA

Adder Block	*Delay*	*Area*
XOR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows

{c6,sum[6:4]} =c3[t=10] + mux
{c1o,sum[10:7]} =c6[t=13] + mux
{count,sum[15:11]} =c10[t=16] + mux

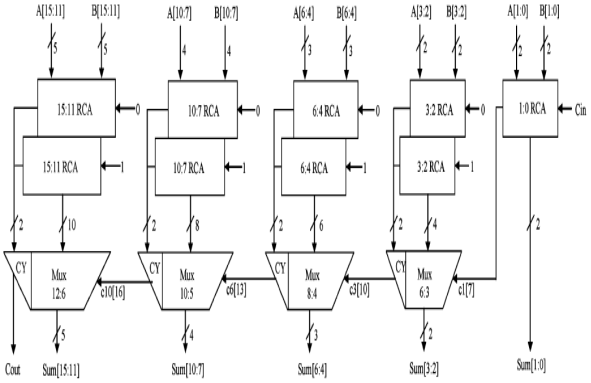


Figure 2: 16 bit CSLA

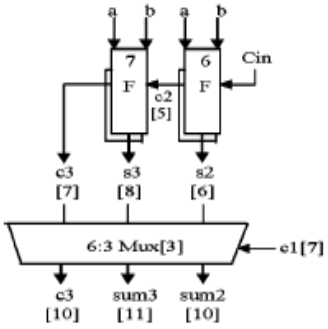


Figure 3: (a)

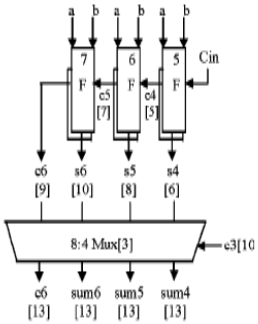


Figure 3 : (b)

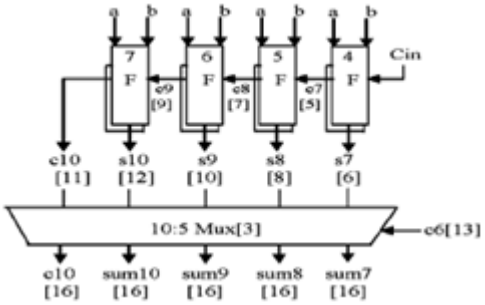


Figure 3: (c)

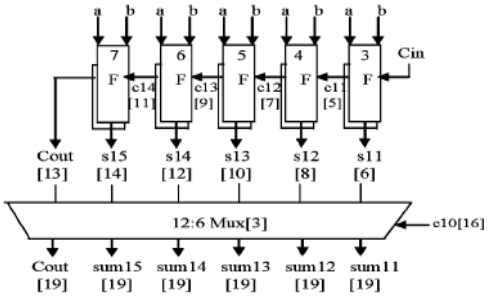


Figure 3: (d)

Figure 3: Delay and area evaluation of regular CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder.

3) The one set of 2-b RCA in group2 has 2 FA for Cin =1 and the other set has 1 FA and 1 HA for Cin=0. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

Gate count=57(FA+HA+mux)
FA=39(3*13)
HA=6(1*6)
MUX=12(3*4)

4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in

Group	Delay	Area
Group 2	11	57
Group 3	13	87
Group 4	16	117
Group 5	19	147

Table 2: Delay and Area of CSLA

5. Delay and Area Evaluation Methodology of Modified 16-BIT CSLA

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 5. The steps leading to the evaluation are given here.

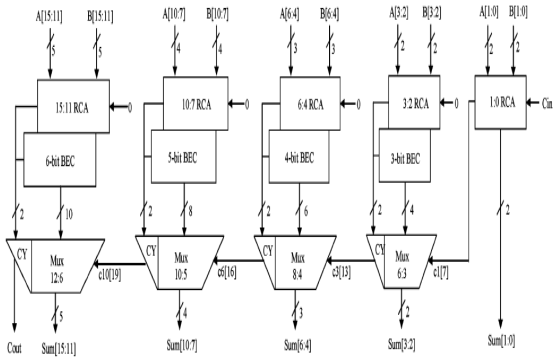


Figure 4: Modified 16 bit CSLA

1) The group2 [see Fig. 5(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin=0. Instead of another 2-b RCA with Cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time (t=7)] of 6:3 mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4] .Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group2 is determined as follows:

Gate count =43(FA+HA+MUX+BEC)
FA=13(1*13)
HA=6(1*6)
AND=1
NOT=1
XOR=10(2*5)
MUX=12(3*4)

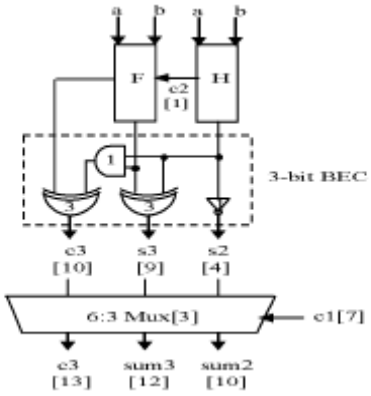


Figure 5: (a)

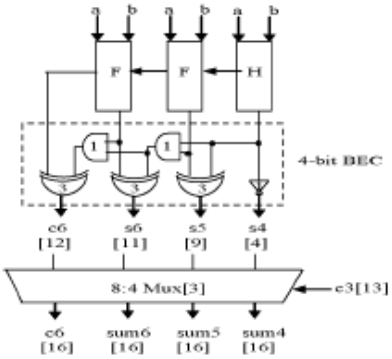


Figure 5 (b)

4) Similarly, the estimated maximum delay and area of the other groups of the III modified SQRT CSLA are evaluated and listed in Table. Comparing Tables II and III, it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

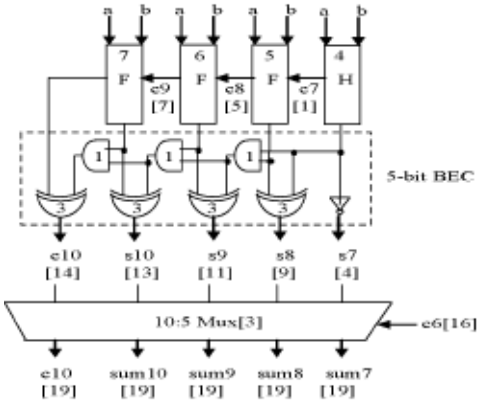


Figure 5: (c)

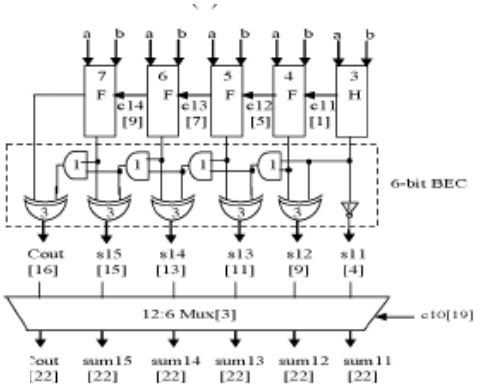


Figure 5: (d)

Figure 5: Delay and area evaluation of modified CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. H is a Half Adder.

Table 3: Delay and Area of Modified CSLA

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

Comparing Tables II and, III it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

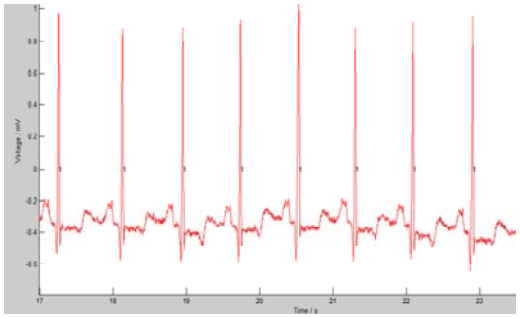
6. Experimental Results

The ECG signal obtained from the MATlab is used for the evaluation of the proposed QRS detection algorithm. It clearly demonstrates that the T wave will be eliminated after the mathematical morphology processing. It is intuitively challenging when the T waves or noise spikes are similar in duration as the QRS complexes. How accurate this algorithm is will be a topic of interest when the QRS duration is not sufficiently different from width of the other waves or any noise spikes. Since it would be helpful to show results of these "corner" cases for universal morphology technology, active data collection and searching have been undergoing to obtain such ECG signals for evaluating the proposed algorithm although it needs trial and error. To fully evaluate the performance of detection algorithm, several indexes are introduced including false negative (FN) which means failing to detect a true beat, and false positive (FP) which represents a false beat detection. By using FN and FP, the sensitivity (Se), positive prediction (+p) and detection error rate (DER) can be calculated using the following equations, respectively.

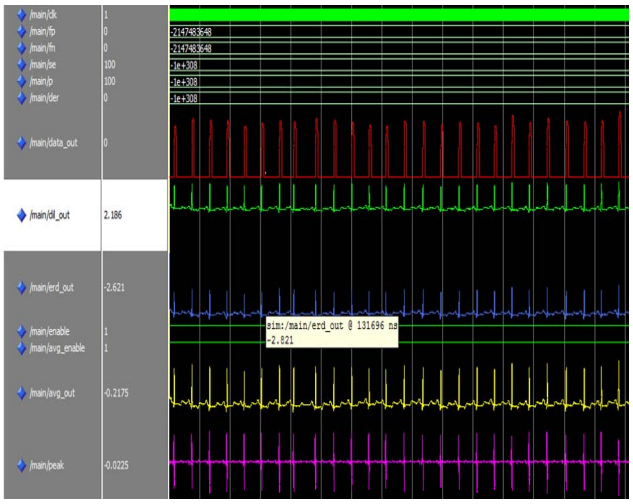
$$Se(\%) = \frac{TP}{TP+FN}$$

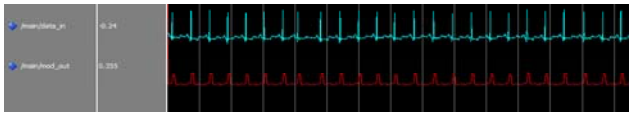
$$+P(\%) = \frac{TP}{TP+FP}$$

$$DER(\%) = \frac{FP+FN}{Total\ QRS}$$



Simulated Output





Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	3,493	7,168	48%
Number of 4 input LUTs	2,955	7,168	41%
Logic Distribution			
Number of occupied Slices	2,114	3,584	58%
Number of Slices containing only related logic	2,114	2,114	100%
Number of Slices containing unrelated logic	0	2,114	0%
Total Number 4 input LUTs	2,956	7,168	41%
Number used as logic	2,955		
Number used as a route-thru	1		
Number of bonded IOBs	34	97	35%
IOB Flip Flops	17		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	46,488		
Additional JTAG gate count for IOBs	1,632		

Synthesis Report of Area Consumed for the Modified System

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,830	7,168	25%
Number of 4 input LUTs	3,925	7,168	54%
Logic Distribution			
Number of occupied Slices	2,616	3,584	72%
Number of Slices containing only related logic	2,616	2,616	100%
Number of Slices containing unrelated logic	0	2,616	0%
Total Number 4 input LUTs	4,077	7,168	56%
Number used as logic	3,925		
Number used as a route-thru	152		
Number of bonded IOBs	34	97	35%
IOB Flip Flops	3		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	39,390		
Additional JTAG gate count for IOBs	1,632		

Power Summary:	I(mA)	P(mW)
Total estimated power consumption:		**63**
Vccint 1.20V:	**21**	**26**
Vccaux 2.50V:	**15**	**38**
Vcco25 2.50V:	**0**	**0**
Clocks:	**6**	**7**
Inputs:	**0**	**0**
Logic:	**0**	**0**
Outputs:		
Vcco25	**0**	**0**
Signals:	**0**	**0**

Power Report of Existing System

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		56
Vccint 1.20V:	15	18
Vccaux 2.50V:	15	38
Vcco25 2.50V:	0	0
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0

Power Report of Modified System

7. Conclusion

This paper has presented a VLSI friendly morphology based algorithm for both resting and wearable exercise ECG QRS detection in BSNs. Unlike the frequency based methods, the proposed method is free of the requirements of prior frequency knowledge of signal component of interest. Also the method can also work in case of the bandwidth overlaps between QRS complex and other components. The algorithm is implemented in FPGA and evaluated with MIT/BIH standard ECG database to achieve, a sensitivity of 100% and a positive prediction of 100%. And it is also effectively verified with our exercise ECG data with lower SNR. Also the power and area of the modified system will be less than that of the existing system.The area consumed by the existing system is 46,488 and the power consumption is 63(Mw) whereas the area consumed by the modified system is 39,390 and the power consumption is 56(Mw).

References

[1] F. Zhang and Y. Lian, “Effective ECG QRS detection based on multiscale mathematical morphology filtering,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 4, pp. 220–228, Aug. 2009.
[2] F. Zhang and Y. Lian, “Novel QRS detection by CWT for ECG sensor,” in Proc. Int. Conf. IEEE Biomed. Circuits Syst., Montreal, ON, Canada, Nov. 2007.
[3] J. Hu and S. Bao, “An approach to QRS complex detection based on multiscale mathematical morphology,” in Proc. 3rd IEEE Int. Conf. Biomed. Eng. Inform. (IEEE BMEI 2010), 2010, p. 725.
[4] B. Ramkumar and Harish M Kittur “Low-Power and Area-Efficient Carry Select Adder” ieee transactions on very large scale integration (vlsi) systems, vol. 20, no. 2, february 2012
[5] B. Ramkumar, H.M. Kittur, and P. M. Kannan, “ASIC implementation of modified faster carry save adder,” Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.

Author Profile

Chinchu Venugopal was born in Alapuzha, Kerala, India. She has received her B.E degree in Electronics and Communication Engineering from Anna University, Thirunelveli, India and pursuing M. Tech in VLSI &Embedded System from Mahatma Gandhi University, Kerala, India.