Implementation of Low Power Test Pattern Generator Using LFSR

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Abstract: ***In our project, we propose a novel architecture which generates the test patterns with reduced switching activities. LP-TPG (Test pattern Generator) structure consists of modified low power linear feedback shift register (LP-LFSR), m-bit counter; gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive–OR ed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns. The proposed architecture is simulated using Modelsim and synthesized using Xilinx ISE 13.2 and it will be implemented on XC3S500e Spartan 3E FPGA board for hardware implementation and testing. The Xilinx Chip scope tool will be used to test the FPGA inside results while the logic running on FPGA.***

Keywords: FPGA, BIST, LP-LFSR, Switching activity

1. Introduction

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power dissipation. Power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing

The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. For example, the platform FPGAs such as Xilinx Virtex II Pro and Altera Excalibur include custom designed fixed programmable processor cores together with millions of gates of reconfigurable logic devices.

In addition to this, the development of Intellectual Property (IP) cores for the FPGAs for a variety of standard functions including processors, enables a multimillion gate FPGA to be configured to contain all the components of a platform based FPGA. Development tools such as the Altera System-On-Programmable Chip (SOPC) builder enable the integration of IP cores and the user designed custom blocks with the Nios II soft-core processor. Soft-core processors are far more flexible than the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test. The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to1. During switching, the power is consumed due to the short circuit current flow.

Four reasons are blamed for power increase during test:

- High-switching activity due to nature of test patterns,
- Parallel activation of internal cores during test,
- Power consumed by extra design-for-test (DFT) circuitry,
- Low correlation among test vectors.

The power dissipation of a system in test mode is more than in normal mode. Low correlation between consecutive tests happens when applying low correlated patterns to scan chains. Increasing switching activity in scan chain results in increased power consumption in scan chain and combinational block. This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Different types of techniques are presented in the literature to control the power consumption. These mainly includes algorithms for test scheduling with minimum power, techniques to reduce average and peak power, techniques for reducing power during scan testing and BIST(built-in-self- test)technique. Since off-chip communication between the FPGA and a processor is bound to be slower than on- chip communication, in order to minimize the time required for adjustment of the parameters, the built in self test approach using design for testability technique is proposed for this case.

The rest of the paper is organized as follows. In section II, previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test

(CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII the results which are presented. Section VIII summarizes the conclusion.

2. Review of Previous Work

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. For linear feedback shift register (LFSR), Giard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched. S.K. Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce the average and peak power of a circuit during test. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used to generate random single input charge sequences .it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5],it is proposed that 2^m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

2.1 Analysis of Power for Testing

Power in electronic devices is defined as the conversion of electrical energy of power supply to heat. Equation (1) represents the power dissipation in electric circuits [9].

P=V.I (1)

Where:

V = Voltage (Joules/Coulomb or Volts)

I = Current (Coulombs/Sec or Amperes)
P = Power (Joules/Sec or Watts)

CMOS technology is the best choice for low-power designs because of its insignificant static power dissipation. However, simply selecting CMOS technology should not be considered as the only method for reducing power in ASIC/SOC devices. Since most of today's designs are based on CMOS technology, the first step toward power reduction is to understand the sources of power dissipation in such devices. Power consumption sources in digital CMOS circuits are divided into three main categories:

- Static power dissipation
- short-circuit power dissipation
- Dynamic power dissipation

Equation (2) illustrates the relationship between these three parameters.

$P_{Average}=P_{Static}+P_{Dynamic}+P_{Short\ circuit}$ (2)

CMOS devices have very low-static power dissipation and most of the energy in them is used to charge and discharge load capacitances. By comparison, the short-circuit and static powers are usually of smaller magnitude than the dynamic power, and they can be ignored. Therefore, dynamic power is the principal source of power dissipation in CMOS devices. The following sections explain each of these power dissipation sources in detail.

2.2 Static Power Dissipation

Static power dissipation occurs when the logic-gate output is stable; thus it is frequency independent.

$P_{Static}=V_{DD}.\ I_{leakage}$ (3)

2.3 Short-Circuit Power Dissipation

Short-circuit power dissipation occurs when current flows from power supply (VDD) to ground (GND) during switching. The value of short-circuit dissipation depends on the amount of short- circuit current flowing to GND.

$P_{Short\ Circuit}=V_{DD}.\ I_{Short\ Circuit}$ (4)

2.4 Dynamic Power Dissipation

Dynamic power is the dominant source of power dissipation in CMOS devices and accounts for approximately 90 percent of overall CMOS power consumption. It occurs during the switching of logic gates, and as a result, this type of power dissipation is frequency dependent. Dynamic power is therefore the average power required to perform all the switching events across the circuit.

$P_{Dynamic}=.\ \beta.\ C.\ V_{DD}^2.\ F$ (5)

Where:

β = Switching Activity per node
C = Switched Capacitance
F = Frequency (switching events per second)
V_{DD} = Supply Voltage

Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E_i=\frac{1}{2}V_{dd}^2C_0F_iS_i \quad (6)$$

Where V_{dd} is the supply voltage, C0 is the load capacitance. The product of Fi and Si is called weighted switching activity of internal circuit node i.

The average power consumption of internal circuit node i can be given by,

$$P_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i f \quad (7)$$

f is the clock frequency. The summary of Pi of all the nodes is named as average power consumption. It can be observed from (6) and (7) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.

A.BIST Approach:

Built-In Self-Test (BIST) has emerged as a promising solution to the VLSI testing problems. BIST is a DFT methodology aimed at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as improved testability, at-speed testing and reduced need for automatic test equipment (ATE).

In BIST, a linear feedback shift register (LFSR) generates test patterns and a multiple input shift register MISR) compacts test responses. Test vectors applied to a circuit under test at nominal operating frequency may have more average and/or peak power dissipation than those in normal mode. The reason is that the random nature of patterns reduces the correlation between the pseudorandom patterns generated by LFSR compared to normal functional vectors. It results in more switching and power dissipation in test mode

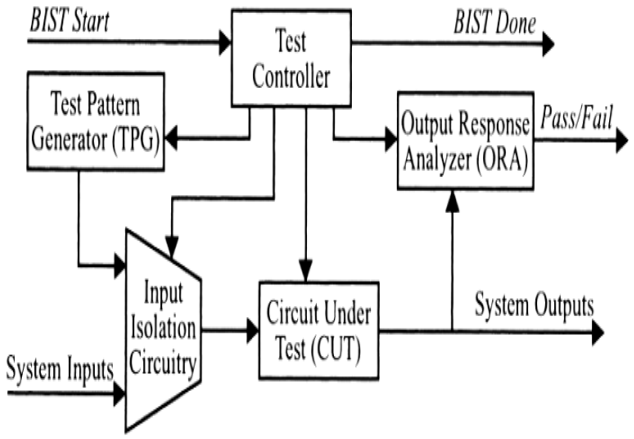

Figure 1: BIST basic block diagram

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks.

BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR].The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation. It causes excessive power dissipation and results in delay penalty into the design.

B. Classification of test strategies:

1. **Weighted Pseudorandom Testing:** In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.
2. **Pseudo exhaustive Testing:** Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.
3. **Pseudorandom Testing:** Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.
4. **Exhaustive Testing:** Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT).It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.
5. **Stored Patterns:** Stored-pattern approach tracks the pre-generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

3. Design of Multiplier

Multipliers are widely used in DSP operations such as convolution for filtering, correlation and filter banks for multi rate signal processing. Without multipliers, no computations can be done in DSP applications. Multipliers are one the most important component of many systems. So we always need to find a better solution in case of multipliers. Our multipliers should always consume less power and cover less power. For that reason, multipliers are chosen for testing in our proposed design. Shift-add multiplier is selected among various multipliers as it follows simple conventional method. We are going to implement 4x4 and 8x8 multiplier by taking corresponding input from the 4bit and 8 bit LP-test pattern generators.

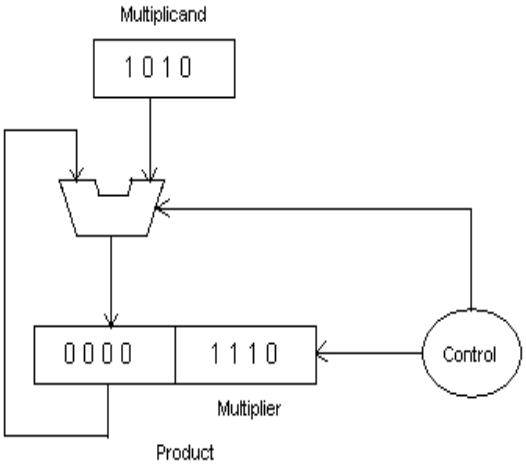

Figure 2: Block diagram for Shift-add Multiplier

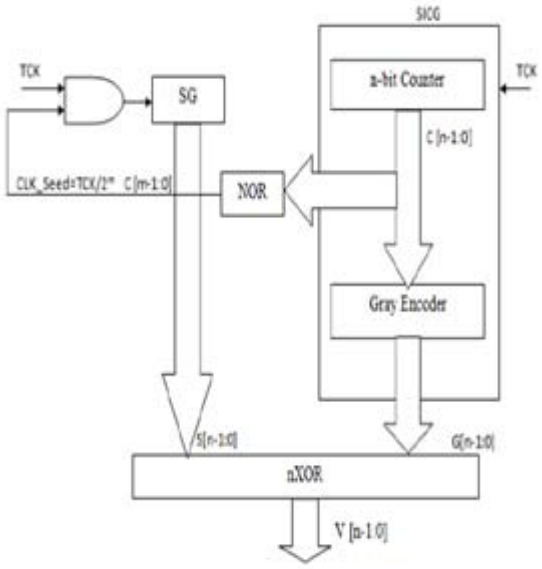

Figure 3: Low Power Test Pattern Generator

4. Proposed Method

LFSR is widely used as test pattern generator because of its small circuit area and excellent random characteristics. Modified LFSR is used as the seed generator in this paper. Low Power TPG consists of a seed generator (SG), an n-bit counter, a gray encoder and an exclusive-OR array. The n-bit counter and gray encoder generate single input changing patterns. The m-bit counter is initialized with Zeros and which generates 2^m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The seed generated from LP-LFSR is Exclusive–OR ed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

5. Algorithm for LP-LFSR

According to proposed structure of LP-TPG C [n-1:0] is the counter output and G [n-1:0] is the gray encoder output. The counter and SG are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates 2n continuous binary data periodically. The output of NOR operation of C [m-1:0] will be the clock control signal of SG where m<=n. It can be found obviously that SG will generate the next seed only when C[m-1:0] are all „0's and NOR output changes to „1's. The period of the single input changing sequences will be 2m.

Gray encoder in Fig. 1 is used to encode the counters output C[n-1:0] so that two successive values of its output G[n-1:0] will differ in only one bit. Gray encoder can be implemented by following equations.

G [0] = C [0] XOR C [1]
G [1] = C [1] XOR C [2]
G [2] = C [2] XOR C [3]
…….
G [n-2] = C [n-2] XOR C [n-1]
G [n-1] = C [n-1]

The seed generating circuit SG is a modified LFSR which is the combination of a Type-II LFSR and several XOR gates. The theory stated that the conventional LFSR's outputs can't be taken as the seed directly, because some seeds may share the same vectors. So the seed generator circuit should make sure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. The final test patterns are implemented as following equations.

V [0] = S [0] XOR G [0]
V [1] = S [1] XOR G [1]
V [2] = S [2] XOR G [2]
…
V [n-1] = S [n-1] XOR G [n-1]

The SG's clock will be TCK/2m due to the control signal. As SICG's cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too. Table 1 is an example of 4 bit single input changing sequence with the seed S0 "0000" and with the seed S1 "0101" when n=4 and m=3. The period of the single input changing sequences will be 8. 4-bit gray encoder output sequence in Table I is {0000, 0001, 0011, 0010, 0110, 0111… 1000}. The chosen seeds S0 and S1 are {0000} and {0101}. S0 will be exclusive-ORed with

sequence {0000, 0001, 0011 … 0100} and generates the SICG single input changing sequence {0000, 0001, 0011, 0110, 0111, 0101, 0100}, S1 will be exclusive-ORed with sequence {1100, 1101, 1111 …1000} and generates the SICG single input changing sequence {1001, 1000, 1010, 1011, 1111, 1110, 1100, 1101}. As an example, two well chosen seeds guarantee two single input changing sequences are unique.

Table 1: An example of 4 bit Single input change sequence (N = 4, M = 3)

S0 = 0000	*S1 = 0101*
V0 = 0000	V8 = 1001
V1 = 0001	V9 = 1000
V2 = 0011	V10 = 1010
V3 = 0010	V11 = 1011
V4 = 0110	V12 = 1111
V5 = 0111	V13 = 1110
V6 = 0101	V14 = 1100
V7 = 0100	V15 = 1101

6. Results and Discussion

3.1 Simulation Results:

The following chapter consists of all the software and hardware results observed in the project. The results include snapshots of top module with the inputs, outputs and intermediate waveforms**.**

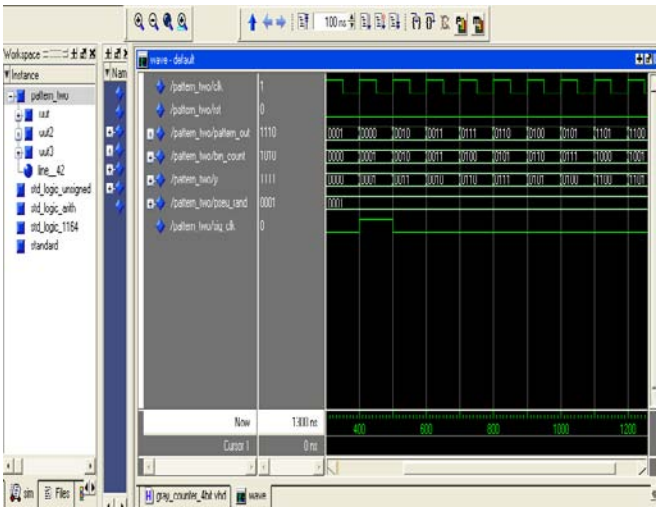

Figure 4: LP-Test pattern Generator Results

3.2 Chipscope Results

Chipscope is an embedded, software based logic analyzer. By inserting an “integrated controller core” (icon) and an “integrated logic analyzer” (ila) into your design and connecting them properly, you can monitor any or all of the signals in your design. Chipscope provides you with a convenient software based interface for controlling the “integrated logic analyzer,” including setting the triggering options and viewing the waveforms. Below Figure shows a block diagram of a Chipscope Pro system. Users can place the ICON, ILA, VIO, and ATC2 cores (collectively called the Chipscope Pro cores) into their design by generating the cores with the Core Generator and instantiating them into the HDL source code. We can also insert the ICON, ILA, and ATC2 cores directly into the synthesized design net list using the Core Inserter tool. The design is then placed and routed using the ISE 9.2i implementation tools. Next, we download the bit stream into the device under test and analyze the design with the Analyzer software.

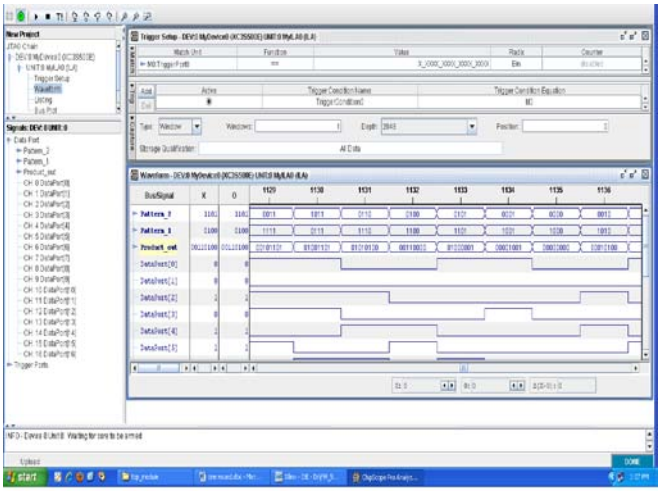

Figure 5: Chipscope results for 4 bit Pattern Generator

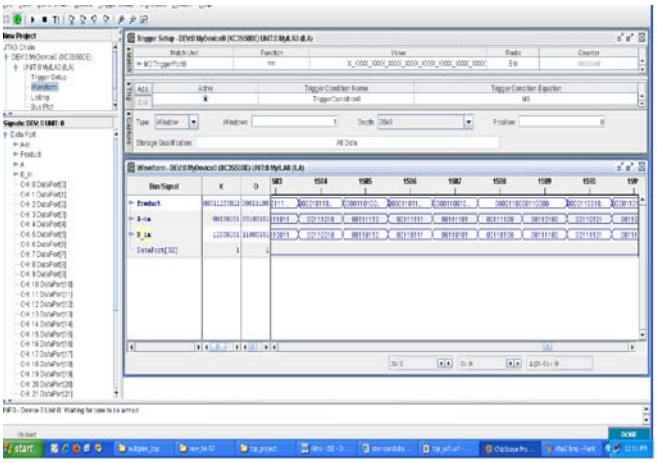

Figure 6: Chipscope results for 8 bit Pattern Generator

7. Conclusion

An efficient low power test pattern generator (LP-TPG) method had been proposed to reduce the test power and uses a modified pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus pseudo-random signal input changing sequences are generated, which greatly minimize circuit switching activities and test power. LP-TPG also reduces the instantaneous power violation compared to conventional LFSR.

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