

Finite Impulse Response (FIR) Filter Design using Canonical Signed Digits (CSD)

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Abstract : *In the presented work, it is proposed to design and analyze a high order FIR filter based on canonical signed digits representation of coefficients in order to minimize the power consumption and fast implementation of the filter. The designed FIR filter is proposed to implement using MATLAB tool and to be tested on high speed communication signal. Although a few works addressed the problem of reducing the complexity of coefficient multipliers in reconfigurable FIR filters, hardly any work demonstrated reconfigurability in higher order filters. Moreover, it is observed that there is sufficient scope for more work on complexity reduction in reconfigurable filters especially for wireless communication applications where higher order filters are often required to meet the stringent adjacent channel attenuation specifications. The CSD based computation and selection of filter coefficients for higher order FIR filters has been identified as a problem to solve in the presented work. An additional approach is proposed i.e. factored canonical signed digits based coefficients computation that serves a great purpose while reducing the power consumption in FIR filter design, the main filter design, selection and implementation parameter.*

Keywords: CSD → Canonical Signed Digits, FIR → Finite Impulse Response

1. Introduction

FIR digital filters find extensive applications in mobile communication systems for applications such as channelization, channel equalization, matched filtering, and pulse shaping, due to their absolute stability and linear phase properties. The filters employed in mobile systems must be realized to consume less power and operate at high speed. Recently, with the advent of software defined radio (SDR) technology, finite impulse response (FIR) filter research has been focused on reconfigurable realizations. The fundamental idea of an SDR is to replace most of the analog signal processing in the transceivers with digital signal processing in order to provide the advantage of flexibility through reconfiguration. This will enable different air-interfaces to be implemented on a single generic hardware platform to support multi standard wireless communications [1]. Wideband receivers in SDR must be realized to meet the stringent specifications of low power consumption and high speed. Reconfigurability of the receiver to work with different wireless communication standards is another key requirement in an SDR.

Processing of data quick enough to achieve real-time performance is a highly power-consuming task. Data is transferred through a network and filtered through filters containing multiplications and/or additions. The power consumed in such a filter is directly related to how many times multiplications or additions must be done. In this thesis the focus is on one-dimensional Finite Impulse Response (FIR) filters.

The FIR-filter's equation is given in equation.

$$Y(n) = \sum_{i=0}^{N-1} C_i * x_n - 1$$

where N is the number of taps (order), C_i is the coefficient of tap i, x_i is the input data samples and Y is the output of the filter.

2. Related Works

DSP multiplies of two's complement signals. CSD has always been considered a fixed-point system, and available conversion algorithms operate on integers. Using methods applicable to many simple number systems, we rederive CSD for fractional numbers, derive a simple floating-point recursion for converting fractions to CSD, and briefly examine the associated truncation error [1].

This paper presents an example filter design that shows the error involved in limiting the number of allowable non-zero CSD coefficients for a real FIR band pass filter. If not done carefully, brute force limiting can lead to large errors in the frequency response. The error is evaluated for varying numbers of non-zero CSD coefficients. Lastly, a system level architecture with a multiplier utilizing the properties of the CSD number representation system is proposed. [2]

Higher Radix CSD has been proposed for dramatic reduction of terms that must be combined. In this paper, we redefine CSD and Radix4 CSD as arithmetic codes. By defining these number representations using the well-known theory of arithmetic coding [3].

Reconfigurability and low complexity are the two key requirements of the SDR channelizers. Architecture for implementing low complexity and reconfigurable finite impulse response (FIR) filters for channelizers is proposed in this paper. Our method is based on the binary common sub-expression elimination (BCSE) algorithm. The synthesis results show that the proposed reconfigurable FIR filter can operate at high speed consuming minimum area and power. The average reductions in area and power are found to be 49% and 46% respectively with an average increase in speed of operation of 35% compared to other reconfigurable FIR filter architectures in literature [4].

The conversion to this code should however not limit the speed of the multiplier. We therefore propose a new conversion algorithm that combines two other algorithms to increase the conversion speed by almost a factor of two, compared with the other solutions. The algorithms, including ours, are implemented in VHDL and synthesized, which verifies that our solution can operate at nearly the double data rate compared with the other two algorithms [5].

The proposed FIR filter architecture is capable of operating for different word length filter coefficients without any overhead in the hardware circuitry. We show that dynamically reconfigurable filters can be efficiently implemented by using common sub expression elimination algorithms. The proposed architectures have been implemented and tested on Virtex 2v3000ff1152-4 field-programmable gate array and synthesized on 0.18 μm complementary metal-oxide-semiconductor technology with a precision of 16 bits. Design examples show that the proposed architectures offer good area and power reductions and speed improvement compared to the best existing reconfigurable FIR filter implementations in the literature [6].

In some cases, evolved circuits can have better performances, or they can be optimized with respect to different parameters. An example on design of a multi-rate digital filter with reduced power consumption is presented and discussed. FPGA implementation demonstrates that evolutionary design can lead to both area and power saving with respect to conventional design [7].

The theory is investigated via a case study, in which we present FPGA hardware mapping results which show that employing the proposed method results in a decrease of more than 70% in the logic gate count needed as compared to the conventional implementation [8].

A new CSE algorithm using binary representation of coefficients for the implementation of higher order FIR filters with a fewer number of adders than CSD-based CSE methods is presented in this paper. We show that the CSE method is more efficient in reducing the number of adders needed to realize the multipliers when the filter coefficients are represented in the binary form. Our observation is that the number of unpaired bits (bits that do not form CSs) is considerably few for binary coefficients compared to CSD coefficients, particularly for higher order FIR filters. As a result, the proposed binary-coefficient based CSE method offers good reduction in the number of adders in realizing higher order filters. The reduction of adders is achieved without much increase in critical path length of filter coefficient multipliers. Design examples of FIR filters show that our method offers an average adder reduction of 18% over the best known CSE method, without any increase in the logic depth [9].

By employing a span reduction technique, we show that the filter coefficients can be coded using considerably fewer bits than conventional 24-bit and 16-bit fixed-point filters. Simulation results show that the magnitude responses of the filters coded in PFP meet the attenuation requirements of wireless communication standard specifications. The proposed method offers average reductions of 40% in the

number of adders and 80% in the number of full adders needed for the coefficient multipliers over conventional FIR filter implementation methods [10].

Two new reconfigurable architectures of low complexity finite impulse response (FIR) filters for channelizers are proposed in this paper. Our methods are based on the binary common sub expression elimination (BCSE) algorithm. The proposed architectures are capable of operating at a high speed clock frequency of 109.7 MHz based on Xilinx's Virtex II 2v2000ff896-6 FPGA for a 12-bit FIR filter coefficient. Design examples show that our method offers an average reduction of 23% in the number of addition operations compared to the conventional FIR filter implementations [11].

3. Canonical Signed Digits

Encoding a binary number such that it contains the fewest number of non-zero bits is called canonic signed digit (CSD). Here, mapping a number to a ternary system $\{-1,0,1\}$ versus a binary system $\{0,1\}$ is done. The following are the properties of CSD numbers:

- No two consecutive bits in a CSD number are non-zero.
- The CSD representation of a number contains the minimum possible number of non-zero bits, thus the name canonic.
- The CSD representation of a number is unique.

Among the N-bit CSD numbers in the range $[-1,1)$, the average number of non-zero bits is $N/3 + 1/9 + O(2^{-N})$. Hence, on average, CSD numbers contains about 33% fewer non-zero bits than two's complement numbers. The conversion of W-bit number in $SW.(W-1)$ notation to CSD format is given as: $A = a'W-1. a'W-2... a'1 a'0 = 2$'s complement number and Its CSD representation is $aW-1. aW-2... a1 a0$.

4. Results

Following are the results after compiling and running the MATLAB code (ver. 7.5) for FIR filter:

```

Filter Order = 10
Filter Type = Low Pass Filter
Cutoff Freq. = 48 KHz
Pass Band Freq. = 9.6 KHz
Stop Band Freq. = 12 KHz.

Filter Coefficients when quantized as 16 bit integers:
* Discrete-Time FIR Filter (real)
1945   -3213   -3844   1217
10090  14618   10090   1217
-3844  -3213,   1945
    
```

A text file is generated of the same and can be viewed for implementing the filter on FPGA kit in order to test the no. of gates required to fabricate the filter.

5. MATLAB Implementation

The main code in MATLAB is given below:

```

for x=1:NoOfCoeff
    Coeff = num2str(b(x));
    ScaledCoeff = SCALING * b(x);
    t = dec2twos(ScaledCoeff,16);

    %***** CSD Computation %*****
    num=ScaledCoeff;
    targetNum=num;
    num=abs(num)/(2^(-resolution));
    if num~=floor(num)
        if floor(num)==0
            error('Insufficient precision to represent this number!')
        else
            warning('Some precision has been lost. Returned value is truncated!')
        end
    end
    num=floor(num);
    if num>(2^(range+resolution))
        error('Input number is too large for the requested bit representation.');
```

```

    end
    binNum=dec2bin(num,range+resolution);
    digits=('0'+0)*ones(size(binNum));
    %allZeros=allZeros;
    onesLoc=findstr(binNum,'1');
    if ~isempty(onesLoc)
        onesRun=find(diff(onesLoc)==1);
        while ~isempty(onesRun)
            onesPointer=find(diff(onesLoc)==1)+1;
            addIn=onesLoc(onesPointer:end);
            adder=('0'+0)*ones(size(binNum));
            adder(addIn)=('1'+0);
            digits(addIn)=('1'+0);
            binAdder=char(adder);
            binNum=dec2bin(bin2dec(binNum)+bin2dec(binAdder),range+resolution);
            onesLoc=findstr(binNum,'1');
            onesRun=find(diff(onesLoc)==1);
            if length(binNum)>length(digits)
                digits=['0'+0,digits]; % add any additional leading zero
            end
            end
            end

            pos=bin2dec(binNum)*2^(-resolution);
            negLoc=find(digits=='-1'+0);
            neg=('0'+0)*ones(size(binNum));
            neg(negLoc)='1'+0;
            neg=bin2dec(char(neg))*2^(-resolution);
            digits(onesLoc)='+1'+0;
            if (length(digits)-resolution)>range
                warning('Number overflowed for this CSD representation')
            end
            if length(digits)<resolution
                digits=[digits,('0'+0)*ones(1,resolution-length(digits))];
            end
            digits=char([digits(1:length(digits)-resolution),'+1'+0,digits(length(digits)-resolution+1:end)]);
            if targetNum<0 % flip representation if negative
                ntemp=neg;
                neg=pos;
                pos=ntemp;
            digits=strrep(digits,'+','p');
            digits=strrep(digits,'-','+');
            digits=strrep(digits,'p','-');
            end
end
end

```

6. Conclusion

Although a few works addressed the problem of reducing the complexity of coefficient multipliers in reconfigurable FIR filters, hardly any work demonstrated reconfigurability in higher order filters. Moreover, it is observed that there is sufficient scope for more work on complexity reduction in reconfigurable filters especially for wireless communication applications where higher order filters are often required to meet the stringent adjacent channel attenuation specifications. The CSD based computation and selection of filter coefficients for higher order FIR filters has been identified as a problem to solve in the presented thesis work.

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