Low Power 8 bit Analog to Digital Converter (ADC) in 180 nm CMOS Technology

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Abstract: ***Analog to Digital Converter (ADC) is developed for operating at ultra low supply voltages. Circuit is realized in 180 nm CMOS technology. The pre-simulation of ADC has been achieved on Caadence Virtuos. The purpose of this work is to develop a biomedical application. The research is focused on the design of ADC with sampling rate 100KS/s. It has very low cost and high speed technology with relative medium resolution and accuracy. This implies it possesses a good tradeoff between speed and cost. R2R DAC is used with a different approch in which matching of resistors is easier than a conventional ADC.***

Keywords: Cadence, CMOS, DAC, Sampling rate, VLSI

1. Introduction

For different application such as wireless communication and digital audio and video and biomedical application have created need for effective data converter which have high speed and accuracy. There are different type of architecture each with unique characteristics and limitations.

There are many different architectures like pipelined convertor [1], successive approximation convertor, Sigma-Delta convertor, folding ADC's, reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper a simple technique for enhancing conversion of successive approximation ADC is proposed. Fig 1 shows a general block diagram of ADC.

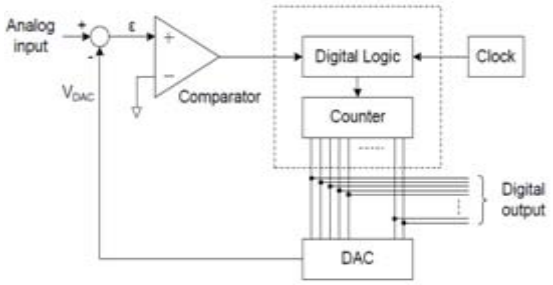

Figure 1: General block diagram of ADC

2. Previous Work

Many designs have evolved from conventional ADCs. The TIQ technology has been used to design a flash ADC. Focus is on low voltage and high speed design. In 2002 an average termination circuit was proposed [2] which help in reducing over range amplification.

1.13W SAR ADC was proposed which have binary scaled error compensation.

3. Architecture Description

Figure 2 explains the scheme of analog to digital converter. The basic building blocks of the entire system are
1. R-2R DAC
2. ADC Control
3. Comparator

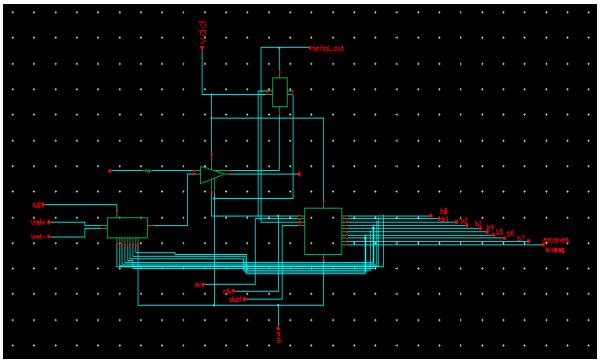

Figure 2: Schematic diagram of ADC in Cadence Virtuoso

3.1 High Speed CMOS Comparator

Comparators are known as 1-bit analog to digital converter and for that reason they are used in abundance. First sample signal is given to comparator [4]. The conversion speed of comparator is limited by response time of comparator. Figure 3 describes the circuit diagram of the comparator.

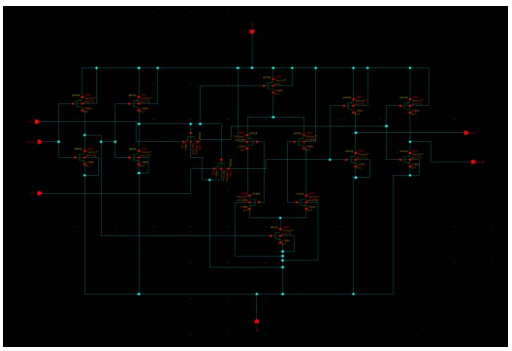

Figure 3: Schematic diagram of Comparator in Cadence Virtuoso

It consists of three stages
a) Input stage
b) Flip Flop or Pre Amplifier stage
c) SR Latch

Pre Amplifier consists of four transistors [3] while input differential pair uses two nmos transistors and load transistor uses pmos transistor. The Gain of pre amplifier easily reaches an acceptable value. Most sensitive part of comparator design is latch. It has two inverters connected in

a back to back fashion and nmos transistor is connected between the nodes of the latch. For least capacitive effect the transistor of latch must have minimum length and an ideal W/L ratio for inverter. The width of a transistor affects the result of latch. When clock goes high amplifier disables and the latches amplify the difference obtained by the input transistor to generate logic level at output.

3. 2 R2R DAC

The binary weighted input DAC (Digital to analog converter) is alos known as R-2R DAC [5] which uses unique values of resistor. Formal DAC design requires several different precious input resistor values. This is the main drawback of a conventional DAC. Figure 4 shows the schematic of an R-2R DAC.

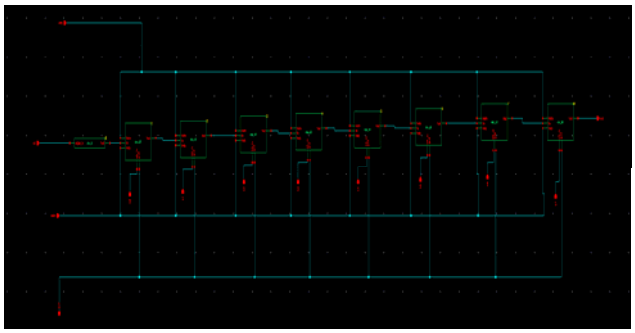

Figure 4: Schematic diagram of an R-2R DAC in Cadence Virtuoso

As the name suggests the R-2R uses an array of registers of value R and 2R. The DAC employs registers, cmos switches and a buffer amplifier. The number of registers required is 2N+1. The buffer has to be designed carefully to allow the input to be linearly amplified.

3.3 ADC Control

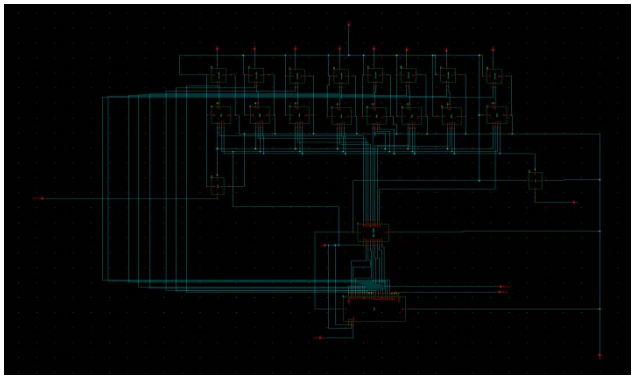

Figure 5: Schematic diagram of an ADC control in Cadence Virtuoso.

The ADC control constitutes of various components.

3.1.1 Shift circuitry

It consists of a NAND gate, NOR gate, D flip-flop and a combinational circuit consisting of a multiplexer whose output serve as an input to a D flip-flop.

3. 1.2 RegLH

RegLH consists of two independent devices, nmos and pmos and two inverters. The input is connected to the drain of the pmos. Gates of both the devices receive a common clock pulse. The drain of the nmos is connected to the source of the pmos. The output is taken from between the nmos and pmos. This ouput acts as an input to the buffer. Eight RegLHs are making up the ADC Ctrl Ccircuit.

3. 1.3 ADC Ctrl

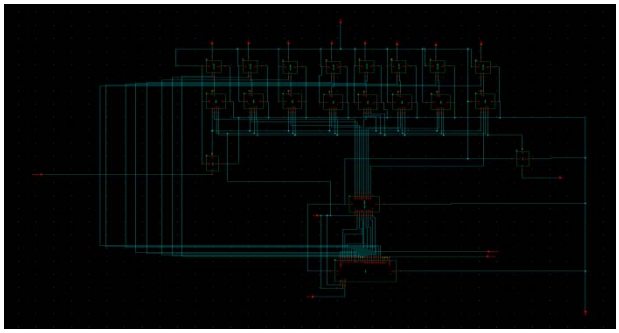

Figure 6: Schematic diagram of an ADC Ctrl.

4. Conclusion

Design and simulation of an 8-bit ADC using 180nm CMOS technology has been presented. Design is suitable for low voltage (0.6Vdd) and high speed (2 GS/sec). System on Chip Application (SoC). Average power consumed is 6.45 microWatt. Thus we have achieved a successful design of a high speed low power consuming eight-bit ADC.

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