Simulation of Multi Converter Unified Power Quality Conditioner for Two Feeder Distribution System

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Abstract: ***In this Project the Power Quality improvement is done for elimination of Sag, Swell and Harmonics for two feeder distribution system by using Multi Converter UPQC. In this system two series voltage source converters and one shunt voltage source converter exits. The system can be applied to adjacent feeder to compensate for supply voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeder. In this configuration all converters are connected back to back on the dc side and share common dc-link capacitor. Hence, Power can be transferred from one feeder to adjacent feeder to compensate Sag, Swell and Interruption. The performance of two feeder distribution system is studied using MATLAB/ SIMULINK.***

Keywords*:* Power Quality (PQ), Unified Power Quality Conditioner (UPQC), Voltage Source Converter (VSC).

1. Introduction

In the distribution system and Industries, Power Quality (PQ) problems such as Harmonics, Sag, Swell, Flickers and Interruptions have become serious concern due to increasing applications of Nonlinear and Electronically switched devices.

In the present scenario pure sinusoidal supply voltage is essential for proper load operation as the sensitive loads are involving Digital Electronics & Complex Process Controllers. To maintain pure sinusoidal supply for Power Quality improvement it is necessary to include some sort of compensation. A flexible AC Transmission system mainly includes Voltage and Current Compensating devises to improve the power quality of the system. The various types of FACTS Devices are mainly used for Compensation, Power Quality Improvement and to control the transmission system using the electronically switched devices. The Unified Power Quality Conditioner (UPQC) is the extinction of the Unified Power Flow Controller (UPFC) concept at distribution level. UPQC consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfection in a supply feeder.

2. Multi Converter UPQC System

In the two feeder distribution system, two different substations supply the loads L1 & L2.The Multi Converter UPQC consists of three VSCs which are connected in series with BUS1 & VSC2 is connected in shunt with load L1 at the end of the Feeder1.VSC3 is connected I series with BUS2 at the Feeder 2 end. The three voltage source converters are connected with a commutation reactor & high-pass output filter to prevent the flow of switching harmonics in to the supply.

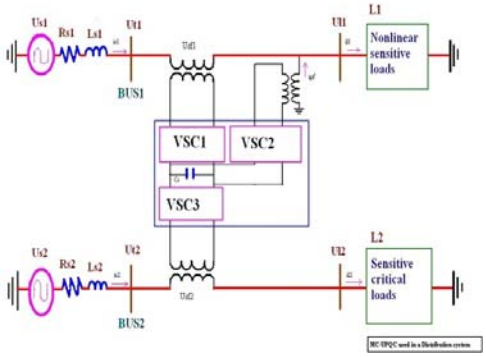

Figure 1: MC-UPQC in Distribution System

The Multi Converter UPQC is mainly used

1) To regulate the load voltage against sag/swell & disturbances in the system to protect the nonlinear/ sensitive load L1.
2) To regulate the load voltage against sag/swell, interruption & disturbances in the system to protect the sensitive critical load L2.
3) To compensate for the reactive & harmonic components of nonlinear load current.

In order to achieve the goals VSC1 & VSC3 operate as voltage controllers & VSC2 operate as a current controller. In fig.1, The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of u_{t1} and u_{t2}, respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of i_{l1}. Supply voltages are denoted by u_{s1} and u_{s2} while load voltages are u_{l1} and u_{l2}. Finally, feeder currents are denoted by i_{s1} and i_{s2} and load currents are i_{l1} and i_{l2}. Bus voltages u_{t1} and u_{t2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell and interruption.

3. Control Strategy

The Multi-Converter UPQC consists of two series voltage source converters & one shunt voltage source converter which are controlled independently. The series VSC operate on SPWM voltage control & shunt VSC operate on Hysteresis current control.

3.1 Series Voltage Source Converter

The main function of series voltage source converter
1) To eliminate voltage sag & swell.
2) To compensate for voltage distortions such as harmonics
3) To compensate for Interruption (In Feeder2 only).

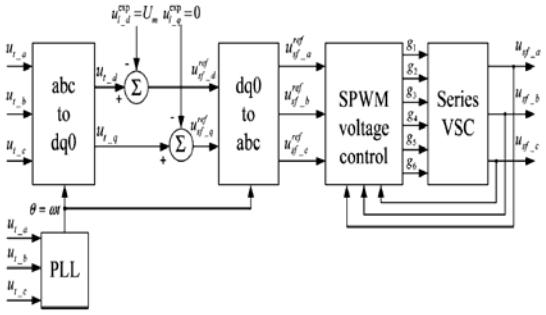

Figure 2: Series VSC Control Block.

The control block of each VSC is shown in fig.2. The bus voltage (Ut-abc) is detected and then transformed into the synchronous dqo reference frame using

$$u_{t\_dq0} = T_{abc}^{dq0} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{\text{th}}$$

Where utp1, ut1n and ut10 are fundamental frequency positive, negative, and zero-sequence components respectively and u^{th} is the harmonic component of the bus voltage. According to control objectives of the Multi Converter UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dqo reference frame only has one value.

$$u_{l\_dq0}^{\exp} = T_{abc}^{dq0} u_{l\_abc}^{\exp} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix}$$

Where the load voltage in the abc reference frame is

$$u_{l\_abc}^{\exp} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - 120°) \\ U_m \cos(\omega t + 120°) \end{bmatrix}$$

The Compensating reference voltage in the synchronous dqo reference frame is defined as

$$u_{\text{sf}\_dq0}^{\text{ref}} = u_{t\_dq0} - u_{l\_dq0}^{\exp}$$

This means ut1p-d in ut1p should be maintained at Um while all other unwanted components must be eliminated. The compensating reference voltage in usf-dqo is then transformed back into the abc reference frame. Hence by using SPWM voltage control technique, the output compensation voltage of the series VSC can be obtained.

3.2 Shunt Voltage Source Converter

The main functions of shunt VSC are
1) To compensate for the reactive component of load L1 current;
2) To compensate for the harmonic components of load L1 current;
3) To regulate the voltage of the common dc-link capacitor

In this measured load currents are transformed into synchronous dqo reference frame by using

$$i_{l\_dq0} = T_{abc}^{dq0}\, i_{l\_abc}$$

Where the transformation matrix is

$$T_{abc}^{dq0} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120°) & \cos(\omega t + 120°) \\ -\sin(\omega t) & -\sin(\omega t - 120°) & -\sin(\omega t + 120°) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

By this transform, the fundamental positive-sequence component, which is transformed in to dc quantities in the d and q axes, can be easily extracted by low-pass filters. Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{l\_d} = \bar{i}_{l\_d} + \tilde{i}_{l\_d}$$
$$i_{l\_q} = \bar{i}_{l\_q} + \tilde{i}_{l\_q}$$

Where il-d,il-q are d-q components of the load current and the rest are dc & ac components of the above equation

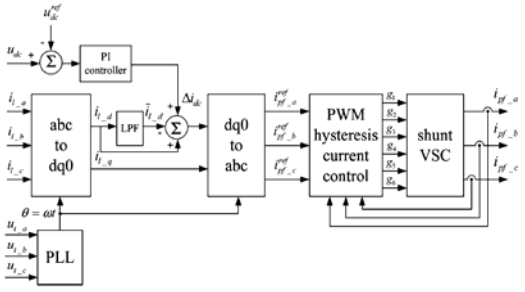

Figure 3: Shunt VSC Control Block

If is is the feeder current and ipf is the shunt VSC current and is=il-ipf, then d-q components of the shunt VSC reference current are defined as

$$i_{pf\_d}^{\text{ref}} = \tilde{i}_{l\_d}$$
$$i_{pf\_q}^{\text{ref}} = i_{l\_q}$$

Also, the d-q components of the feeder current are

$$i_{s\_d} = \bar{i}_{l\_d}$$
$$i_{s\_q} = 0$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of the load can also affect the dc link. In order to regulate the dc-link capacitor voltage, a PI controller is used in the shunt VSC control block. The input of the Pi controller is the error between the actual capacitor voltage and its reference value. The output of PI controller is added to the d component of the shunt-VSC reference

current to form a new reference current and it is transformed back into the abc reference frame. Hence by using PWM Hysteresis current control, the output compensating currents in each phase are obtained

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc} i_{pf\_dq0}^{ref}$$

4. Capacitor Design

Design of the DC side capacitor is based on the principle of instantaneous Power flow on the DC and AC side of the converter. The fluctuation due to the load change cannot be taken as a method for capacitor design. However, unlike the Voltage ripple caused by the load unbalance that the ripple must be suppressed by enlarging the capacitor value, the voltage control section will regulate this fluctuation caused by the load change. The magnitude of the voltage fluctuation depends on the closed loop response and can be made small by suitable design of the control parameters. For Voltage Source Converter the DC link voltage is given as

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m}$$

And the capacitor can be obtained as

$$C = \frac{m}{2w\Delta V_c} I_f$$

Where *m* is Modulation Index, w is Switching Frequency, If is Shunt Current and ΔVdc is Ripple value of Capacitor Voltage.

5. Simulation Results

5.1 Distortion and Sag/Swell on the BUS Voltage in Feeder-1 and Feedeer-2

Let us consider that the power system in Fig. 1 consists of two three-phase three-wire 380(v) (RMS, L-L), 50-Hz utilities. The BUS1 voltage (u_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage (u_{t2}) contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between 0.1s<t<0.2s and 20% swell between 0.2s<t<0.3s. The BUS2 voltage contains 35% sag between 0.15s<t<0.25s and 30% swell between 0.25s<t<0.3s. The nonlinear/sensitive load L1 is a three-phase rectifier load which supplies an RC load of 10Ω and 30μF. The Simulink model for distribution system with various condition of MC-UPQC is shown fig.4.

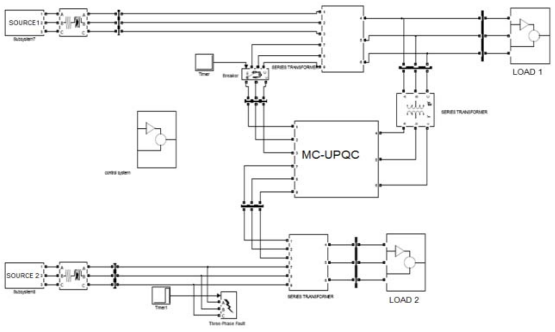

Figure 4: Simulink model for two feeder distribution system using MC-UPQC

The critical load L2 contains a balanced RL load of 10Ω and 100mH. The MC–UPQC is switched on at t=0.02s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Figure 6. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in figure 9.

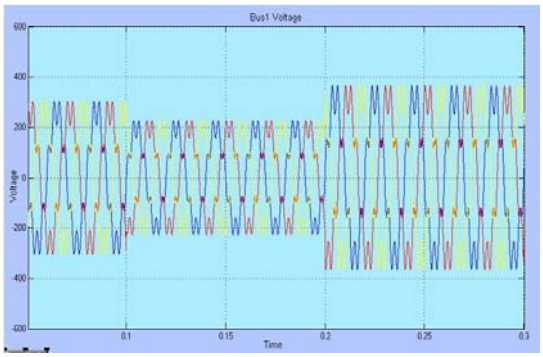

Figure 5: Three phase Bus1 voltage in feeder1

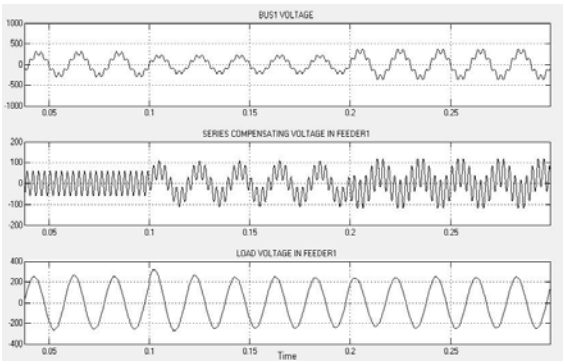

Figure 6: BUS1 Voltage, series voltage and load voltage in feeder1

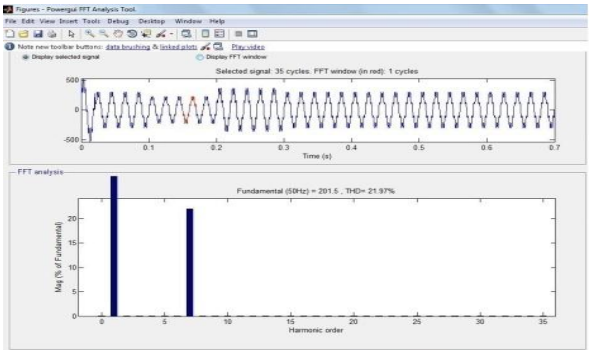

Figure 7: BUS1 Voltage FFT in Feeder1

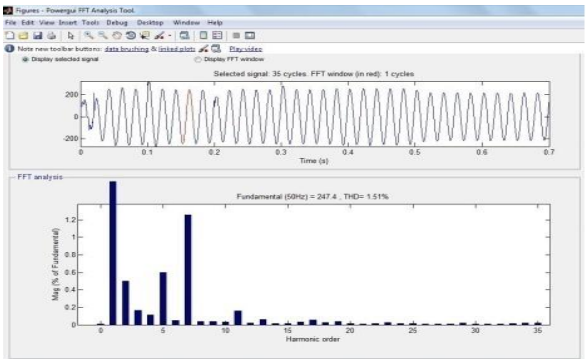

Figure 8: BUS1 Load Voltage FFT in Feeder1

Fig. 7 & 8 shows the FFT Analysis of BUS1 input voltage and load voltage. This shows that the THD is reduced from 21.97% to 1.51%.

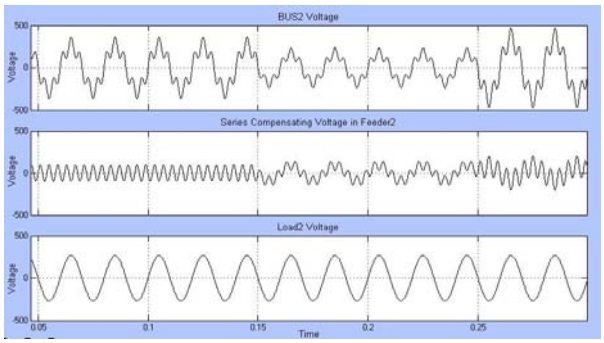

Figure 9: BUS2 Voltage, series voltage and load voltage in feeder2

5.2 Fault on Feeder 2

When a fault occurs in feeder2, the voltage across the Load L2 is involved in sag, swell and interruption. This voltage imperfection can be compensated by VSC2.in this case the power required by load L2 is supplied through VSC2 and VSC3.the performance of MC-UPQC under a fault condition on Feeder is tested b applying a three –phase fault to ground on feeder2 between 0.3<t<0.4.the results are shown in fig.10.

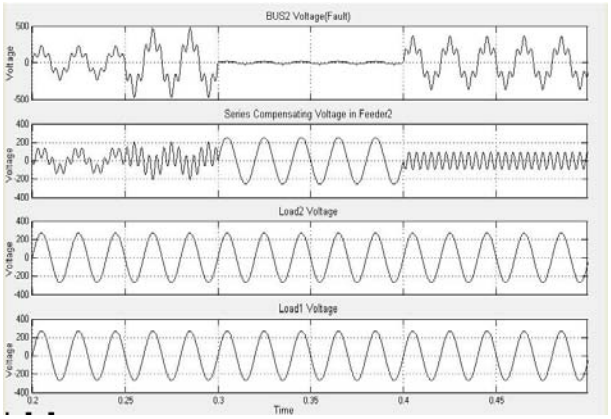

Figure 10: Upstream fault on Feeder2: BUS2 voltage, compensating voltage and Load L1 and L2 voltages.

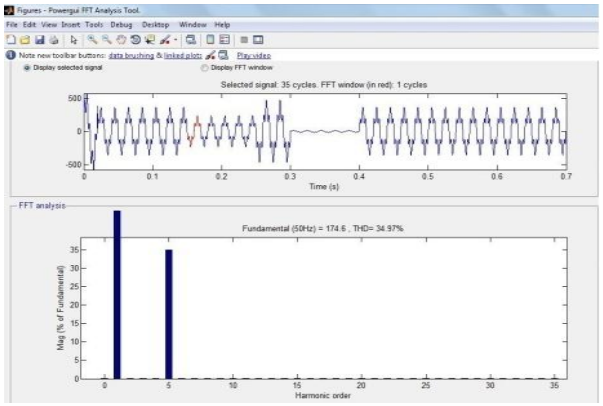

Figure 11: BUS2 Voltage FFT Analysis in Feeder2

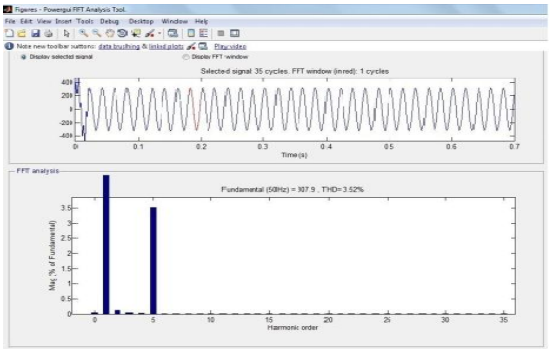

Figure 12: BUS2 Load Voltage FFT Analysis in Feeder2

Fig. 11 & 12 shows the FFT Analysis of BUS1 input voltage and load voltage. This shows that the THD is reduced from 34.97% to 3.52%.

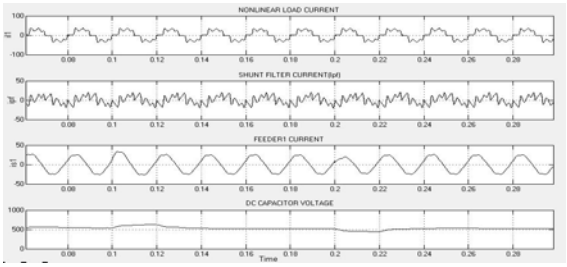

Figure 13: Nonlinear load current, compensating current, Feeder1 current and capacitor voltage.

The Nonlinear load current ,its corresponding compensation voltage injected by VSC2 ,compensated Feeder1 current and dc-link capacitor voltage is shown in fig.13.The distorted nonlinear load current is compensated very well, and the THD of the feeder current is reduced.

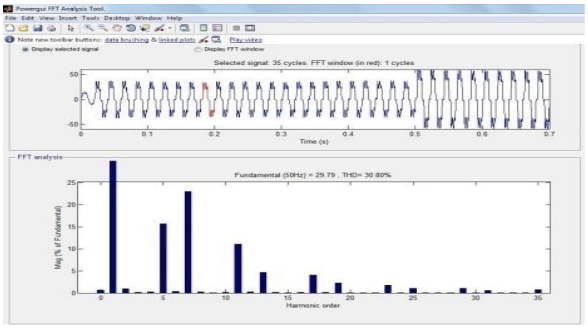

Figure 14: Nonlinear Load Current FFT Analysis

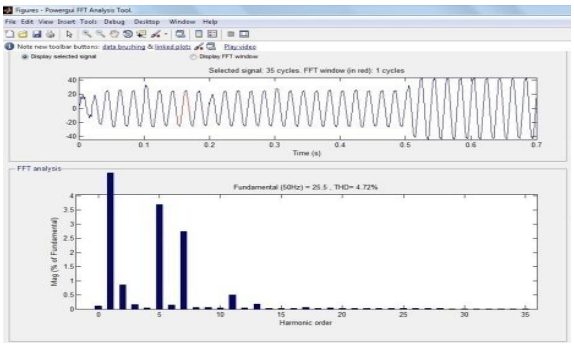

Figure 15: Feeder1 Current FFT Analysis

Fig. 14 & 15 shows the FFT Analysis of BUS1 input voltage and load voltage. This shows that the THD is reduced from 30.80% to 4.72%.

In addition to this another shunt converter is implemented by using hysteresis current controller and it is connected in BUS2 to operate load2.

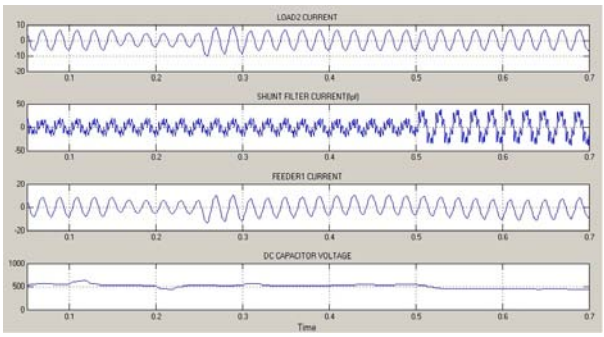

Figure 16: Bus2 Load current, Shunt filter current, Feeder current and DC Capacitor voltage.

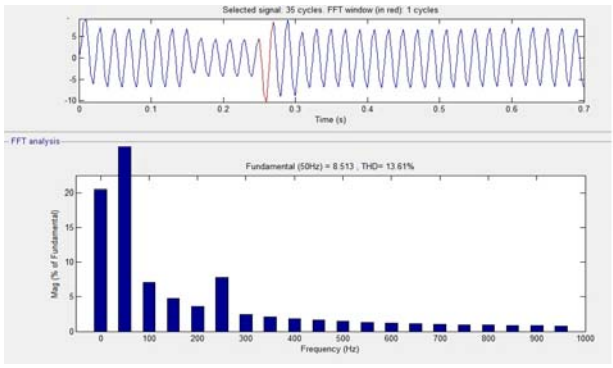

Figure 17: Load2 Current FFT Analysis

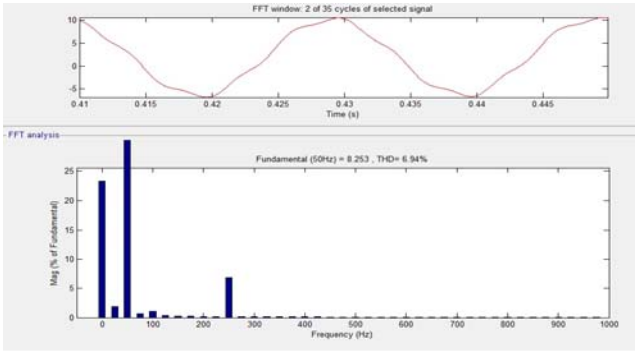

Figure 18: Shunt Filter Current FFT Analysis

Fig.17 & 18 shows the FFT Analysis of BUS2 Load current and compensation. This shows that the THD is reduced from 13.61% to 6.94%.

THD	*Before Compensation*	*After Compensation*
BUS1	21.97%	1.51%
BUS2	34.97%	3.52%
Nonlinear Load Current	30.80%	4.80%

The THD Analysis is made for the various conditions under compensation and without compensation. It shows that THD is reduced for various conditions. Hence Power Quality is improved by using Multi Converter UPQC in a Two Feeder Distribution System. Applications of Multi Converter UPQC are IT Parks, Commercial Office Complexes, Semiconductor industries, Machine Tool plants, Process Industries.

6. Conclusion

In the simulation of Multi Converter Unified Power Quality Conditioner, the performance of the MC-UPQC has been evaluated under various disturbance conditions such as voltage sag, swell and harmonics in the feeders, interruption in one of the feeder is observed and compensation is done. Also the FFT Analysis shows that the load voltages and feeder current is reduced after compensation for Power Quality improvement.

The Multi Converter is evaluated under various conditions and it is shows that the Power transfers between two adjacent feeders for sag, swell and interruption compensation, Compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity limitation. Also the capacitor voltage is regulated and power compensation is obtained between two adjacent feeders which are not connected. Hence by using MATLAB/SIMULINK the power quality of the two feeder distribution is improved and it forms the flexible operation of the system.

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