

Low Power, Noise-Free Divided By 4/5 Counter Using Domino Logic: A Survey

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Abstract: Reduction of propagation delay is very important for high speed applications. This paper gives an idea about the delay reduction on divided-by-4/5 counter. The delay is reduced by domino logic. Dynamic domino logic circuits are widely used in advanced digital Very Large Scale Integration (VLSI) circuits because it is uncomplicated to implement and low cost. Domino logic is a CMOS based approximation of the dynamic logic techniques. It was technologically advanced to speed up the circuit. Compare to static Complementary Metal Oxide Semiconductor (CMOS) logic, dynamic domino logic deals better performance. Domino gates naturally consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static Complementary Metal Oxide Semiconductor (CMOS) gate. In this paper, dynamic logic flip-flop such as Extended True-Single-Phase-Clock (E-TSPC) flip-flop based divided-by-N/N+1 counter is used for high speed and low power applications. And the proposed work is then compared with the static Complementary Metal Oxide Semiconductor (CMOS) logic.

Keywords: D-Flip Flop, Extended True Single Phase clock, Low power, High speed.

1. Introduction

In VLSI technology miniaturization in size of the circuit has increased dramatically. This has made it technologically achievable for high speed applications. For this, a high speed frequency divider which operates by applying high input frequency. In modern wireless communication systems, the power consumption is a key consideration for the longer battery life. The MOS current mode logic (MCML) circuit, which is of high power consumption, is commonly used to achieve the high operating frequency, while a true single-phase clock (TSPC) dynamic circuit, which only consumes power during switching, has a lower operating frequency [13]. To get high operating frequency Extended True Single Phase Clock (E-TSPC) is used. A prescaler is the most demanding part in this high speed frequency divider as it consumes high power. Dual modulus prescaler consists of flip-flop based divided-by-N/N+1 counter. It is adapt to Extended-True Single Phase Clock (E-TSPC) Flip-Flops for high speed and low power applications.

By combining two different techniques, there is a possibility of getting higher speed of the circuit. This can be done by interconnecting the extended true single phase clock of dual modulus prescaler with some extra logic. Due to the incorporation of additional logic gates between the flip-flops to achieve the two division ratios, the speed of the prescaler is affected and the switching power increases [7]. Various techniques have been proposed to improve the operating frequency. The rest of this paper is organised as, Section II – Analysis both True Single Phase Clock (TSPC) and Extended True Single Phase Clock (E-TSPC). Section III - Discussing about Dual modulus prescaler. Section IV - Discussing about Domino logic. Section V- Divide-by-4/5 counter using Domino logic. Section VI- simulation results and performance comparisons. Section VII- Conclusion of this survey and Section VIII- Future Work.

2. TSPC and E-TSPC Prescalers

In this section, maximum operating frequency with low power consumption of the TSPC and the E-TSPC based flip-flop is analyzed. True Single Phase Clock has the advantages of simple and compact clock distribution, high speed and logic design flexibility [1]. There is no clock skew problem because it uses single clock phase. But the main disadvantages of this true single phase clock is number of transistor usage is increased and large propagation delay. To overcome from this Extended True Single Phase Clock is used for this low power and high frequency applications which removes transistor stacked structure so that all the transistors are free of body effect. Main advantages of this E-TSPC are it uses two transistors. So it has higher operating frequency compared to true single phase clock. The propagation delay of the Extended True Single Phase Clock (E-TSPC) techniques is smaller than the True Single Phase Clock (TSPC) techniques [13]. The Extended True Single Phase Clock uses two transistors while a True Single Phase Clock uses three transistors as shown in fig 1.

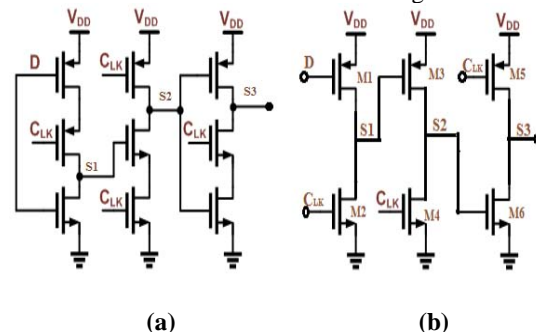


Figure 1: (a) TSPC flip-flop. (b) E-TSPC flip-flop.

3. Dual-Modulus Prescaler

When combining two different counters in the form of N/N+1 counter a dual modulus counter will produced. This dual modulus prescaler is designed by using D-Flip-flop (DFF). The prescaler is also called as counter which is used

for the high frequency application. A counter is nothing more than a specialised register or pattern generator that produces a specified output pattern or sequence of binary values upon the application of an input pulse signal called the "Clock". The clock is actually used for data transfer in these applications. Counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter where "n" is the number of counter stages used and which is called the Modulus.

3.1 Architecture of Divide-By-4/5 Counter

The divide-by-4/5 prescaler is the synchronous sequential circuit. The sequential logic circuits are used as data storage purpose. The D-flip-flop is widely used for many electronic devices. It is also known as data (or) delay flip-flop. So, the divide-by-4/5 prescaler is constructed with D-Flip-Flop.

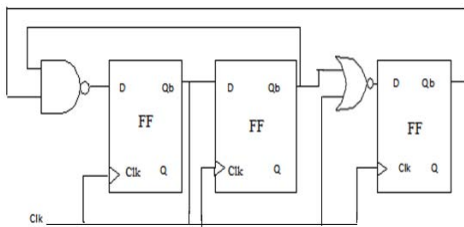


Figure 2: Divided-By-4/5 counter

The circuit shown in Fig 2 is the divide-by-4/5 counter using D flip-flop. It consists of three flip-flops. The first two flip-flops are the divide-by-4 counter. The third flip-flop is the divide-by-5 counter. The NAND gate is used to connect the divide-by-4 as the input and the NOR gate is used to connect the output of divide-by-4 counter to the input of divide-by-5 counters [16]. Here when the clock goes to high the output of the divide-by-4/5 counter is high. When the clock signal goes to low the output of the counter goes to high and low respectively. This divide-by-4/5 counter is proposed in the Extended True Single Phase Clock form. Due to the radioed method, this D flip-flop circuit only uses six MOS transistors in three stages. Because of the series of MOS transistors from the voltage supply to ground is reduced, it can operate at a high frequency. When applying supply voltage the circuit becomes to operate at high speed. Then this circuit is implemented with domino logic for low power applications.

4. Domino Logic

Domino logic uses fast N- transistor to increase the speed of the circuit. Where the static logic uses slow P- transistors to compute logic. To increase the speed and area efficiency domino gates are often employed in high performance circuits. Due to its performance and CMOS power consumption domino logic has created a considerable interest. Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [16].

4.1 Concept of Domino Logic

Domino logic requires two phases, precharge phase and evaluation phase. In this the output is high the precharge phase will occur and when the clock is high the evaluation phase will occur. Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. It was developed to speed up the circuits [17]. The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clk cycle), just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic [18].

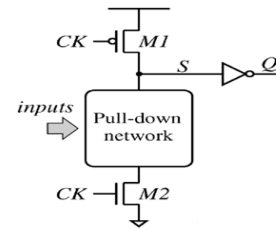


Figure 3: Domino Logic

In the precharge phase when the clock CK is low, the dynamic node S is charged to logic high through M1 and the output of the gate Q is low. The evaluation phase starts when the clock goes high. In this phase, M1 is OFF and M2 is ON. The dynamic node S discharges or retains its charge depending on the inputs to the pull-down network. Since there are cascaded logic blocks, the evaluation of a stage causes the next stage to evaluate and so on [19].

4.2 Divide-By-4/5 Counter Using Domino Logic

Extended True Single Phase Clock form of divide-by-4/5 counter is designed with domino logic for high speed and reduce noise immunity in the circuit. The Extended True Single Phase Clock is used to increase the higher operating frequency by reducing the number of transistors used. The circuit diagram which shows the working principles is given below.

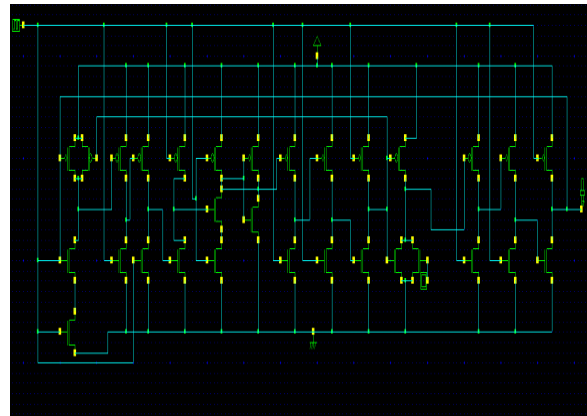


Figure 4: Schematic diagram of Divide-By-4/5 counter using Domino logic

From the Fig 4 the E-TSPC form of D Flip-Flops (DFF) are connected together. The divide-by-4/5 counter consists of three flip-flops and one negated AND (NAND) gate and negated OR (NOR) gate. The NAND gate connected in front of the DFF1 and domino logic is connected between the both DFF1 and DFF2. Then the NOR gate is connected before the DFF3. The MOS transistors are act as switches. The Metal Oxide Semiconductor (MOS) is turned on or off depending on the gate voltage. In Complementary Metal Oxide Semiconductor (CMOS) technology, both n-channel (and nMOS) and p channel MOS (or pMOS) devices exist. The n-channel MOS device requires a logic value 1 (or a supply Vdd) to be “on” the p-channel MOS device requires a logic value 0 to be “on”. The MC signal is used to control the circuit.

5. Simulation Results and Performance Comparisons

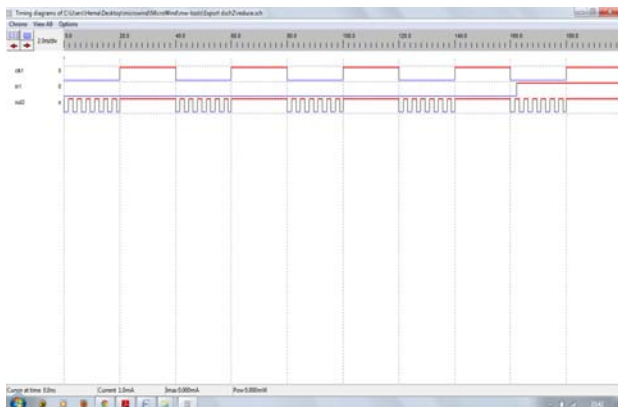


Figure 6: Timing Diagram of Divide-by-4/5 counter using domino logic

Extended True Single Phase Clock based Divide-by-4/5 counter using Domino logic is designed by using MICROWIND TOOL. Click on the timing diagram icon in the icon menu to see the timing diagram of the input and output waveforms. The frequency versus time of divide-by-4/5 counter using domino logic. The time scale is given as 10ns with 5GHz frequency then the power consumption is 19.466µW shown in Fig 7.

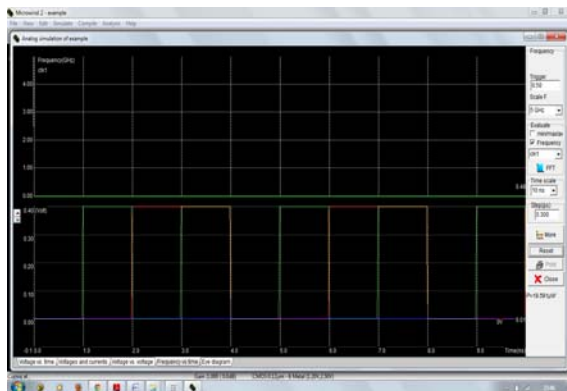


Figure 7: Frequency Vs Timing diagram of divide-by-4/5 counter using Domino logic

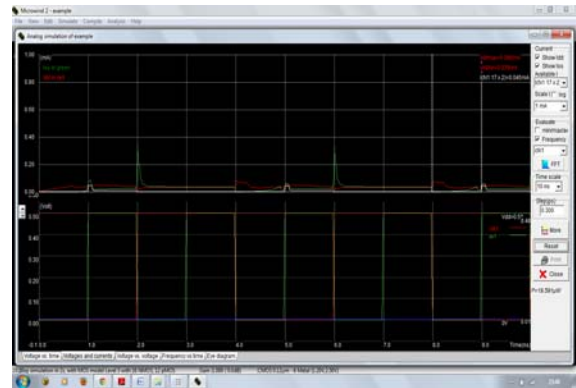


Figure 8: Voltage and Current diagram of divide-by-4/5 counter using Domino logic

The Fig 8 shows the voltage and current waveform of Divide-By-4/5 counter using Domino Logic. When the supply voltage is given as 5V and the current supply is 1mA and the time scale is 10ns. So the power obtained is 19.466µW and the average drain current is 0.039mA. the following figure shows the voltage vs time diagram of proposed circuit.

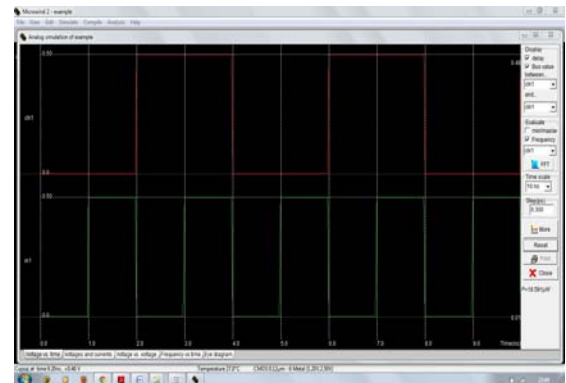


Figure 9: Voltage Vs Time diagram of divide-by-4/5 counter using domino logic

Table 1: Comparisons of domino with other logic

S. No	Dynamic Logics	Time Scale (ns)	Power Dissipation	I _{dd} Avr (mA)	Area (µm ²)
1	Domino logic	10	4.989 µW	0.004	104
2	C ² MOS	10	0.173 mw	0.144	132
3	CVSL	10	0.478 mw	0.502	121

From the above table, when applying constant 1.20 volt and constant time scale of 10 ns, when comparing to the other Dynamic logic the power dissipation of the Domino logic circuit is reduced. The power dissipation is the important challenge in the VLSI circuit design and also the area of Domino logic circuit is reduced. By using the comparison table we are obating a graph for power dissipation and average Drain current. In these power dissipation and average drain current of the Domino logic is reduced.

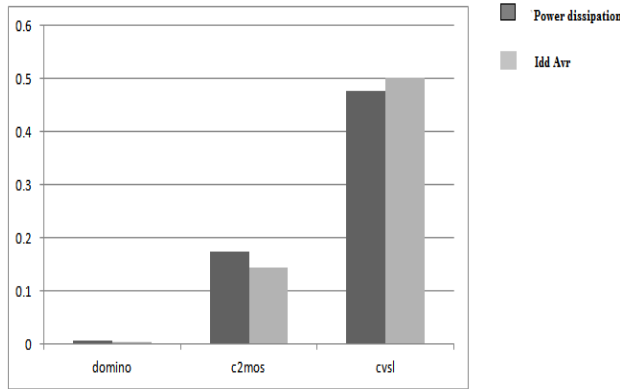


Figure 5: Power Dissipation versus Idd Avr

By implementing these Domino logic with the Dual modulus prescaler we are getting a circuit with increased speed and low power and low voltage performance. The following table gives the measured performance of proposed circuit.

Table 1.2: Measured Performance Summary

Supply Voltage	0.5v
Power Consumption	19.466 Mw
I _{dd Avr}	0.038ma
Time Scale 20 Ns	6 Pulses Of Output Signal
Core Area	65 X 14 Mm ²

From the above table, when the supply voltage is 0.5v the power consumption is reduced to microwatt and the speed of the circuit is increases.

6. Conclusion

Extended True Single Phase Clock based divide-by-4/5 counter of dual modulus prescaler is used to increase the operating frequency of the circuit. The circuit simplicity leads to a shorter critical path and reduced power consumption. When the Domino logic is designed with this divide-by-4/5 counter the speed of the circuit will increase and reduces the noise immunity. This proposed design is used for the modern communication like frequency synthesizer, timers.

7. Future Work

- Investigating the proposed system with other dual modulus architecture and to obtain performance comparisons.
- The layout of the proposed dual modulus circuit will be obtained in reduced nanometre.

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