Techniques Used for Mask Less Lithography

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Abstract: ***The ability to do selective lithography drives the semiconductor technology, but with the ever decreasing minimum feature size the need for higher resolution increases and so does the cost and complexity. Mask less lithography provides solution in the form of several techniques which are cost effective. In scanning electron beam lithography, instead of light, electron beam is used and the setup and principle used are similar to that of scanning electron microscope. Similarly scanning probe lithography is based on atomic force microscopy which employs cantilevered tips to modify the surface at an atomic scale. Both these techniques have low throughput and need to bring in some parallelism to improve the throughput. Zone-plate array lithography (ZPAL) uses diffracted light for patterning the surface. There are several other techniques as well. Though ZPAL has an increased speed, but all the techniques are being improved to achieve higher throughput rates.***

Keywords: photo resist, numerical aperture, lithography

1. Introduction

Technological advancements have been made possible by the semiconductor industry, which in itself has been driven by the ability to do selective lithography, and thus etching selectively.

The conventional photolithography technique involves the transfer of an image from a photographic mask to form the resultant pattern on a wafer. It is achieved by the use of a photosensitive polymer film called the photo resist which is spin coated and baked on the wafer. The coated wafer is then exposed to radiation of the suitable wavelength through a patterned mask. The exposed part of the photo resist undergoes photochemical reaction, and thus is able to record the image of the mask. The irradiated wafer is baked to reduce standing wave phenomena, caused due to interference of incident light. After this post-exposure bake the wafer is processed using a developer solution. The photo resist can be classified as positive or negative, depending on the polymer used. In positive photo resist the exposed part dissolves in the developer, and in negative, the unexposed part is soluble and gets removed. The resulting patterned wafer is then hard baked to solidify the remaining photo resist and make it a more durable protective layer in the future processes of etching, ion implantation, etc. After all the processing has been done the remnant patterned photo resist can be removed by chemical mechanical processes.

In order to get better outputs, a variety of resolution enhancement techniques (RETs) are used.

2. Need For Mask less Lithography

Though optical mask-based lithography has been predominantly used, but with ever decreasing feature size, the cost and the complexity of the mask as well as the tools have been increasing.

The mask gives fixed patterns and the cost of the tools and the mask make the process over-conservative, and hence loses the flexibility. Mask Based lithography is ideal for high volume manufacturing because batch processing enables enormous data transfer rates. Low-Cost is achieved by amortizing mask cost over large number of dies. However for low-volume manufacturing, experimentation, design verification,, research and novel applications of lithography, mask less lithography systems convincing advantages in cost and convenience. The mask itself is Numerical Aperture (NA) is a measure of the optical resolution of the system. The cost and complexity increases exponentially with NA for both the tools and the mask to achieve maximum speed with this

3. Mask less Lithography Techniques

3.1 Scanning Electron Beam Lithography (SEBL)

SEBL works on the principle of Scanning Electron Microscope. The electron beam is generated by an electron gun and is driven towards the anode due to the potential difference. The beam is passed through magnetic lenses and optical column. The action of magnetic lenses on the electrons is same as that of optical lenses on light. They are fabricated by wrapping circularly symmetric iron core with turns of copper wire. The purpose of the magnetic lenses is to focus the diverging beam to a point and that of the optical column is to magnify or de magnify as per the need of the resolution. The optical column also has blanking plates which switches ‘on’ or ‘off’ the converging electron beam on the substrate by letting it pass un deflected or deflecting it. The scanning coils change the point of focus within a fixed radius by deflecting it using electrostatic and electromagnetic field. The sample is mounted on a holder and clamped on to a stage which can be shifted for printing the pattern.

As minimum feature sizes in CMOS technology scale, the cost of critical dimension masks dramatically increases. Mask costs in 90nm technology are exceeding 1 million dollars. An alternative to mask-based optical lithography is mask less lithography, where the layout data is directly written onto a wafer. Various approaches have been investigated, including e-beam, micro-machined mirror projection, and nano-jet printing [1]. To achieve the required 1nm edge placement with25nm pixels in 45nm technology, a 5-bit per pixel data representation is needed, resulting in a total of over 500Tb of information on a 300mm wafer. To be competitive with conventional optical systems, any future lithography system should be capable of projecting one layer

per minute, resulting in approximately 12Tb/s of raw data throughput. Adding the necessary redundancy and communications overhead to the data stream would likely increase the required throughput by another 25%, reaching 15Tb/s ranges. This paper presents a mask less lithography interface and circuitry that provide the required throughput. It is designed to work with a micro-machined mirror array integrated on a chip exposed by extreme ultra-violet (EUV) light in a conceptual system as shown in Figure 1. In this approach, the conventional mask is replaced by a programmable one, which is reprogrammed between consecutive light flashes. Either storing or continuously feeding the required amount of data to the writer chip is not feasible. The key idea of the work presented here is the compression of rasterized data on a main storage unit and the continuous decompression on-the-fly. The basic design of a data processing system capable of delivering tera-pixel data rates necessary to achieve next generation mask less lithography. This design consists of storage disks, a processor board with memory, and a decoder-writer chip with data-decoding circuitry fabricated together with a massive array of pixel writers .Layout data for all layers of a single chip is compressed off-line and stored on the disks. Before the writing process begins, only a single compressed layer is transferred from disks to the processor board memory and stored there. As the writers write a stripe across the wafer, compressed data is streamed from the processor board to the decoder writer chip in real-time as needed. The on-chip decoding circuitry, in real-time, expands the compressed data stream into the data signals necessary to control the writers. The key challenge for such a system is the design of a high -throughput on-chip data decompression architecture and the circuitry that implements it. This paper demonstrates the design of such a high throughput decompression chip. To simplify the solution, a binary interface to the writers using an SRAM array is implemented. This avoids the handling of 5-bit grayscale values that would require analog control of mirror dollars. An alternative to mask-based optical lithography is mask less lithography, where the layout data is directly written onto a wafer. Various approaches have been investigated, including e-beam, micro-machined mirror projection, and nano-jet printing [1]. To achieve the required 1nm edge placement with25nm pixels in 45nm technology, a 5-bit per pixel data representation is needed, resulting in a total of over 500Tb of information on a 300mm wafer. To be competitive with conventional optical systems, any future lithography system should be capable of projecting one layer per minute, resulting in approximately 12Tb/s of raw data throughput. Adding the necessary redundancy and communications overhead to the data stream would likely increase the required through put by another 25%, reaching 15Tb/s ranges. This paper presents a mask less lithography interface and circuitry that provide the required throughput. It is designed to work with a micro-machined mirror array integrated on a chip exposed by extreme ultra-violet (EUV) light in a conceptual system. The essence of Huffman encoding is that it assigns shorter code words to more frequent data, thus reducing the average number of bits required for representation. With layout data tested in [4] it achieves a typical compression ratio of approximately 5. This implementation uses the canonical Huffman table because of its simple representation that lends itself to a less complex decoder implementation. The algorithm description can be found in [6]. The Huffman decoder architecture is shown in Figure 4. The coded data is input sequentially into a shift register. For every bit that is shifted in, the counter is incremented. The output of the counter is used to address mincode, maxcode and index tables. The word in the shift register is compared to the output of the maxcode table. If the shift register word is less than the output of the maxcode table then the decoding is done. To get the decoded word, the shift register word is added to the output of the index table, and then subtracted from the output of the mincode table. This value is then used to address a symbol table which holds the decompressed symbols. To increase the decoding speed, the architecture is pipelined at the cut-sets, leaving only the symbol memory lookup time in the critical path.

When implemented in 0.18µm CMOS technology, the area of this Huffman decoder is about 6mm x 120µm. The Lempel-Ziv algorithm replaces repeating sequences of symbols with a pointer to a history buffer. This pointer indicates where in the buffer to retrieve the data (offset), and how many symbols to copy (length). Uncompressed symbols are literals. The architecture chosen for this design consists of a systolic array processor, where the data pass bidirectionally from one processing element to neighboring elements in a regular pattern [7]. Each processing element consists of one forward buffer and one reverse buffer and stores two 8-bit symbols. Data flows from left to right through the forward registers and then wraps back, flowing from right to left through the dictionary registers.. The decoding is done locally, avoiding any long wires to the history lookup buffer that would be unavoidable in the non-systolic implementation. To get better compression, the literal, offset, and length symbols are independently Huffman coded. To allow this, separate Huffman tables must be multiplexed in, depending on the current symbol being decoded. Furthermore, in the systolic implementation, arun length decoder is used.

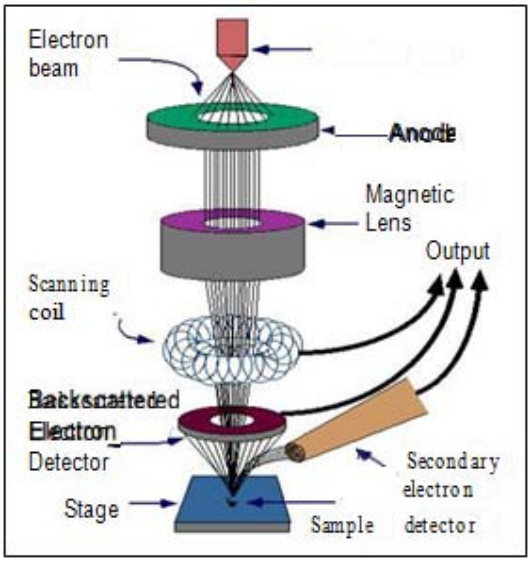

Figure 1: Simplified Schematic of SEM/SEBL

The writing speed is low since each pixel is individually scanned, thus increasing the throughput time. It also results in the throughput time being same for sparse and dense patterns. Vector scan involves jumping over from one

patterned area to next, skipping all non-patterned area. Here though the writing time is less but it takes more time for the beam to settle. The beam current and current density prove to be critical parameters in optimization of pattern writing time.

Structures 1nm in size and devices with minimum feature size of about 20nm have been reported using SEBL. The beam can be as small as 0.5nm. [3]

Limitations: Though SEBL provides higher resolution than mask- based lithography in addition to reduction of the cost and complexity, it has its drawbacks. The major constraint of SEBL, as can be realized from above, is the low throughput time. Proximity error is seen in this case as well but its correction is relatively easier and involves adjusting the dose. Another drawback in this is that, the electron mass being very less, it penetrates to a very small depth and has significant lateral scattering which may lead to defects. There are backscattered electrons which need to be taken care of. Also since the electron beam is passed through a series of lenses and deflected several times, aberration also comes into play and needs correction.

Improvements: It is evident that to increase the throughput, some degree of parallelism has to be introduced. This can be achieved by using arrays of beams scanning the substrate. Another improvement is the use of variable shaped beam with multiple pixels in place of the commonly used round beams. They use vector scan for writing on the substrate. Even as the cost increases in using variable shaped beams, it can be traded off for increased throughput.

3.2 Scanning Probe Lithography (SPL)

It works on the basic principle of an Atomic Force Microscope (AFM). In an AFM, the surface is imaged by utilizing a pointed tip the order of the atomic scale. The tip is supported using a cantilever. As the tip scans through the surface, the cantilever deflects due to the forces between the tip and the surface. The deflection is recorded and using this, the image is obtained.

Using this tip, lithography can be done in the nanometer range. In fact this is the prevalently used technique for nanolithography. Four methods are common in use.

a) Atomic Manipulation: The tip can push or pull particles using electric field, magnetic interactions or chemical binding force, thus can be used to form desired patterns by shifting or removing particles.
b) Mechanical and thermomechanical patterning: The probe tip can be used to make pits, lines and craters on a soft layer of resist. This is being used to make memories on a large scale. Heating the tip proves to be highly effective in this.
c) Local Oxidation: The silicon wafer is dipped in HF solution which removes the local oxide and passivates the dangling bonds on the surface with hydrogen. In the presence of moisture, the tip being at very high electric field ionizes the water molecules to give oxide and hydrogen ions. The oxide ions remove the hydrogen ions from the surface and form local oxide in the region to be patterned.
d) Electron Exposure of Resist: The substrate is coated with electron sensitive resist. Electric bias between the probe tip and sample, leads to field emission of electrons. Chemical changes are induced and thus the desired pattern is formed.

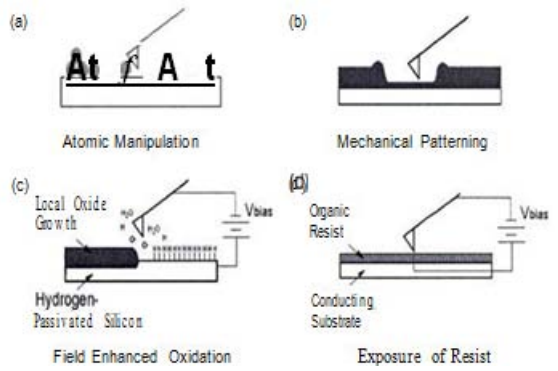

Figure 2: Nano patterning methods using SPL

Lateral atomic resolution of 1-10 nm and vertical resolution 1Å have been reported. [5]

Limitations: Though all these methods serve the purpose of nano machining and nano deposition, and the resolution is very high, the probe tip undergoes significant wear and damage, hence requiring frequent replacement. The writing speed is also very less.

Improvements: Newer materials with more durability can be used for the probe tip. To bring in parallelism, large arrays of cantilevered probe tips are being used.

4. Zone Plate Array Lithography (ZPAL)

Unlike the previous two techniques, ZPAL is based on the optical lithography, with a modification in the optical system. It utilizes an array of zone plates instead of lenses. Zone plates are symmetric rings of alternating transparent and opaque regions (Fresnel zones). The light hitting the zone plates diffracts around the opaque zones. The symmetric rings are placed such that the diffracted light interferes constructively at the desired focus. These plates are arrayed to form a unit cell. The light incident on this array determines the pattern printed on the wafer.

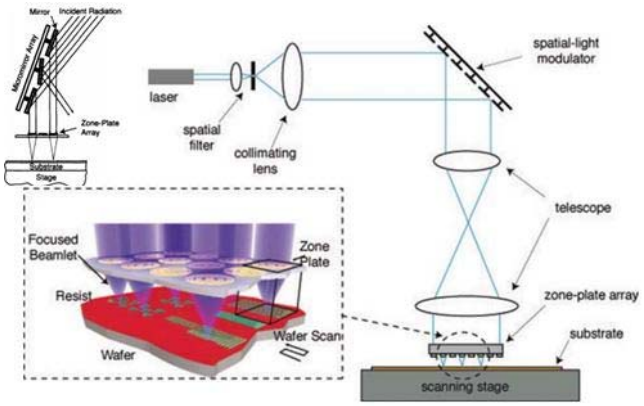

Figure 3: (a) Blanking and un blanking using micro mirrors on SLM

(b) Schematic of the ZPAL system
(c) Patterning using diffracted light in ZPAL

As seen in the schematic (Figure 3), collimated light from the source is focused onto a spatial light modulator (SLM). This modulator can consist of array of micromirrors or shutters which govern the illumination pattern of the pixels in the unit cell. The micromirrors govern the blanking or unblanking of light onto a plate by changing the inclination. The shutters can open or close, thereby illuminating the desired plates.

The entire unit cell is shifted to scan the sample, the number of pixels printed simultaneously, being equal to the number of plates in the unit cell. Here the speed limiting factor is the time to modify the pattern on the SLM. This paper presents a mask less lithography interface and circuitry that provide the required throughput. It is designed to work with a micro-machined mirror array integrated on a chip exposed.

Limitation: ZPAL is a promising technique with the limitation of increased complexity as both the sample stage and the modulator need to be synchronized.
Improvement: Though the NA of ZPAL is high (~0.9), but this technique being optical based, there is scope of enhancing the NA by incorporating immersion lithography with deionised water

5. Few Other Techniques

- **Focused Ion Beam Lithography:** It involves scanning a focused beam of ions in a patterned fashion across a surface. The beam hitting the wafer induces chemical reactions and hence patterning. This offers higher resolution patterning because of heavier particles having more momentum. It gives a smaller wavelength and therefore almost no diffraction.
- **Interference Lithography:** An interference pattern between two or more coherent light waves is set up and recorded on a photo resist. This interference pattern consists of periodic series of fringes representing intensity minima and maxima.
- **Dip pen Nanolithography:** Putting down chemical compound as ink on the substrate by molecular transport utilizing the water meniscus, using the probe tip of AFM to get the desired pattern.

6. Conclusion

With the demand for mask less lithography and high resolution, several promising techniques have been devised. Scanning E. Beam Lithography is widely used for research and low-volume manufacturing purposes. Scanning Probe Lithography is an effective tool for nanofabrication. Zone-Plate Array Lithography has extensive experimental results and promises application for making, direct writing, and as a complement to SEBL. All mask less lithography techniques yielding high resolution, some parallelism, would decrease the cost and complexity involved in silicon wafer lithography, and thus processing.

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