Implementation of Four Morphological Operators for Image Filtering on FPGA

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Abstract: ***Field Programmable Gate Array (FPGA) technology has become a viable target for the implementation of real time algorithms suited to video image processing applications. The unique architecture of the FPGA has allowed the technology to be used in many applications encompassing all aspects of video image processing. Non-linear morphological filters represent a basic set of image operations for a number of applications. In this work, an implementation of four morphological image filtering techniques using a FPGA Nexus II, Xilinx, Spartan 3E, is presented. The FPGA-based system is accessed through a Mat lab graphical user interface, which handles the communication setup. A comparison between results obtained from MATLAB simulations and the described FPGA-based implementation is presented.***

Keywords: Image, Filtering, FPGA, Morphology.

1. Introduction

Field Programmable Gate Arrays (FPGAs) are part of Current reconfigurable computing technology, which in some ways represent an ideal alternative for image and video processing. FPGAs generally consist of a system of logic blocks, such as look up tables, gates, or flip-flops, just to mention a few, and some amount of memory, all wired together using a vast array of interconnects. All of the logic in an FPGA can be rewired, or reconfigured, with a different design, according to the designer needs. FPGAs generally consist of a system of logic blocks (usually look up tables and flip-flops) and some amount of Random Access Memory (RAM), all wired together using a vast array of interconnects. This type of architecture allows a large variety of logic designs for a number of real time applications. There is currently a vast amount of software for digital image processing applications, for industrial or educational purposes. Among these, MATLAB has been extensively used becoming a standard mathematical language for engineers and scientists around the world. MATLAB is a software environment that allows problems and solutions to be expressed in familiar mathematical notations. Numerous toolboxes and other software packages have been developed for MATLAB to facilitate a variety of engineering and educational tasks such as algorithm development, modeling, simulation, data analysis, visualization, engineering graphics, and application development. Simulink is a software package that works in conjunction with MATLAB for modeling, simulating, and analyzing dynamic systems through an intuitive block diagram-based GUI that utilizes various block-set libraries to incorporate preconfigured blocks and connectors by simple drag and drop operations. MATLAB can be used also for generating hardware description language in order to synthesize FPGA-based designs. In this paper, a Nexus II system based on the Xilinx FPGA Spartan 3E has been used to implement a low-cost image processing system for real time applications with educational purposes. A MATLAB graphical user interface allows the designer to open the image to be processed, setup the communication parameters, specify the required processing, send the input image, and receive the corresponding result after the process.

This paper organized as follows. In section II.Simple Introduction of morphological operations, Architecture of Proposed morphological operations in section III, Results in section IV and finally conclusion will be in Section V.

2. Over View of Morphological Operators

Morphology deals with shapes of images in Image Processing. The value of the each output pixel is based on a comparison of the corresponding pixel In the input image with its neighborhood pixels. The size and shape of the structural element determines the morphological operation to be done On a particular image. Morphological operations are usually applied to the processing of binary and Grayscale images. Fundamental operations are Dilation and Erosion. Form these two basic operations; other operations like opening and closing of an image are developed. The principle of Dilation operation is the value of the output pixel is the maximum value of all the pixels in the input pixels neighborhood. In Erosion, the value of the output pixel is the minimum value of all pixels in their input pixel's neighborhood. Structuring Element consists of 1's and 0's and the size is much smaller than input image. The center of the structuring element identifies the pixel being processed. Opening means erosion followed by dilation operation and closing means dilation followed by erosion operation.

3. Architecture of Proposed Morphological Operators

Structuring element is chosen properly according to the requirements. This structuring element is moved over the entire input image, with center of structuring element is coincided with the pixel of interest and the output pixel corresponds to this pixel being processed is either

maximum (Dilation) or minimum (Erosion) of all pixels in the neighborhood pixels. This operation is done for all input image pixels and thus output dilated/eroded image is found. The size and shape of the structuring element decides the output image. By properly choosing this element, one could get the desired morphological operation on the input image.

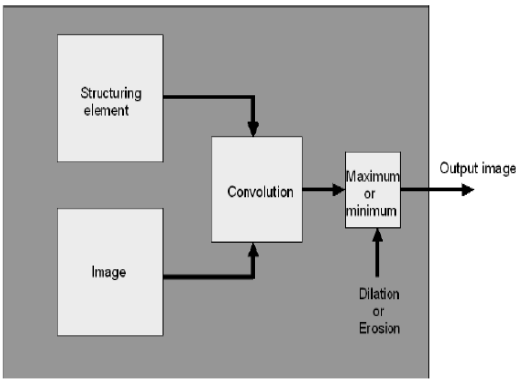

Figure 1: Dilation/Erosion Block Diagram

Figure.1 shows the block diagram of the Dilation/Erosion IP core. It consists of input image, structuring element, convolution block and maximum/minimum blocks. The desired structuring element with appropriate size and shape is convolved with input image by convolution block. Then maximum/minimum (Dilation/Erosion) of neighborhood pixels is found by Maximum/Minimum block.

Architecture Diagram

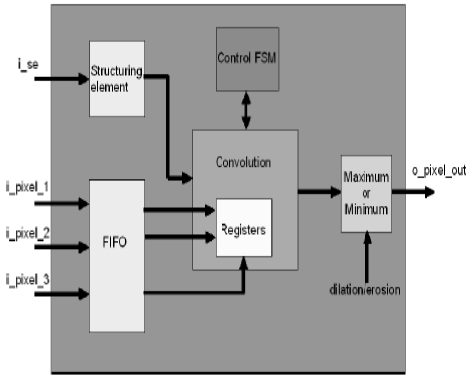

Figure 2: Dilation/Erosion core Architecture Diagram

Fig.2. represents the architectural diagram of the Dilation/Erosion core. Input pixels are written into FIFO. Structuring elements which are coming from input port i_se are stored in internal memory. The FIFO data is read and stored in internal memory and the depth of the memory depends upon the size of the structuring element. Then structuring element is convolved with these input image pixels and the output pixel which is either maximum (Dilation) or Minimum (Erosion) is done.

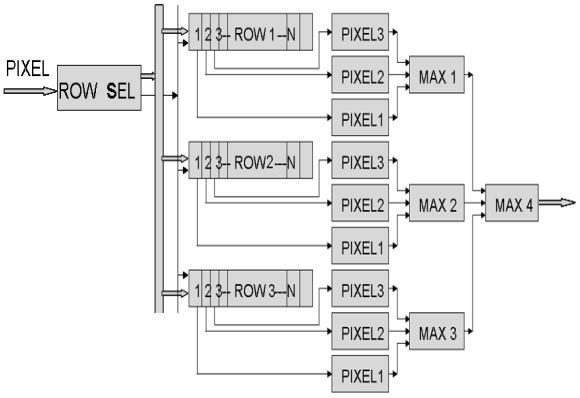

Figure 3: Block Diagram of Dilation Internal Operation

The data from UART receiver is given to Module which performs Dilation. Pixel information as in gray scale coded format. Pixel information must be stored into rows for this row_sel will take care of it. Row contains Data banks which is equal to the dimensions (only width) of the image. Row sel first select first row and stores information (pixel value) in it after first row is full i.e. it is end of the image of first line then the row_sel select row 2 for filling of the data if row 2 is full then goes for row3 after completing the row 3 it go for the row 1 and the process will continue. Row sel will select row *simultaneously* till the image is complete.

The data in row 1 columns 1,2 and 3 pixel which ever pixel is maximum will be selected in the same manner row 2 and row 3 maxim pixel value is selected from these three maximum is given to max4 in max 4 resultant will be maximum of all three maximum of rows, that resultant is taken as output. This is forced on to the UART transmitter section.

4. Results

Simulation results are observed in Modelsim tool. Fig4 shows the results of dilation, we can observe that the maximum value pixel in an image are detected and performed required operation.

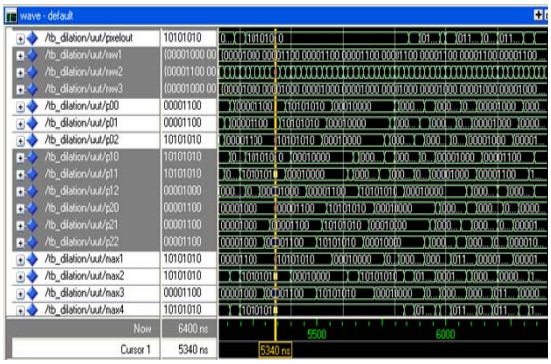

Figure 4: Simulation results of Dilation

Mat lab results of dilation are observed, that every background pixel that is touching an object pixel is changed into an object pixel.Fig5 shows the mat lab results of dilation of an image named photographer.

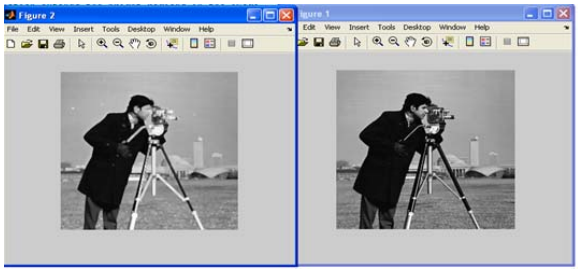

Figure 5: Matlab results of Dilation

5. Conclusions

A low-cost image processing system for real time application has been presented. The system takes advantages of the available resources in a Nexus II system based on the Xilinx FPGA Spartan 3E. The described FPGA-based real-time image processing system was shown to provide a very good tool for further computer vision applications. At the same time, it is worthwhile to mention the educational value of the developed prototype as a laboratory tool in modern digital system courses.

References

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Authors Profile

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