A Survey of HDLC Controllers

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Abstract: ***HDLC is an efficient protocol defined in the layer 2 of OSI model. HDLC is a group of protocols for transmitting synchronous data over a point-to-point link. Many chips have been designed for HDLC controllers. Not all the features of the controller are always needed. Due to the advantages of FPGA, controller chips are being designed according to the needs of the communication system. This paper discusses the design and implementation of some such HDLC controllers.***

Keywords: HDLC controller, FPGA, CRC, customization

1. Introduction

HDLC protocol is a common protocol in networking. HDLC is the mother of all LANs and WANs. SDLC protocol was adopted by IEEE and defined as HDLC. HDLC is defined in the second layer of OSI model. It is preferred because of the advantages offered namely supports both half duplex and full duplex communication lines , offers error control (used for error correction in modems), efficient and powerful synchronization features. Due to these features HDLC controller chips have been designed. Many networking applications use HDLC controller for communication. For faster implementation HDLC controllers were designed and developed according to the requirements of the basic communication system using FPGA. Researchers have presented work where more number of channels is implemented using FPGA and also simple controller designs as a part of a large system eg. the implementation for 128 channels based on FPGA, implementation where HDLC controller is a part of an SOC. In this paper, a comparative review of these applications of HDLC controller has been presented. Section 2 discusses the HDLC frame structure. In section 3, the various designs and implementations are discussed along with their results.

2. HDLC frame structure

The data transmitted is termed as a frame. The frame has to follow a predefined format called as frame structure.

Flag	Address	Control	Data	FCS	Flag

The frame starts and ends with same bit string (01111110) called flag. These are called header and frame end. Address field holds the address of the receiving station. Control field holds the control code. Data field is the information to be transferred. FCS stands for Frame Check Sequence which is the calculation of the entire frame excluding the flag. FCS adopts the CRC $x^{16} + x^{12} + x^5 + 1$ as calculating polynomial. Bit stuffing is performed on the frame i.e. a '0' is inserted after a sequence of five '1's. Thus '0111110' is the longest sequence that will appear in the frame other than the flag. After the fifth '1' the next bit is checked for a '1' or '0'. If a '1' is found the code is taken as a flag or else as a data. The control field varies depending on the mode of operation. There are three modes of operation for a HDLC controller.

2. Various Designs and Implementations

The need for communication in each application is different. Hence the design for the HDLC controller for each application is different. The controllers have been designed for half duplex transmission line, and also for full duplex. The clock requirement, synchronization requirement for every design is different. The CRC polynomial selected can be 16-bit or 32-bit. Mostly CRC-16 has been used.

Next part of this section presents a review of the controller designs. The papers selected for review are on the basis of application of the controller.

Chen Zhifeng et al have proposed a broadband radar system communication, the requirements are few**:** baud rate not less than 2 Mb/s, the communication distance does not exceed 10 meters, the error rate less than 10^{-6}. In view of the demands for baud rate and stability, the controller is based on a simple register design. Hence, very few hardware resources are needed and resources are saved for large-scale data processing of the wideband radar system. Also to ease the access of the radar signal processor to the controller, a SRAM interface is added.

The block diagram for this system is shown below:

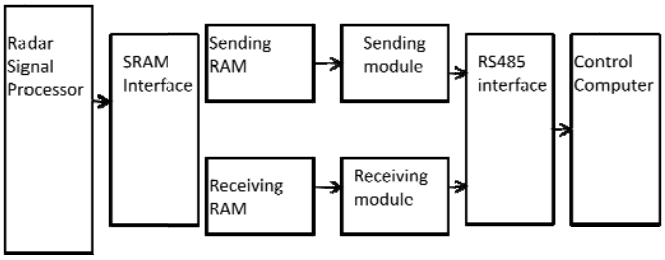

Figure 1: RADAR System Structure

The controller is in control of the communication between the radar signal processor and the control computer through 485 bus. While processing data, the control computer sends

the control instructions to the radar signal processor. The radar signal processor sends back the processed results to the control computer. The data processing is done by following an algorithm.

A half duplex communication system is being used for communication. The HDLC controller operates in three states: idle state, sending state and receiving state. These state transitions are controlled through a radar processor software program. The HDLC controller has three main modules: control module, send module and receive module.
The HDLC controller is designed using top-down methodology using VHDL in ISE 10.1. The design is simulated in Modelsim 6.3. Programs are written on radar signal processor software to achieve transmit HDLC receiving data. The simulation results show that the frame data are successfully received, with less CRC errors.

The controller is synthesized on xc4cfx60-10ff672 of Xilinx FPGA. The hardware resources consumption of the controller have the following statistics:

Number of Slice Flip Flops: 274 out of 50,560; 1%
Number of 4 input LUTs: 451 out of 50,560; 1%
Number of occupied Slices: 313 out of 25,280; 1%
Total Number of 4 input LUTs: 497 out of 50,560 1%
Number of BUFG/BUFGCTRLs: 4 out of 32; 12%
Number of FIFO16/RAMB16s: 2 out of 232; 1%

This HDLC controller has the following features: receiving and sending module programming control, query/interrupt working mode, 8-bit station address freely set, data overflow/CRC error detection, SRAM memory and registers can be accessed by SRAM interface, storage resource can be expanded.[5]

Gao Zhen-Bin et al have implemented a multi-channel HDLC controller on Xilinx Virtex. A double full duplex transceiver has been developed for general applications with built-up dual port RAM and an interrupt controller. It is controlled by the host CPU with few commands. The chip receives and transmits data frames automatically. The status is also provided after the completion of operation. The control registers dominate the modes of operation and can be easily set. The baud rate of each channel can be changed. The transceiver consists of four main blocks: Interrupt controller, Control unit, Registers and Bus buffers, Two channels: channel A and channel B, Dual port RAM and RAM management unit.

The following block diagrams show the details of the transceiver:

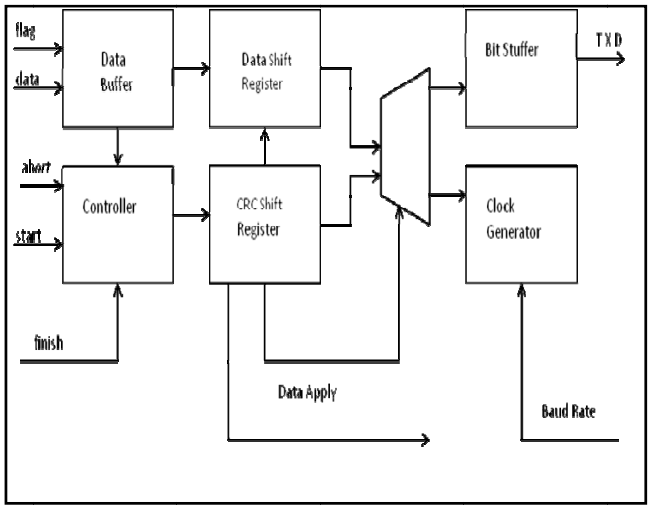

Figure 2: Channel Transmitter

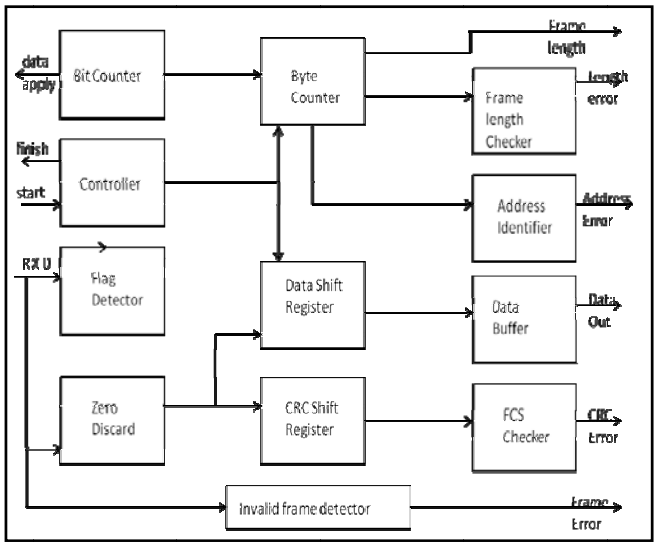

Figure 3: Channel Receiver

The top-down method is followed for designing the transceiver and a FSM is used for RAM management. The device utilization is as follows:

4 input LUTs: 854 out of 1536; 55%
IOBs: 51 out of 98; 52%
Block of RAMs: 8 out of 8; 100%
Slice flip flops: 610 out of 1536; 39%

This transceiver can be applied in bit-oriented packet transmission, is suitable for Frame Relay switches, Cable Modem, Private packet data networks and switches etc [6].

S. Hamed Javadi and Ali Peiravi has implemented a HDLC controller based on Modified MT8952B using Xilinx VirtexII FPGA. The transceiver designed works in two modes: normal mode and internal control mode.

The block diagram of the transceiver is as shown below:

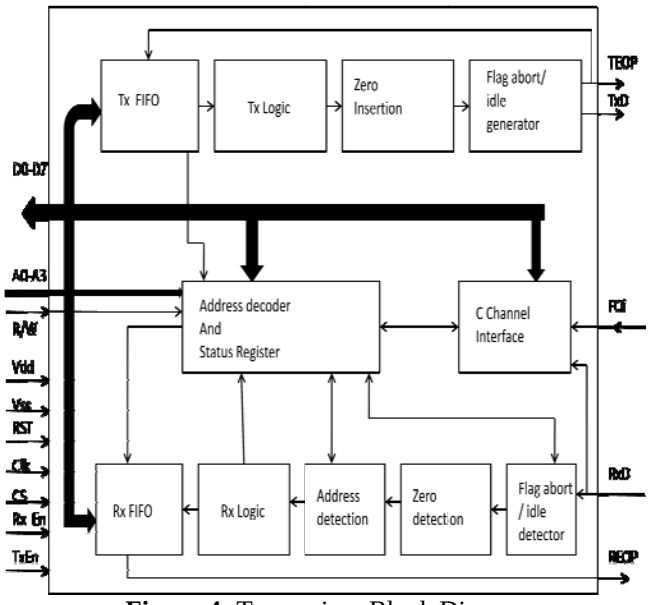

Figure 4: Transceiver Block Diagram

The design offered the following advantages:

- High bit rate 85 Mbps.
- Compatible with MT8952, Zarlink HDLC controller
- Compatible with ST Bus format.

This controller is suitable for packet switching and ISDN [2].

4. Conclusion

The HDLC is the basic module for communication of data in bit-stream form. Through the study of the various applications it can be deduced that the device is still important for error-less data transfer. The FPGA is used due to its advantages of flexibility, upgradability and customization. The memory required is mostly available internally when an FPGA is used. This increases the speed of the controller and makes it compatible with today's high speed technology. Also the controller can be simple or complicated depending on the features required.

Due to these advantages of FPGA technology, the HDLC controller can be built as a standalone multi-channel chip or embedded in large systems like SoC.

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