# Interfacing between High Performance Drivers and Low Power Devices using ABP Bridge

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**Abstract***: ARM introduced the Advanced Micro controller Bus Architecture (AMBA) 4.0 specifications in March 2010, which includes Advanced extensible Interface (AXI) 4.0. AMBA bus protocol has become the de facto standard SoC bus. That means more and more existing IPs must be able to communicate with AMBA 4.0 buses. Based on AMBA 4.0 bus, we designed an Intellectual Property (IP) core of Advanced Peripheral Bus (APB) bridge, it can translates the AXI4.0- lite transactions into APB 4.0 transactions. The bridge provides an interface between the high-performance AXI bus and low-power APB domain.*

**Keywords:** SoC; AMBA; AXI; APB

## 1. Introduction

Integrated circuits have entered the era of System-on-a-Chip (SoC), which refers to integrating all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on a single chip substrate. With the increasing design size, IP is an inevitable choice for SoC design. And the widespread use of all kinds of IPs has changed the nature of the design flow, making On-Chip Buses (OCB) essential to the design. Of all OCBs existing in the market, the AMBA bus system is widely used as the de facto standard SoC bus.

On March 8, 2010, ARM announced availability of the AMBA 4.0 specifications. As the de facto standard SoC bus, AMBA bus is widely used in the high-performance SoC designs. The AMBA specification defines an on-chip communication standard for designing high-performance embedded microcontrollers. The AMBA 4.0 specification defines five buses/interfaces [1];

- Advanced eXtensible Interface (AXI)
- Advanced High-performance Bus (AHB)
- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)
- Advanced Trace Bus (ATB)

## 2. Block Diagram

In this study, we focused mainly on the implementation aspect of an AXI4-Lite to APB Bridge. The APB Bridge provides an interface between the high-performance AXI domain and the low-power APB domain. It appears as a slave on AXI bus but as a master on APB that can access up to sixteen slave peripherals. Read and write transfers on the AXI bus are converted into corresponding transfers on the APB. The AXI4- Lite to APB bridge clock diagram is shown in Figure. 1.

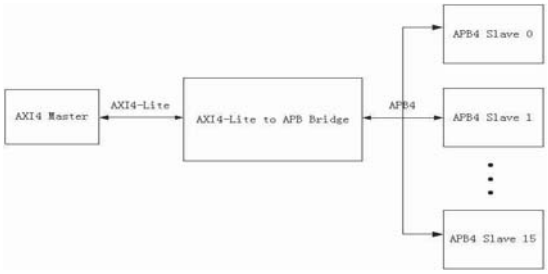


**Figure 1.** Block Diagram

## 3. AXI Handshake Mechanism

The VALID and READY handshaking mechanism in AXI allows both masters and slaves to control the flow of data. This can be problematic if, for example, a poorly designed master makes a write request while still assembling write data that is coming in from a slower or narrower interface. One real benefit of having the handshake mechanism is that slaves with long latencies can accept more requests than they have buffer space for. So, for example, an AXI PCIe slave may queue eight reads, but only have enough buffer space for four.

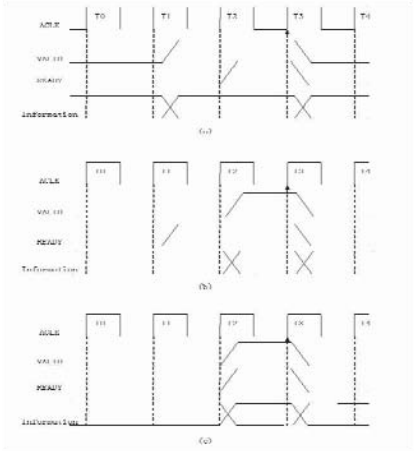

**Figure 2**. Handshake Mechanism

### 3.1 Asynchronous FIFO

An asynchronous FIFO refers to a FIFO design where data values are written to a FIFO buffer from one clock domain and the data values are read from the same FIFO buffer from another clock domain, where the two clock domains are asynchronous to each other.

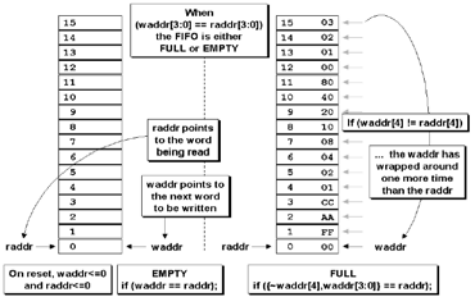


**Figure 3.** FIFO full and empty conditions

### 3.2 Mechanisms of AXI & APB

**Finite state machine**

A finite state machine is a mathematical abstraction sometimes used to design digital logic or computer programs [9]. It is a behavior model composed of a finite number of states, transitions between those states, and actions, similar to a flow graph in which one can inspect the way logic runs when certain conditions are met.

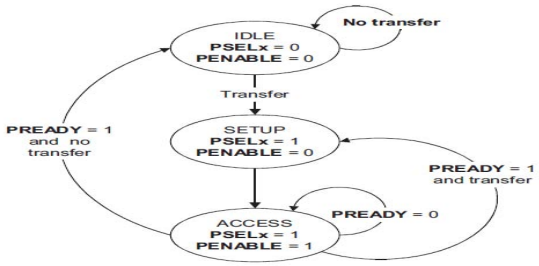


**Figure 4.** Operational activity of the APB

According AXI specification, the read address channel, write address channel and write data channel are completely independent. A read and a write requests may be issued simultaneously from AXI4-Lite, the AXI4-Lite to APB Bridge will give more priority to the read request than to the write request. That is, when both write and read requests are valid, the write request is initiated on APB after the read is requested on APB.

### 3.3 Advanced Peripheral Bus (APB) Protocol

The Advanced Peripheral Bus (APB) is part of the Advanced Microcontroller Bus Architecture (AMBA) protocol family. It defines a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow. Every transfer takes at least two cycles.

The APB can interface with the AMBA Advanced High-performance Bus Lite (AHB-Lite) and AMBA Advanced Extensible Interface (AXI).

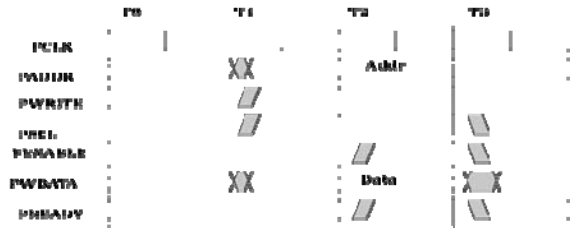


**Figure 5.** Write transfer with no wait states

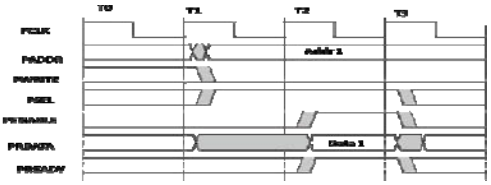


**Figure 6.** Read transfer with no wait states

## 4. Figures and Tables

### 4.1 Simulation and Synthesis Results

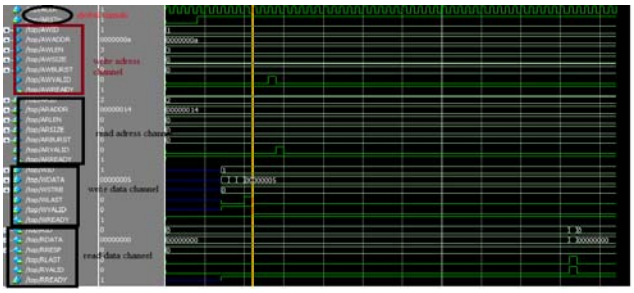

**Figure 7.** Different channels in AXI.

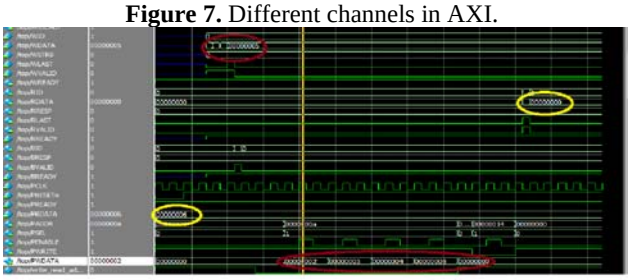

**Figure 8.** Data transfer between AXI and APB

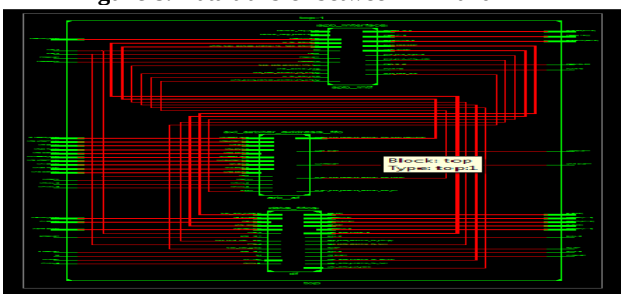


**Figure 9.** Technology schematic of APB Bridge

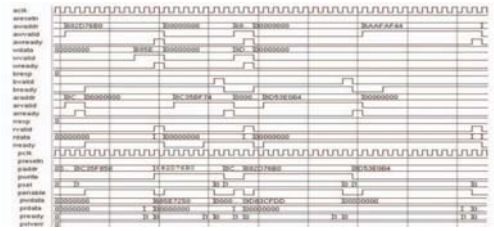

**Figure 10**. Typical Read and Write Transfer

### 4.2 Tables

**Table1.** Write address channel signals

| | *Source* | *Description* |
|---|---|---|
| AWID [3:0] | Master | Write address ID. This signal is the identification tag for the write address group of signals. |
| AWLEN [3:0] | Master | Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers |
| AWSIZE [2:0] | Master | Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update. |

**Table2.** Read Data Channel Signals

| *Signal* | *Source* | *Description* |
|---|---|---|
| RDATA[31:0] | Slave | Read data. The read data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide. |
| RRESP[1:0] | Slave | Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. |
| RLAST | Slave | Read last. This signal indicates the last transfer in a read burst. |

## 5. Other recommendations

**Applications**

- Computing**:** Net book, Smart book, Tablet, eReader, thin client.
- Mobile Handset**:** Smartphone's, Feature phones**.**

## 6. Conclusions

The APB Bridge provides an implementation of AXI4-Full to APB Bridge which has the following features:

- 32-bit AXI slave and APB master interfaces.
- PCLK clock domain completely independent of ACLK clock domain.
- Support up to 16 APB peripherals
- Burst length is 32 bits
- Support the PREADY signal which translates to wait states on AXI.
- An error on any transfer results in SLVERR as the AXI read/write response.

## 7. Future scope

- When read request and write request are simultaneously occurs the bridge gives the high priority to read request. This condition creates the race condition in APB Bridge.
- For example FIFO has only one date item to read operation. If read and write requests are simultaneously occurs the bridge first execute the read request and it read the single date item from the FIFO and now the read date FIFO was empty.
- Again read and write requests are simultaneously occurs again it execute read request but there is no data item in read data FIFO so transaction will fail. This situation is called race condition.

## References

[1] Design and Implementation of APB Bridge based on AMBA 4.0 (IEEE 2011), ARM Limited.
[2] http://en.wikipedia.org/wiki/System_on_a_chip#Structure
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[4] http://www.arm.com/products/system-ip/amba/amba-open-specifications.php
[5] ARM, "AMBA Protocol Specification 4.0", www.arm.com, 2010.ARM, AMBA Specification (Rev 2.0).

## Author Profile

**N. Sudhakar** received the B. Tech degree in Electronics and Communication Engineering from Jawaharlal Nehru technical university in 2006 respectively. During 2006-2010, he worked in Vijay Rural Engineering College (VREC) and Avanthi Engineering College as an assistant professor in Electronics and Communication Engineering department utilized signals and systems, analog communication, digital communication and electronic devices and circuits, microwave engineering, and antennas. He now with pursuing M. Tech in VLSI system design Anurag group of institutions (formerly CVSR College of engineering) in Hyderabad.