A Novel Pass Transistor Logic Based Pulse Triggered Flip-flop with Conditional Enhancement

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Abstract: ***For the past several years, much progress has been made in Low power VLSI Design .In this paper; we propose a novel low-power pulse-triggered flip-flop (FF) design with conditional pulse enhancement scheme. Pass transistor logic based AND gate is used for pulse generation which reduces circuit complexity and enhances faster discharge. The transistor sizes of the delay inverter and pulse-generation circuit are reduced for power saving. Simulation is performed for various pulse-triggered flip-flops to demonstrate the effectiveness of our proposed design using ami.05nm technology in Mentor graphics.***

Keywords: Flip-flop, low power, pulse-triggered

1. Introduction

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. One of the important factors is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the power consumption of the flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance.

This paper is organized as follows. In Section II, basics of sequential elements are described. Existing pulse-triggered flip-flops is shown in Section III. Proposed design is shown in Section IV. Section V discusses the simulation results. The paper ends with conclusion in Section VI.

2. Background

2.1 Basics of Sequential Elements

Sequential elements are mainly used to store computation result values for future use. At the minimal level of storage an element should be able to store logic “1” or “0” reliably.

Transitions on the inputs of a flip-flop may or may not lead to a state change. When input transitions do not change the

State, the internal switching inside the flip-flop consumes some power. On the other hand, when the input transitions do change the state, a bigger amount of power is consumed.

Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network.

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

3. Existing Pulse-Triggered Flip-Flops

3.1 Implicit Data Close to Output

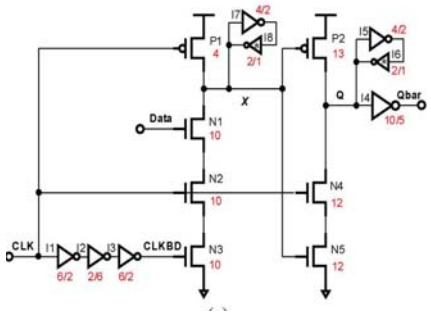

Figure 1. ip-DCO

A state-of-the-art P-FF design, named Implicit-Data Close to Output (ip-DCO), is given in Fig. 1. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3.

Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

3.2 Master Hybrid Latch Level Triggered Flip-Flop(MHLLF)

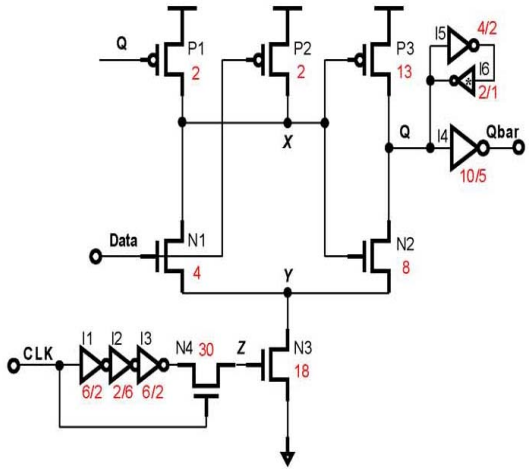

Figure 2. MHLLF

Fig. 2 shows an improved P-FF design, named Master Hybrid Latch Level Triggered Flip-flop (MHLLF), by employing a static latch structure. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1"

3.3 Single Ended Conditional Capture Energy Recovery (SCCER)

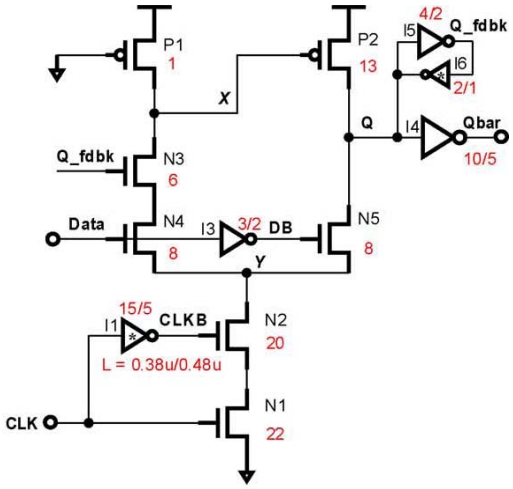

Figure 3. SCCER

Fig. 3 shows a refined low power P-FF design named Single Ended Conditional Capture Energy Recovery (SCCER) using a conditional discharged technique. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

4. Proposed Design

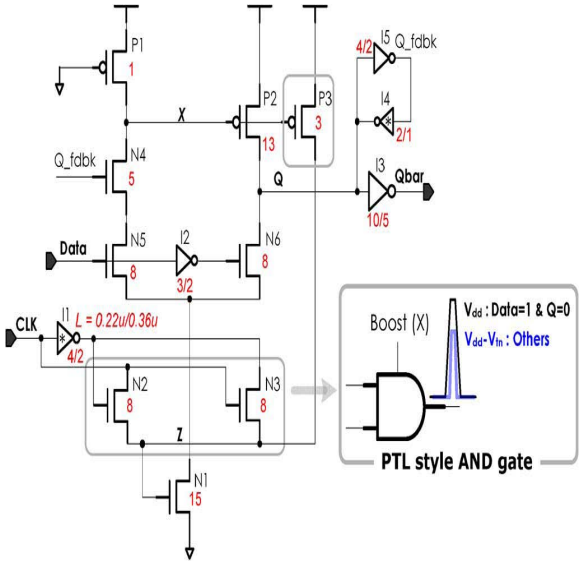

Figure 4. Schematic of the proposed P-FF design with pulse control scheme

The P-FF design with pulse control scheme, as shown in Fig. 4, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 4, the upper part latch design is similar to the one employed in SCCER design. As opposed to the transistor stacking design in Fig. 1 and 3, transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. It steps in when node X is discharged to $|V_{TP}|$ below the V_{DD}. This provides additional boost to node Z (from V_{DD}–V_{TH} to V_{DD}). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path.

The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

5. Simulation Results

The simulation results for the above various types of flip flops were obtained from MENTOR GRAPHICS in ami.05nm technology at room temperature. The supply voltage VDD is 5V. Simulation results for various P-FF designs are shown in Fig5.

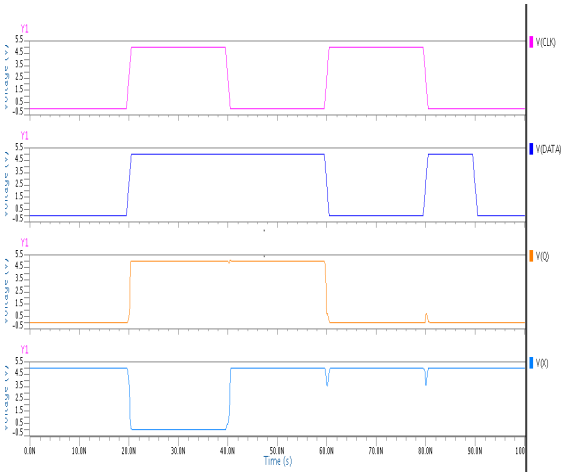

Figure 5(a). Waveform of ip-DCO

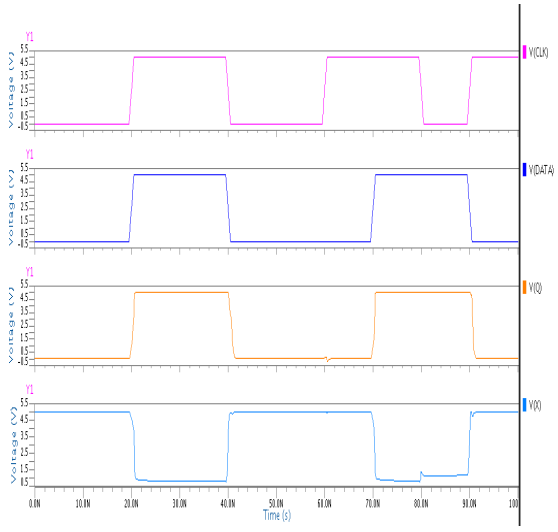

Figure 5(b). Waveform of MHLLF

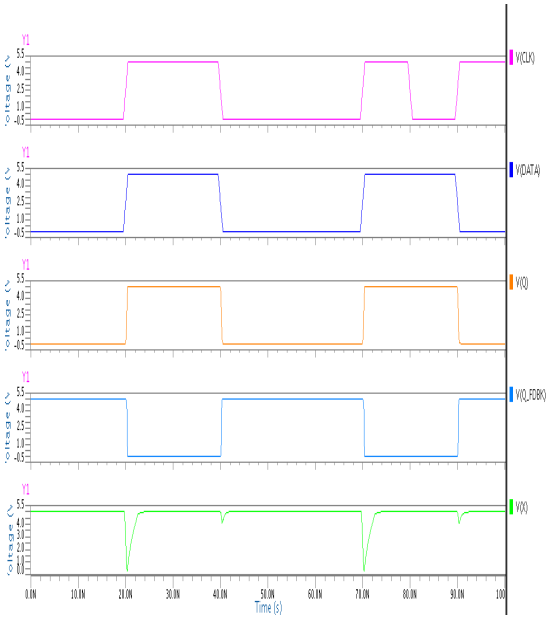

Figure 5(c). Waveform of SCCER

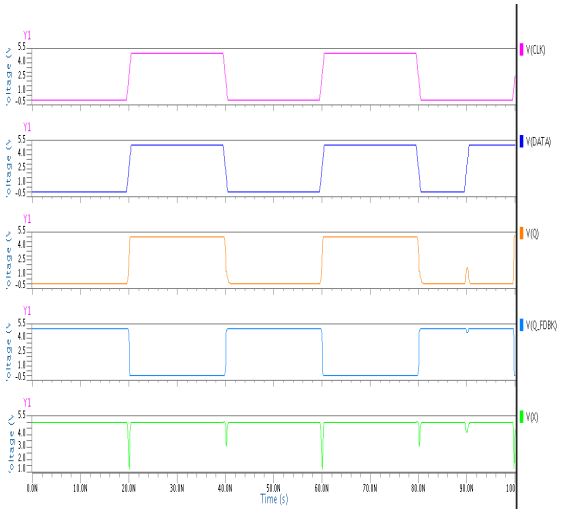

Figure 5(d). Waveform of Proposed P-FF Design With Pulse Control Scheme

Table 1. Feature Comparison of Various P-FF Designs

P-FF	*ip-DCO*	*MHLLF*	*SCCER*	*Proposed P-FF With Pulse Control scheme*
No of transistors	23	19	17	19
Power Dissipation (µW)	52.6038	41.9647	36.9508	19.9647
Data to Q Delay(Ns)	49.777	49.634	49.727	39.989
Discharge Time(Ns)	10	10	0.5	0.35

Table 1. summarizes some important performance indexes of these P-FF designs. A trade-off in performance occurs in the P-FF design

6. Conclusion

In this paper, we devise a novel low-power pulse-triggered FF design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum.

7. Acknowledgement

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