Reduction of Power in Active Mode by Automatic Monitoring and Control System

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Abstract: ***This paper describes a novel monitoring scheme to minimize total active power in digital circuits depend on the demand frequency, by adjusting automatically both supply voltage and threshold voltages based on circuit operating conditions such as temperature, process variations, and desirable frequency. The delay monitoring results, will be control and apply so as to be maintained at the minimum value at which the chip is able to operate for a given clock frequency. Design details of power monitor are examined using simulation framework in 32nm BTPM model CMOS process. Experimental results show the overhead of proposed circuit in terms of its power consumption is about 40 μW for 32nm technology; moreover the results show that our proposed circuit design is not far sensitive to the temperature variations and also process variations. Besides, uses the simple blocks which offer good sensitivity, high speed, the continuously feedback loop. This design provides up to 40% reduction in power consumption in active mode.***

Keywords: active mode, delay monitor, body biasing, VDD scaling, low power.

1. Introduction

Due to technology scaling, microprocessor performance has increased tremendously albeit at the cost of higher power consumption. Energy efficient operation has therefore become a very pressing issue, particularly in mobile applications which are battery operated [11]. The demand for increased battery life will require designers to seek out new technologies and circuit techniques to maintain high performance and long operational lifetimes [13]. Power in modern digital CMOS integrated circuits has traditionally been dominated by dynamic switching power, however, as technology scales leakage currents become increasingly large and must be taken into account to minimize total power consumption. In nano scaled CMOS devices, there are many leakage sources such as gate leakage, sub threshold leakage, BTBT based leakage, GIDL, DIBL, etc., [2]. The total power dissipation is given by the sum of switching dynamic power and sub threshold leakage power given by Equation (1) [13].

Pdynamic=CeffV2
Pleakage=VDDI0exp[ln(10)((nfkVDD)1/α–VDD)/S]
Ptotal= Pdynamic= + Pleakage (1)

Hence most applications do not always require the peak performance from the processor, Dynamic voltage scaling (DVS) was proposed as an effective approach to reduce power consumption, and is now utilized in a number of low-power processor designs [11].

It has recently been proposed that forward body bias (FBB) be used for microprocessors in the active mode. The FBB in the active mode improves performance and reduces sensitivity to variations in VDD, gate length, oxide thickness, and channel doping in the active mode. But the optimal bias condition (RBB, NBB, or FBB) for standby mode leakage minimization depends on the particular technology employed and is sensitive to process variations [12]. Process variations are classified as die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameter values. However, the devices on the same die are assumed to behave differently, in WID variations [15]. Furthermore; it has been shown in [15] that correctly applying body bias reduces the impact of die-to-die and within die parameter variations. Thus, applying the optimal body bias leads to both minimum leakage current and improved yield [12].

In the active mode, forward biasing the source–body junction, the transverse electrical field in the channel can be reduced, thus improves the carrier mobility and the transistor operation. On the other hand, in standby mode, reverse body bias is applied to reduce the off-state leakage current [6]. Forward biased there will be excessive sub-threshold leakage adding to the total leakage; if the body is reverse biased there will be excessive BTBT, also increasing the total leakage [5]. FBB is also considered as a promising solution to extend bulk-

Si CMOS scaling limit since short-channel behavior of MOSFET could be greatly improved under FBB [6]. The rest of this paper is organized as follows. In Section 2, presents a review of the previous works while Section 3 explains the main idea behind the proposed monitoring system. Experimental results are given and discussed in Section 4 with the conclusion in Section 5.

2. Background and Related Work

Dynamic voltage scaling (DVS) is a popular approach for energy reduction of integrated circuits. Current processors that use DVS typically have an operating voltage range from full to half of the maximum VDD. Equation (2) explains propagation delay, power and energy dependence on VDD [11].

Delay = 1/f = VDD/(VDD-VTH)1.3

Power ∞ f V_{DD}^2

Energy ∞ V_{DD}^2

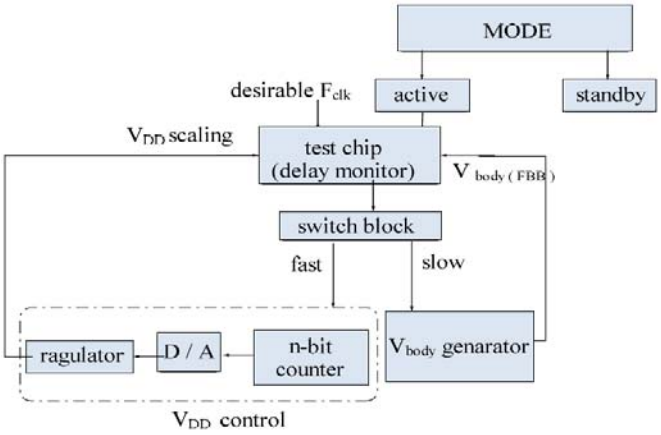

Figure 1: Proposed design for active mode

DVS is therefore an effective method to reduce the energy consumption of a processor, especially under wide variations in workload that are increasingly common in mobile applications. Hence, extensive work has been performed on how to determine voltage schedules that maximize the energy savings obtained from DVS. The optimal voltage limit depends on the power /delay trade-offs at low operating voltages [11]. Adaptive body biasing (ABB) works on the principle of applying reverse bias voltage (RBB)/forward bias voltage (FBB) to increase/decrease the threshold voltage of devices. This results in increasing gate delay while reducing leakage in case of RBB and vice versa in case of FBB. One can trade-off delay with leakage to achieve low leakage or high speed [4]. Forward bias reduces the BTBT current, but too much forward bias will cause excessive PN junction leakage as the junction becomes more weakly reverse biased. Reverse biasing the substrate to source junction of a MOSFET widens the bulk depletion region. This increases the threshold voltage and thereby reduces the sub-threshold leakage. This threshold voltage increase with reverse body bias is known as the body effect. Forward biasing the substrate to source junction has the opposite effect on the depletion region and thus increases sub-threshold leakage [12]. A number of previous works have used ABB for compensating process variations to improve design yield [1, 3, 2, 7]. In [12], the authors analyze the effect of body bias on leakage components and provide a methodology to obtain optimal body bias voltage for leakage reduction and process compensation in nano-meter devices. The work in [8] uses forward body biasing to reduce active leakage power. They propose to use high VTH devices for synthesizing the circuit and then use forward body biasing to speed up only a set of gates to achieve original timing, they do not compensate for timing variability. In [9,10] have been described delay and power monitoring schemes for minimizing power consumption by means of dynamic control of supply voltage and threshold voltage in active modes.

3. Proposed Monitoring System

To reduce leakage power in active mode, this paper proposes a new circuit design which determines the optimal reverse body bias voltage and optimal supply voltage, by using the adaptive body bias (ABB) technique to compensate die-to-die parameter variations. The proposed circuit is a delay monitoring scheme which consider the process, voltage, and temperature (PVT) variations, without any extra monitor and control circuits. Reference [7] is mentioned PVT variations but it is used the circuit with the high overhead to control PVT variations. Fig. 1 illustrates the diagram of proposed design which considered active mode. Here we briefly explain system operation in the standby mode, then demonstrate it with more details.

3.1 Standby Mode

In this mode are used a total leakage current monitor circuit, comparator, and the body voltage generator. The total leakage monitor circuit is used to monitor the leakage current during standby mode directly from a given load circuit. Our new design technique automatically generates the optimal body bias voltage during standby mode, by monitoring the total leakage current ($I_{leakage}$) and comparing the value of Ileakage at the time of t0 and t1 (t1 > t0). This system increases VTH by adjusting body voltage in the RBB direction, so reduces total $_{leakage}$ current [14].

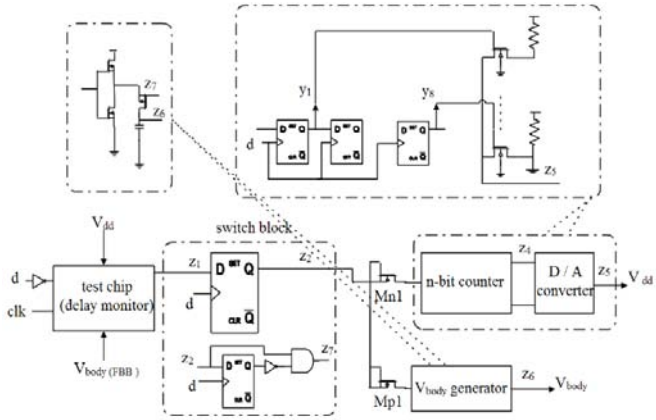

Figure 2: Expanded proposed V_{DD} / V_{TH} monitoring Circuit

3.2 Active Mode

Depend on the demand frequency of the load circuit, in many cases the peak performance from the processor, is not necessary to use, so we can management the energy consumption by reducing supply voltage insofar as desirable speed, with considerate to the demand frequency. As Fig. 1 illustrates the diagram of proposed design in active mode, we exploit VDD/VTH control system to control power and speed in active mode. This diagram consist of a test chip, which is a critical path replica circuit to reflect the delay characteristics of the critical paths under process, voltage, and temperature (PVT) changes, with beneficial of this test chip we can monitor if the circuit works fast or slow and then The VDD/VTH control switching block decided to utilize VDD control or VTH control system. In the case it works faster than needed we reduce VDD to prevent extra power consumption, and if it works slower than needed speed, VTH control will be active to compensate delay by using FBB technique. Circuit propagation delay is high

sensitive to VDD variation so if the circuit works fast, we should precisely reduce supply voltage. Fig. 2 shows expanded proposed VDD/VTH monitoring circuit in active mode, with feedback loop, a key component of this controller circuit. VDD and VTH are changed on the basis of reference voltages by feedback control. In the first step the clk signal with the desirable frequency, and signal 'd' with half of the clk frequency(period time=T1) fed to the test chip, Fig. 3 shows a timing chart of the control and output signals of delay monitoring circuit. If signal d pass the test chip during T1, as shown in signal z1(during first period of d) in Fig. 3, it means that test chip speed is faster than clk frequency, in this step we can precisely reduce VDD, to reduce power consumption. For activate VDD controller block, the D flip flop had been applied which works with signal'd' as clock. Switch block selects either VDD control or VTH control, will be active. Table I summarizes truth table for the VDD/VTH control circuit for each states which delay monitor encounters harmonize to Fig. 3. In the case z2=1, VDD control mode will start to work, which helps to maintain the desirable circuit speed and to minimize switching power consumption. This block consists of n-bit counter, analog to digital circuit and at the end, a regulator to amplifier the output current. Eight D flip flops constitute 8-bit counter, we can set the number of supply voltage steps by the value of n, whatever the value of n is greater, supply voltage steps will be more accurate. At last a simple D/A converter have been introduced to denote desirable supply voltage. In the case signal 'd' cannot pass the test chip during T1 period as signal z1(during third period of d) in Fig. 3 shows, it means that test chip speed is slower than clk frequency, so z2=0, VDD control will stop and VTH control mode will start to compensate extra delay, this block utilize an inverter and a capacitor. By charging or discharging the output capacitor the optimal VTH will be generate. This system decreases VTH by adjusting body voltage in the FBB direction, so increasing the device speed at the expense of increased leakage power.

Switching block will automatically hold VDD and VTH values depend on current state and previous state of Z2. These values are maintained by feedback control. D flip flop helps to have Z2 value on current state and previous state contemporaneous, when d changes from 0 to 1, Z2 value on the previous state fed to D flip flop, there for inputs of AND gate will be ready, to generate Z7. The proposed scheme uses the simple blocks which offer the advantages, such as good sensitivity, high speed and the feedback loop continuously works.

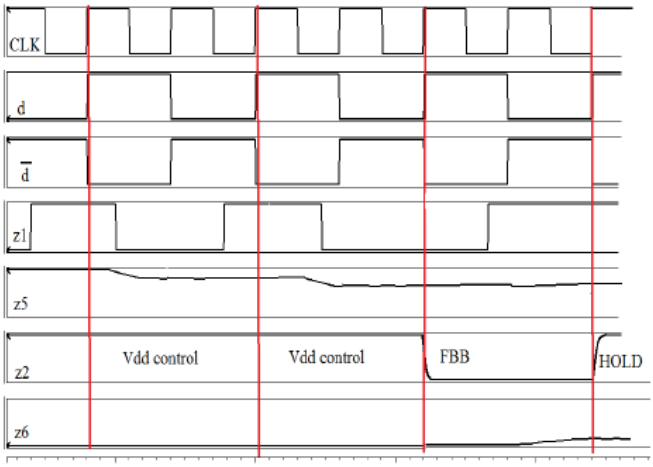

Figure 3: Timing Chart of Control and output signals

Table 1: Truth Table for the V_{DD} / V_{TH} Control Circuit

# Clk	$Z_2(V_{DD}/V_{TH})$	Z_7(active/hold)	Operation
2	1	0	V_{DD} control
4	1	0	V_{DD} control
6	0	0	V_{TH} control
8	0	1	HOLD

The proposed circuit is an automatically VDD/VTH controlling scheme using the critical path replica circuit, which reflect the delay characteristics of the critical paths under process, voltage, and temperature (PVT) variations conducted to reduce delay margin and to achieve lower power consumption.

4. Experimental Results

In this paper we propose a new circuit to determine the optimal supply voltage and optimal body bias voltage with low overhead, in active mode. Simulation results in this paper, has been implemented in HSPICE for 32nm, we used Berkeley Predictive Technology process models (BPTM) to perform all experiments for 32nm BPTM technology node. For the technology bellow 90nm the ITRS road map predicts that leakage power easily wins over dynamic power. Therefore, it is important to have efficient and accurate estimation of total leakage currents from all sources. Our monitor and control circuit has been implemented and evaluated using chain inverter circuit designed. The propagation delay of the chain inverter, replicate critical path of the main circuit. Table II shows the summary of the results for the proposed approach at 32nm technology and typical corner (TT), for three desirable clk frequencies. The average power consumption has been measured at 0.9V supply voltage; as shown Table II, this design provides up to 40% reduction in power consumption in active mode, compared to the cases where any reduction techniques are not used at all. In order to show the efficiency of the proposed methodology against temperature variations, test circuit is simulated at three temperature conditions (25o C, 50o C and 100o C). Also, to demonstrate the proficiency of the system, it is simulated at different process-corner conditions (SS, FF, SF and FS). Fig. 4 (a) shows the experimental results of the chain inverter circuit at different process corner conditions, different demand frequency and at

two temperatures, for both cases, without optimization and by applying our proposed monitor and control VDD/VTH circuit to the test circuit in 32nm technology. Fig. 4 (b) illustrates optimal values of supply voltage and body bias voltage, for above cases. It is obvious optimal VDD is lower than its nominal value. For the designs which are slower than nominal due to process, voltage, temperature variations and circuit aging, this circuit leverage FBB to speed-up that, this condition mentioned at for 100oc. Overhead of proposed monitoring circuit in terms of its power consumption is about 40 µW for 32nm technology. This power dissipation is very small compared with the power consumption of the general digital cores. In the case of nano-scale circuit process variation maintaining the circuit yield is the most important design challenge, when the proposed technique is applied to the test chip besides the circuit yield safeguard and demand performance compliance, power dissipation is reduced. A previous study has shown that a critical path replica consists of gate delay, RC delay, and rise/fall delay components, and that it can track well, with good voltage accuracy [9].

Table 2: Results for the proposed approach at 32 NM Technilogy and Typical Corner (IT)

Frequency	Without optimization (uw)			With optimization (uw)			Optimal V_{DD} (v)			Optimal Vbody-pmos (v)			Optimal Vbody-nmos (v)		
	25°c	50°c	100°c	25°c	50°c	100°c	25°c	50°c	100°c	25°c	50°c	100°c	25°c	50°c	100°c
1 GHZ	120.67	139.9	155	108.24	128.1	161.57	0.8	0.85	.9	0.7	0.7	.6	0.2	0.2	.3
.5 GHZ	80.2	97.12	120.37	55.20	66.43	79.58	0.7	0.75	0.8	0.7	0.8	.8	0.2	0.1	.1
.25 GHZ	56.8	60.69	65.38	32.8	36.41	37.42	0.65	0.65	0.7	0.8	0.8	.8	0.1	0.1	.1

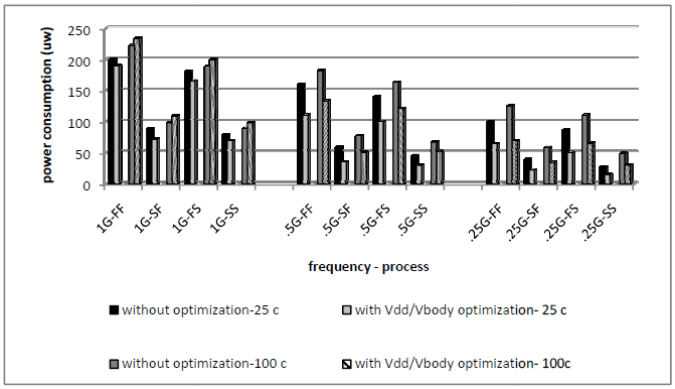

Figure 3: Power Consumption Vs Frequency Process

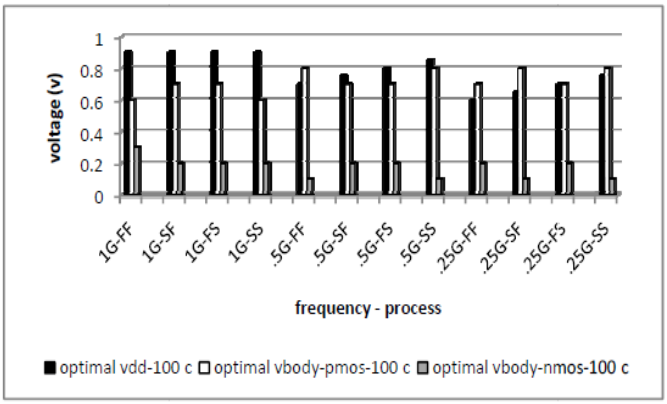

Figure 4: Voltage Vs Frequency Process

5. Conclusion

Low power considerations are becoming increasingly important in modern integrated circuits. As portable battery powered devices become more complex and prevalent, the demand for increased battery life will require designers to seek out new technologies and circuit techniques to maintain high performance besides achieve minimum power consumption and long operational lifetimes. In this paper we have described a monitoring scheme for minimizing power consumption by means of Vbody control in standby mode and VDD/VTH control in active mode. The proposed system is very effective and practicable in reducing the power dissipation in the big circuits with the minimal hardware overhead of transistors and the minimal power overhead, moreover the continuously feedback loop control and adjusted optimal VDD and Vbody automatically, depend on PVT and frequency variations.

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