FPGA Implementation of Picoblaze based Embedded System for Monitoring Applications

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Abstract: ***The microprocessors are used for executing instructions by fetching from memory. The processor interact with other peripherals, it requires additional circuitry .This makes system complexity ,requires large area and high power consumption .To overcome this problem the microprocessor itself capable to handle peripherals up to its limit. This feature comes in Pico Blaze microprocessor. Pico Blaze is a 16-bit soft core microprocessor developed by Xilinx that can be synthesized in some FPGA families. In this design a set of peripherals that have been developed to interface with Pico Blaze. They are PS/2 keyboard port, Light monitor control serial communication. The system has been implemented in a FPGA board and some typical control and monitoring systems have been developed. Pico Blaze is aimed to replace large finite-state machines in low- to mid-complexity designs by the advancement of programmable logic devices CPLD /FPGA and with the help of hardware descriptive languages. The system has been implemented in a FPGA board and some typical control and monitoring systems have been developed.***

Keywords: Verilog, VLSI, FPGA

1. Introduction

The project aims at making the monitoring system by using Pico Blaze soft-core processor connected the peripheral blocks and transducer controls the monitoring system based on user requirement. The project uses the soft-core microprocessor and Embedded System to design this application. The main objective of this project is to design a system that continuously checks the peripheral readings and controlees the system accordingly.

In this project the embedded system is customized by adding a set of peripherals, described in Verilog HDL, that are intended to extend the capabilities of Pico Blaze. Developed basic monitoring tasks built around this Pico Blaze-based embedded system. The set of peripherals that have been developed to interface with Pico Blaze are serial communication, PS/2 keyboard port and light controller monitoring. To demonstrate its capabilities, the system has been implemented in a FPGA board and some typical control and monitoring systems have been developed. The measure of efficiency is based on how fast the microprocessor can read the data, detect the signal received and make it off or on. The system is totally designed using VerilogHDL and embedded systems technology.

The performance of the design is maintained by Pico Blaze unit and peripherals. Pico Blaze is a 16-bit microprocessor soft core aimed to replace large finite-state machines in low- to mid-complexity designs.

Simulations are done using Modelsim tool. Synthesis and FPGA implementation of the project is carried out using Xilinx ISE 12.1 tool.

2. PicoBlaze Microprocessor

PicoBlaze is a 16-bit microprocessor developed by Xilinx that can be synthesized in the following FPGA families (in its KCPSM3 version): Spartan3, Virtex-II and VirtexIIPro [4]. Figure 1 shows the components of PicoBlaze. PicoBlaze is instantiated as three VHDL modules. Two internal components: (1) KCPSM3 encapsulates the operation of the microprocessor and (2) a block memory contains the program to be executed. Both components are encapsulated by a third parent component.

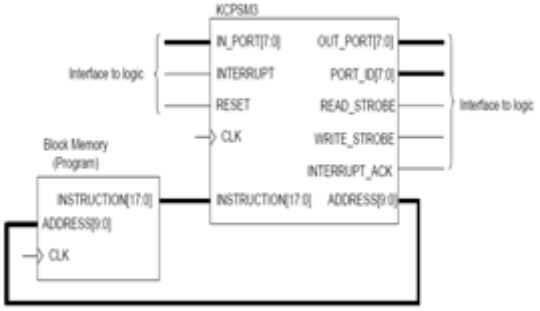

Figure 1: Internal components of PicoBlaze (after [4])

2.1. Programming

In its current release, PicoBlaze is programmed in assembly language. The instruction set is composed of fifty seven instructions, which can be classified as: program control, arithmetic, logic, interrupt and input/output.

2.2. Tools and development flow

The assembly language code that is to be run by PicoBlaze is developed as a text file with a psm extension.

This file is fed into the KCPSM3 program to generate the program memory as a VHDL module, which can then be attached to the microprocessor.

The software application and the hardware implementation help the Verilog HDL and the data from peripherals and accordingly change the condition of the system. This way, the debugging process of the microprocessor can entirely be conducted in the hardware side.

2.3 Microprocessor capabilities

Among the main features of PicoBlaze are;

- 1K addressable program memory
- Up to 256 input/output ports
- One interrupt port with acknowledge
- 64 bytes of scratch pad memory
- Zero and carry flags
- 31-level hardware stack

3. Peripheral blocks

The selection of the peripherals that have been added to the system has been based on the capabilities of the Spartan-3 FPGA board [5], a schematic of which is shown in Figure 2. Among the main features of the board are: eight LED, eight slide buttons, four push buttons, 1 Megabyte of static RAM, PS2 keyboard socket and three 40-pin expansion connectors. The peripherals that have been developed are: an LCD controller, a PS/2 keyboard controller, a VGA controller and a serial communication module. Details of design are given next.

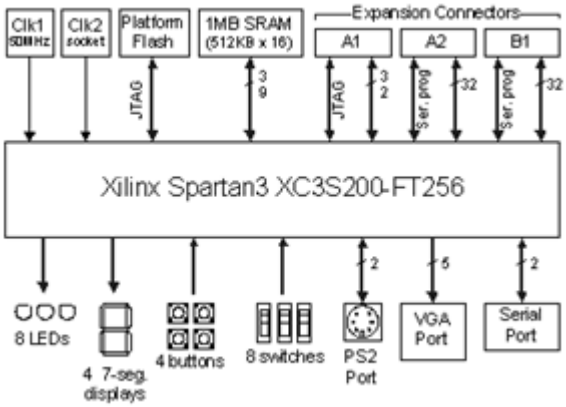

Figure 2: Schematic diagram of the Spartan 3 FPGA board (after [5])

3.1 PS/2 keyboard controller

A controller that allows the communication between PicoBlaze and a PS/2 keyboard has been developed. This design is based on a controller that has been previously reported [7]. However, a set of registers has been added to the controller to facilitate the communication with PicoBlaze. Figure 4 shows a diagram with the internal organization of the keyboard controller, as generated by the synthesis tool. The implemented communication with the keyboard has only one direction: from the keyboard to PicoBlaze. The communication routine in assembly

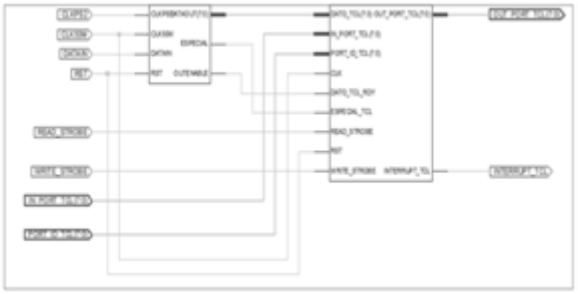

Figure 3: Keyboard controller

3.2 Serial communication

The PicoBlaze development kit provided by Xilinx includes a VHDL description of a basic UART. Likewise, Spartan-3 board provides all the facilities to enable serial communication: a DB-9 port and a voltage-level shifter circuit. In order to enable PicoBlaze to handle a UART as a peripheral, both the transmitter (Tx) and receiver (Rx) modules have been encapsulated along with an interface module. This interface allows PicoBlaze to operate the UART by accessing a set of registers.

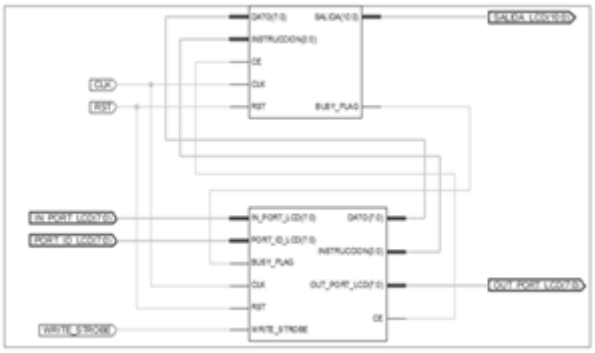

Figure 4: Serial communication peripheral

The register-based interface of the UART supports the following features

- Enabling/disabling Tx interrupt
- Enabling/disabling Rx interrupt
- Clearing Tx and Rx interrupt flags
- Writing the Tx data
- Reading the Rx data

4. Complete Embedded System

The peripherals presented in the previous section have been integrated along with a single instantiation of PicoBlaze. Since each peripheral is provided with a set of registers that PicoBlaze can access, all the registers have been given an identifier so that PicoBlaze can use it to access a specific register. The complete embedded system has been used in the implementation of monitoring tasks to demonstrate its functionality. The working environment of these monitoring applications are as follows: keyboard monitor represent the workstation where the system is allocated, while the serial communication module enables a remote access to the system in order to either query the present condition of the task or reconfigure the operation of the system. Next session provides more details on the monitoring applications.

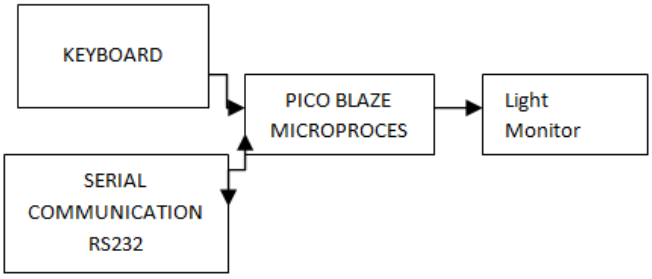

Figure 5: Block Diagram of Picoblaze based embedded system

5. Monitoring applications

Each application has been synthesized by Xilinx ISE and implemented in the FPGA board of Figure 2.

5.1 Simulation Results

The PicoBlaze based application is realized using Verilog HDL code of the PicoBlaze processor. Once the design is done initially Simulations have been carried out using Modelsim tool. The simulation results are shown below figure Waveforms show in these figures indicate address, clock, data and other input and output signals related to the project the data& corresponding to address for each cycle is presented. After successfully completing the simulations the synthesis is done using Xilinx ISE tool. After synthesis Place and route is done for the XilinxXC3S200 FPGA and bit file is loaded on the FPGA board.

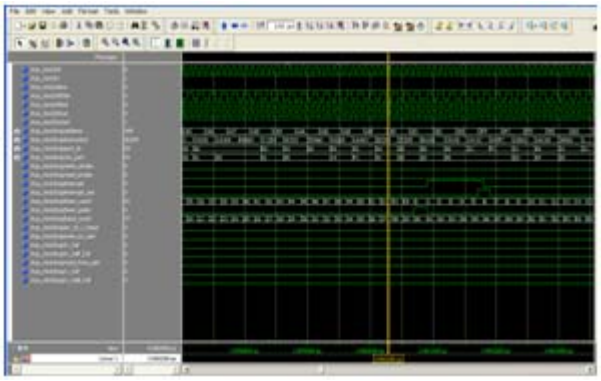

Figure 6: Simulations Results showing RS-232Tx signal

6. Conclusion

Soft core system is a one of the significant technology in present days. Undoubtedly, the industrial automation application is one of the key issues in developing Pico Blaze. The utilization of soft core technology is novel and might enhance the existed Testing and automation system. With this project we are proposed too optimizing the memory, simultaneously increase the machine power for accurate results with minimum time .Due to increasing the performance no need to spend much more money for other controlling elements, automatically the cost of the product will be get normal rates. A PicoBlaze based Embedded System was successfully designed and implemented in this project.

The design of four peripherals for PicoBlaze soft core microprocessor has been presented. The design approach consisted in VerilogHDL descriptions and register- based interfaces. Monitoring control applications have been developed around PicoBlaze and the designed peripherals and implemented in the Spartan-3E FPGA board. Experimental results demonstrate the validity of the proposed system.

7. Future scope

Pico Blaze is a soft core RISC processor. Its power lies in its architecture where it uses simple components and a very simple interconnects. This leads to high speed implementation due to reduced combination l delay in critical path .However, its non-pipelined architecture leads to a slower implementation.

The speed can further be increased by making the architecture pipelined. The area would increase because of addition of pipelined registers and them architecture also needs to be slightly modified so that no overlapping transfers are done in between the instructions. For auto mobile industries usage of pico Blaze technology in industrial automation may lead to the wide and far-reaching adaption of every area.

Some more comprehensive and advanced control methods and their corresponding control commands, with heavy payload, speed increase and decrease with and without obstacles. This type of Soft core can also be designed and implemented accurately, the limitation that some of the applications faced were the program memory of PicoBlaze. This led to the inclusion of more PicoBlaze instances in the system. Exploration of schemes of communication between microprocessor instances is underway.

8. Acknowledgements

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