Utilizing Serial Interface to Make Effective Communication for 16X2 LCD

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Abstract: ***Advancements in technology for chip manufacturing are leading to the device which incorporates various functionalities within single chip. So as to reduce the complexity and size of the overall printed circuit board .Keeping the same idea in mind, lots of embedded project require to interface with 16x2 LCD or character LCD, which is one of widely used LCD available in market, with growing complexity and need to provide lots of functionality within the same size, the pins provided on the controller remains same, now it become difficult to share pins of the controller, the present work reflects about the working model which describes a technique to reduce the pin requirements of pin hungry interfaces for example considering 16x2 LCD normally if one has to interface such LCD's, they need to dedicate at least 6 pins or at maximum 11 pins of a controller. Since we are moving towards lesser number on to pin's, thus we want to take initiative towards development of such device.***

Keywords: LCD, UAR, UART, µC

1. Introduction

Concept of this application is to provide proper writing our data on to the LCD without wasting time and recourses unnecessary. The first and foremost question arise in our mind that in this era of high speed and faster world why we need for interfacing the LCD since we know that LCD is very slow device and generally need at least ten to eleven pins for writing from the controller. The controller will takes much time to write on LCD which is not a worth full and profitable application.

LCD

The 16x2 LCD is very popular because of its built in HD44780 interface module. This module makes it extremely easy to add an LCD to any project with its built in character Set and easy command structure LCD – Liquid Crystal Display Lower power than LED display. More flexible in size and shape slower response time The LCD's internal controller can accept several commands and modify the display accordingly. These commands would be things like:

- Clear screen
- Return home
- Decrement/Increment cursor

We need to insert time delay between any two commands or data sent to LCD. So for achieving a faster device we develop a device which will takes lesser number of pins approx two and lesser time to write data with in some nano seconds, so that one can interface LCD over standard serial protocol such as UAR.

The 16x2 LCD interface has 8 data bits (DB0~DB7) and 3 control pins (RS, R/W*, E). The data bits are connected to the 8 pins of ***µC***.

Figure 1: 16x2 LCD

The motive of this device is to develop a bridge between character LCD and UAR. Although, the design and the function will explain whole propose methodology of LCD interfacing with lesser port.

1.1 Schematics

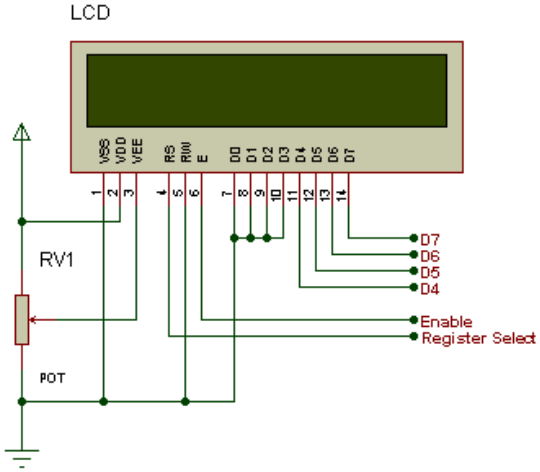

Figure 2: Schematic diagram of 16x2 LCD

Above is the quite simple schematic. The LCD panel's Enable and Register Select is connected to the Control Port. The Control Port is an open collector/open drain .While most Parallel Ports have internal pull-up resistors. We make no effort to place the Data bus into reverse direction. Therefore we hard wire the R/W line of the LCD panel, into write mode. This will cause no bus conflicts on the data lines. As a result we cannot read back the LCD's internal Busy Flag which tells us if the LCD has accepted and finished processing. Above is the simple schematic. The LCD panel's Enable and Register Select is connected to the Control Port. The Control Port is an open collector/open drain .While most Parallel Ports have internal pull-up resistors. We make no effort to place the Data bus into reverse direction. Therefore we hard wire the R/W line of the LCD panel, into write mode. This will cause no bus conflicts on the data lines. As a result we cannot read back the LCD's internal Busy Flag which tells us if the LCD has accepted and finished processing the last instruction. This problem is overcome by inserting known delays into our program.

Pin No:	*Name*	*Function*
1	VSS	This pin must be connected to the ground
2	VCC	Positive supply voltage pin (5V DC)
3	VEE	Contrast adjustment
4	RS	Register selection
5	R/W	Read or write
6	E	Enable
7	DB0	Data
8	DB1	Data
9	DB2	Data
10	DB3	Data
11	DB4	Data
12	DB5	Data
13	DB6	Data
14	DB7	Data
15	LED+	Back light LED+
16	LED-	Back light LED-

Figure 3: Pin function of 16x2 LCD

VEE pin is meant for adjusting the contrast of the LCD display and the contrast can be adjusted by varying the voltage at this pin. This is done by connecting one end of a POT to the Vcc (5V), other end to the Ground and connecting the centre terminal (wiper) of of the POT to the VEE pin. See the circuit diagram for better understanding

1.2 UAR

A universal asynchronous receiver, abbreviated UAR, is a type of "asynchronous receiver/", a piece of computer hardware that translates data between parallel and serial forms data and transmits the individual Data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. The UART usually does not directly generate or receive the external signals used between different items of equipment. Separate interface devices are used to convert the logic level signals of the UART to and from the external signaling levels bits in a sequential fashion. A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly Universal Asynchronous Receiver takes bytes**.** External signals may be of many different forms. Examples of standards for voltage signaling are RS-232, RS-422 and RS-485 from the EIA. Communication may be "full duplex" (both send and receive at the same time) or "half duplex" (devices take turns transmitting and receiving).

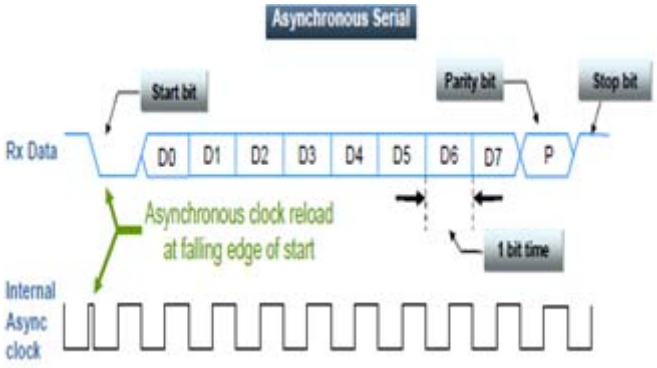

Figure 4: Asynchronous serial communications

A UART takes a parallel data stream and funnels it down to a serial data stream at the transceiver end and then returns the data stream to a parallel signal at the receiver end.

- This lowers the cost of connection by decreasing the number of transceivers that are necessary.
- Enabling the connecting cable to be less costly and less bulky.
- A UART takes a parallel data stream and funnels it down to a serial data stream at the UARTs are useful in applications that require a bandwidth of 3 Mbps if a LVDS transceiver/receiver is used and a bandwidth of up to 500 kbps if a RS232 receiver is used.
- Most computers and microcontrollers have one or more serial data ports used to communicate with serial input/output devices.

1.3 Receiver

All operations of the UART hardware are controlled by a clock signal which runs at a multiple (say, 16) of the data rate - each data bit is as long as 16 clock pulses. The receiver tests the state of the incoming signal on each clock pulse, looking for the beginning of the start bit. If the apparent start bit lasts at least one-half of the bit time, it is valid and signals the start of a new character.

If not, the spurious pulse is ignored. After waiting a further bit time, the state of the line is again sampled and the resulting level clocked into a shift register. After the required number of bit periods for the character length (5 to 8 bits, typically) have elapsed, the contents of the shift register is made available (in parallel fashion) to the receiving system.

1.4 Field Programmable Gate Array

FPGA is an integrated circuit that contains many identical logic cells that can be viewed as standard components. Each logic cell can independently take on any one of a limited set of personalities.

Field Programmable concept

Field Programmable means that the FPGA's function is defined by a user's program rather than by the manufacturer of the device.

Applications of FPGA

Applications of FPGAs include DSP, software-defined radio, aerospace and defense systems, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, and a growing range of other areas.

FPGA Design Flow

The FPGA based Design Flow is extensively used in today's world due to

- Design Entry
- Synthesis
- Simulation
- Implementation
- Program

2. Contribution

The motive of this device is to develop a bridge between character LCD and UAR. Although; normally it takes up to ten no. of pins to establish this interface where as we are developing an interface which requires only one pin. The circuit diagram will explain whole methodology and functionality to develop the LCD interfacing with lesser port. Further the proposed design will indicate how the LCD and UAR controller's function and performance are all achieve with design target.

3. Proposed Design

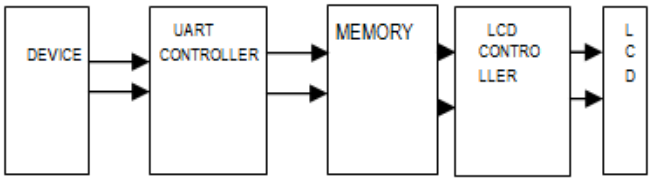

Figure 5: Block diagram of LCD interfacing

In this block diagram describing how 16x2 LCD will develop serial interfacing. In which a universal asynchronous receiver/transmitter will require for interfacing of LCD with the ***μC***. In this diagram UART devise will transmit signal of 8 bit data serially to the UART controller. UART controller will control the performance of UART device from where 8 bit data will send to the memory. Memory will store this 8 bit data. This 8 bit data is taken by LCD controller as input signal. LCD controller is used for controlled transmission and data will send to the LCD in parallel form. By this process we can develop serial interfacing of 16x2 LCD with ***μC***. This design will help in controlling and operating any LCD which is placed at far end through μC by the help of universal asynchronous receiver.

3.1 Detail circuit description

I. This data will be stored in the dual port memory. Dual port memory is a memory which is used to read as well as to write stored data. So memory will receive data by the receiver of UART device and this store data will be send to the LCD with the help of LCDFSM block. Memory and receiver's operations are controlled by the memory controller.

II. LCD FSM is a device used as controller which will generate signal of read and write for memory as well as generate two signals of enable and RS to LCD.

RS is a resister select control pin used as in two modes in command mode and also in data mode. By this circuit LCD will interface by the ***μC***.

In this circuit diagram PC will transmit 8 bit data serially with the help of UART device to the RXD under FPGA board and baud rate generator will set standard baud rate for the receiver block to receive data from PC. The number of bits transmitted per second is often referred to the BAUD rate.

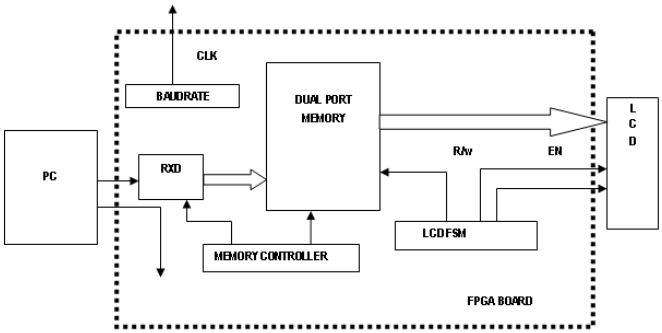

Figure 6: Detail circuit diagram of 16x2 LCD with pc

- R/W = 0 → Write , R/W = 1 → Read
- E = Enable
- Used to latch the data present on the data pins.
- RS = Register Select
- RS = 0 → Command Register
- RS = 1 → Data Register

4. Literature Survey

Majorly the main concern of the designer here is on reducing the complexity of cables and pins to acquire the bridging between the ***μ***c and LCD. This will reduce the extra resources which give achieve lesser capita as economical application and increase the performances of the controller. This paper provides the application which takes only one pin count for a ***μ***C for interfacing with LCD. This is the new achievement till now no such type of device had developed and no work had done on this paper. UAR is also used in this as a reviser controlling device. To improve performance of device she incorporates a module between the controllers to reduce the number of pins to transfer data from the controller.

5. Results and Conclusion

After implementing the design on tool XYLINX we found this fig1which shows the RTL viewer having mux and all the gates which are been used here. And on the fig2 shows simulation waveform as a result of LCD receiving of data on it. The function of LCD controller is on clk_in, rs, lcd_en, ps, data _out is set high for writing data on it. This concludes the required result of device which reduces the pin count to one for whitening on LCD with in 1ms.

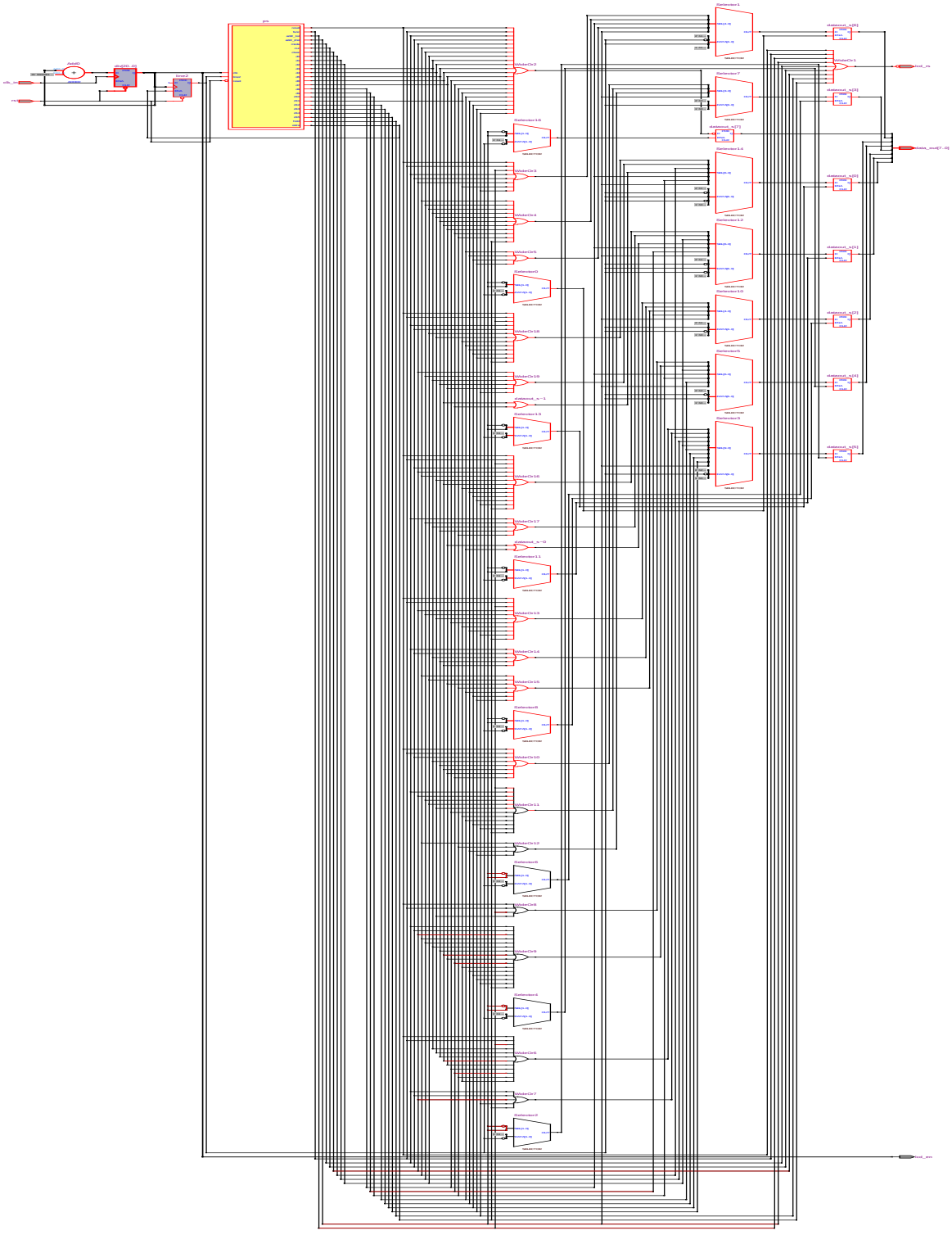

Figure 7: RTL viewer

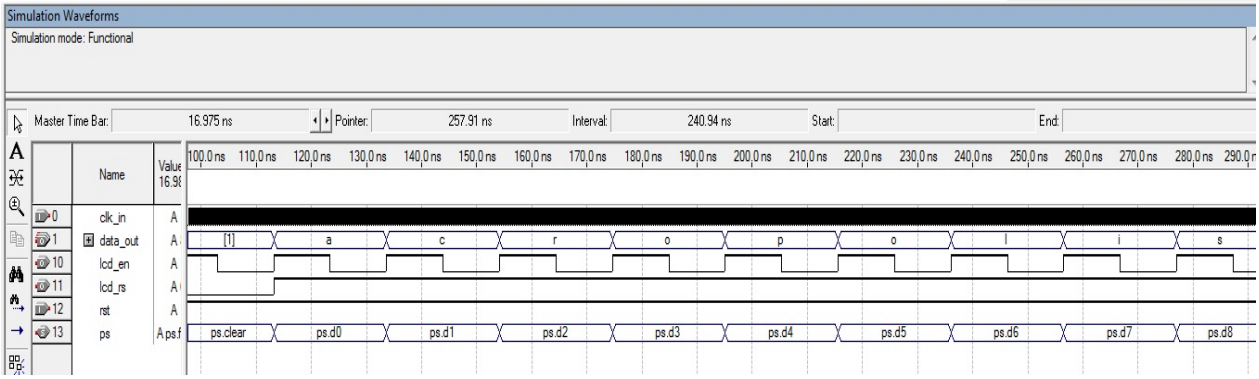

Figure 8: Simulation waveform of LCD

6. Tools

6.1 Xilinx ISE means Xilinx Integrated Software Environment (ISE). This Xilinx design software suite allows you to take your design from design entry through Xilinx device programming.

6.2 The ISE Project Navigator manages and processes your design through several steps in the ISE design flow. These steps are Design Entry, Synthesis.

I. Implementation,

II. Simulation/Verification

III. Device Configuration

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