Implementation of Adaptive Viterbi Decoder for Wireless Communication

Rupali Dhobale[1], Kalyani Ghate[2], Nikhil Pimpalgaonkar[3], R. B. Khule[4]

[1]B.E. Electronics, K.D.K. College of Engineering,
Nagpur, Maharashtra, India
rupalidhobale8@gmail.com

[2]B.E. Electronics, K.D.K. College of Engineering,
Nagpur, Maharashtra, India
kalyanighate@rediffmail.com

[3]B.E. Electronics, K.D.K. College of Engineering,
Nagpur, Maharashtra, India
npnikhilp08@gmail.com

[4]Assistant Professor, K.D.K. College of Engineering,
Nagpur, Maharashtra, India
rajendra_khule@rediffmail.com

Abstract: ***Viterbi algorithm is employed in wireless communication to decode the Convolution codes; those codes are used in every robust digital communication systems. Such decoders are complex & dissipate large amount of power. Thus the paper presents the design of an Adaptive Viterbi Decoder (AVD) that uses survivor path with parameters for wireless communication in an attempt to reduce the power and cost and at the same time increase in speed. Most of the researches work to reduce power consumption, or work with high frequency for using the decoder in the modern applications such as 3 GPP, DVB, and wireless communications. Field Programmable Gate Array technology (FPGA) is considered a highly configurable option for implementing many sophisticated signal processing tasks. The proposed decoder design is simulated on ModelsimSE6.3f and implemented using VHDL code.***

Keywords: Viterbi Algorithm, Adaptive Viterbi Decoder, Field Programmable Gate Array, VHDL, ASIC.

1. Introduction

Most digital communication systems nowadays Convolutionly encoded the transmitted data to compensate for Additive White Gaussian Noise (AWGN), fading of the channel, quantization distortions and other data degradation effects. For its efficiency the Viterbi algorithm has proven to be a very practical algorithm for forward error correction of Convolutionly encoded messages. The requirements for the Viterbi decoder or Viterbi detector depend on the applications used. Most of the researches work to reduce cost, the power consumption, or work with high frequency for using the decoder in the modern applications such as 3GPP, DVB, and Wireless communications. Some of them comparing between using FPGA, Application Specific Integrated Circuit (ASIC) , and Digital Signal Processing (DSP) to find which one is suitable for the applications, other studies the differences method for back trace unit to find the correct path, and the other trying to work with high frequency by using parallel operations of decoder units . The complexity of these decoders increased with the increasing of the constraint length. Thus, we attempts to;

1. Design an adaptive Viterbi decoder that uses survivor path storage with parameters for wireless communication.
2. Design and implement the decoder using ModelsimSE6.3f modeling tool. Evaluate the decoder for timing accuracy and resource utilization.

VHDL stands for VHSIC Hardware description language. VHSIC is itself an abbreviation for very high speed integrated Circuit. This language was first introduced in 1981 for the Department of Defense (DoD) under the VHSIC program. In 1983 IBM, Texas instruments and intermetrics started to develop this language. In 1987 IEEE standardized the language. VHDL is a hardware description language. It describes the behavior of an electronic circuit or a system from which the physical circuit or system can then be implemented. VHDL is intended for circuit synthesis as well as circuit simulation. VHDL is programming language that allows one to model and develop complex digital system in dynamic environment by dataflow, behavioral and structural style of modeling. The behavior of field programmable gate arrays can be illustrated by this language.

2. Convolution Codes

The convolution encoder is basically a finite state machine. The k bit input is fed to the constraint length K shift register and the n outputs are calculated from the generator polynomials by the modulo-2 addition. The generator polynomial specifies the connections of the encoder to the modulo-2 adder. Convolution codes are applied in applications that require good performance with low implementation cost. They operate on data stream, not static block. Convolution codes have memory that uses previous bits to encode or decode following bits. It is denoted by *(n,k,L)*, where L is code memory depth. The Fig 2.1 below illustrates a simple Convolution coder.

$$V_1 = m_2 \oplus m_1 \oplus m_0 \ldots\ldots(1)$$
$$V_2 = m_2 \oplus m_0 \ldots\ldots\ldots\ldots(2)$$
$$V_3 = m_2 \oplus m_1 \oplus m_0 \ldots\ldots(3)$$

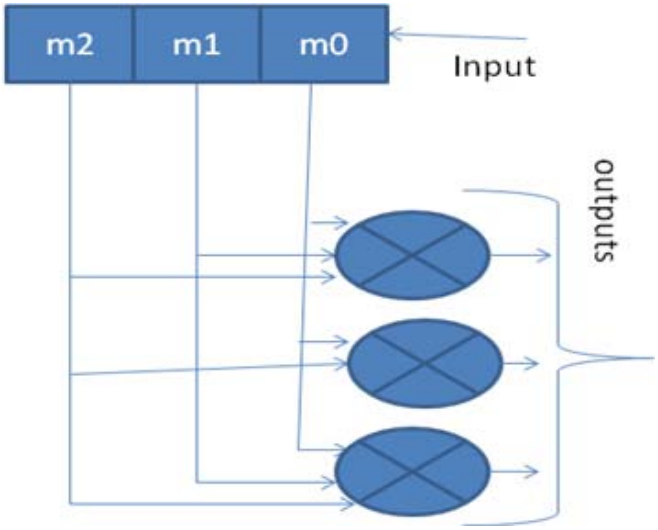

Figure 2.1: Convolution Encoder

3. Viterbi Algorithm

Viterbi algorithm was devised by Andrew J. Viterbi (1967). The optimality and the relatively modest complexity for small constraint lengths have served to make the Viterbi algorithm the most popular in decoding of Convolution codes with constraint length less than 10. Viterbi algorithm is called as optimum algorithm because it minimizes the probability of error. The Viterbi algorithm is one of the standard sections in number of high-speed modems of the process for information infrastructure applicable in modern world. The unit of branch metric will calculate all the branch metrics and then processed to add compare for selecting the surviving branches as per the branch metrics finally the decoded data bits are generated by the trace back unit.

The algorithm can be broken down into the following three steps;

a. Weight the trellis; that is, calculate the branch metrics.
b. Recursively computes the shortest paths to time n, in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. This is known as add-compare-select (ACS) recursion.
c. Recursively finds the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the process is referred to as survivor path decode. Finally, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path.

4. Architecture of Viterbi Decoder

The input to our proposed design is an identified code symbols and frames, i.e. the design decodes successive bit stream and the proposed decoder has no need to segment the received bit stream into n-bit blocks that are corresponding to a stage in the trellis in order to compute the branch metrics at any given point in time. The architecture of the Viterbi decoder is illustrated in fig 3.1.

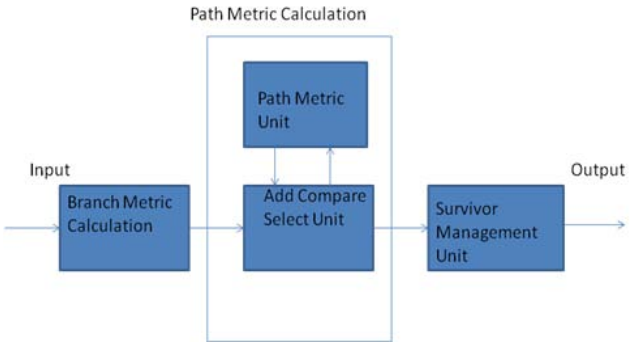

Figure 4.1: Basic building blocks of the Viterbi decoder

The basic performance of the Viterbi decoder is analyzed with the block diagram shown below. It consists of three main blocks:

1. Branch Metric Calculation
2. Path Metric Calculation
3. Survivor Management Unit

4.1 The Branch Metric Calculation (BMC)

This is typically based on a look-up table containing the various bit metrics. The computer looks up the n-bit metrics associated with each branch and sums them to obtain the branch metric. The result is passed along to the path metric Calculation. The responsibility of this unit is to compute the Hamming code between the expected code and the receiving code as a frame. At each processing, the BMU finds the Hamming code for these symbols.

4.2 Path Metric Calculation

There are Path Metric Unit (PMU) and Add Compare Select Unit (ACSU) blocks in it.

4.2.1. Path Metric Unit (PMU)

It computes the partial path metrics at each node in the trellis.

4.2.2 Add Compare Select Unit (ACSU)

This ACSU is the main unit of the survivor path decoder. The function of this unit is to find the addition of the Hamming code received from BMU's and to compare the total hamming code. This takes the branch metrics computed by the BMC and computes the partial path metrics at each node in the trellis. The surviving path at each node is identified, and the information-sequence updating and storage unit notified accordingly. Since the entire trellis is multiple images of the same simple element, a single circuit called Add-Compare-Select may be assigned to each trellis state.

4.3 Survivor Management Unit (SMU)

This is responsible for keeping track of the information bits associated with the surviving paths designated by the path metric Calculation. There are two basic design approaches: Register Exchange and Trace Back. In both techniques, a shift register is associated with every trellis node throughout the decoding operation. Since one of the major interests is the low power design, the proposed decoder has been implemented using the trace back approach which dissipates less power. The major disadvantage of the RE approach is that its routing cost is very high especially in the case of long-constraint lengths and it requires much more resources.

5. Modified Architecture of Adaptive Viterbi Decoder

The aim of the adaptive Viterbi Decoder is to reduce the average computation and path storage required by the Viterbi algorithm. Instead of computing and retaining all 2*K-1* possible paths, only those paths which satisfy certain cost conditions are retained for each received symbol at each state node. Path retention is based on the following criteria.

A threshold T indicates that a path is retained if its path cost is less than dm + T, where dm is the minimum cost among all surviving paths in the previous trellis stage.

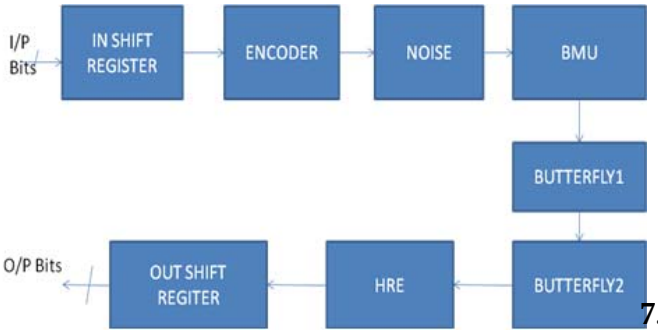

Figure 5.1: Block diagram of adaptive Viterbi decoder

6. Flowchart of Viterbi Decoding Algorithm

Fig 6.1 shows the flowchart of Adaptive viterbi Decoding Algorithm. As seen in viterbi decoding algorithm, it can choose the best path or shortest path in terms of hamming distance at the end of trellis or decoded bits. This leads to an extra computations and processing delay.

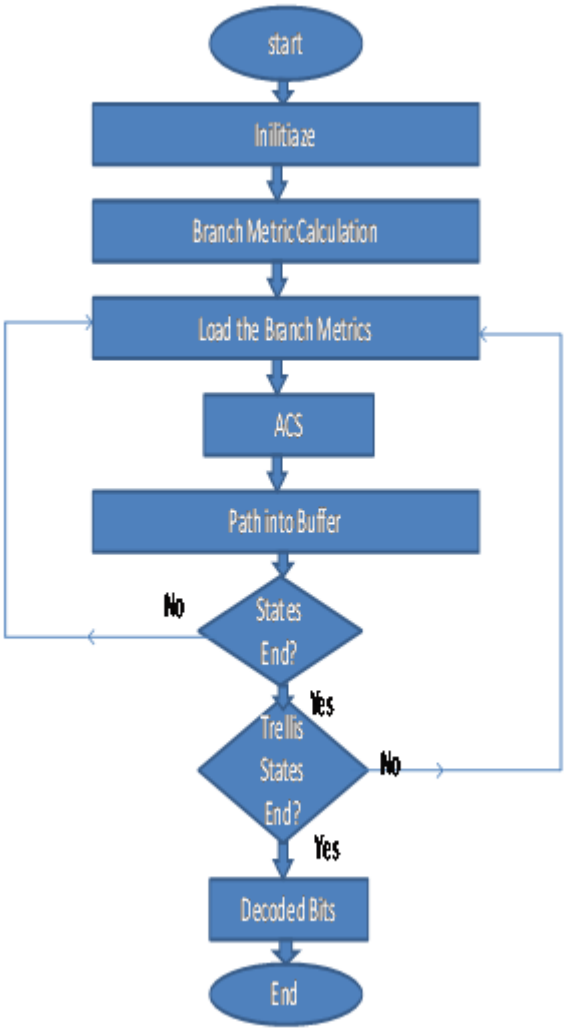

Figure 6.1: Viterbi Decoding Flowchart

7. Simulation Results

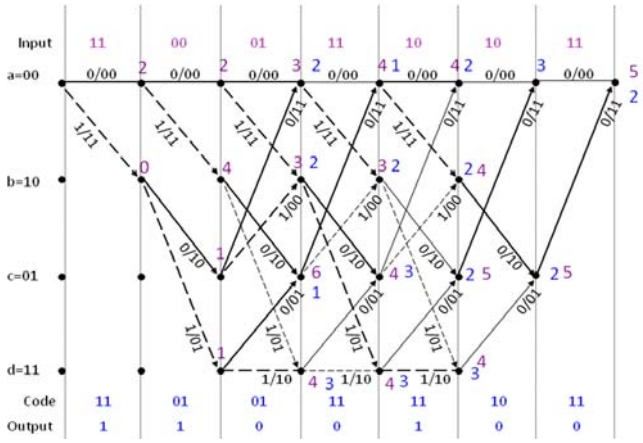

Figure 7.1: Viterbi algorithm

Fig 7.1 shows the Viterbi Algorithm diagram and Fig 7.2 shows the simulation result of Adaptive Viterbi Decoder using ModelsimSE6.3F.

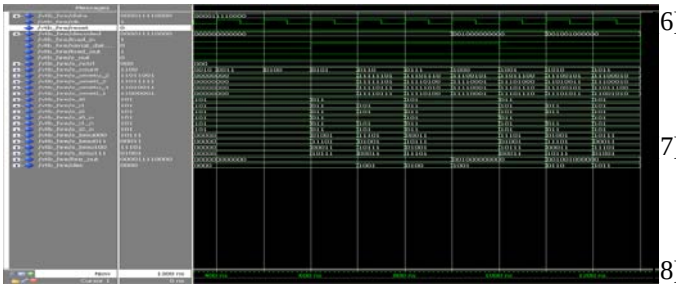

Figure 7.2: Simulation result of Adaptive Viterbi Diagram

8. Applications

- A Low Power Viterbi Decoder for Wireless Communications Applications
- Pipelined VLSI Architecture of the Viterbi Decoder for IMT-2000
- 200Mbps Viterbi decoder for UWB
- Viterbi Decoder for WCDMA System
- Low complexity efficient trackback Viterbi decoder for wireless applications.
- A Soft IP Generator for High-speed Viterbi Decoders

9. Conclusion

As mobile and wireless communication becomes increasingly ubiquitous, the need for dynamic reconfigure ability of hardware shall pose fundamental challenges for communication algorithm designers as well as hardware architectures. This paper attempts to solve this problem for the Particular case of the Viterbi decoder. Reconfigure the Viterbi decoder, and adaptive Viterbi decoder units will give simple elements in each unit and new algorithms. The processing execution time has been reduced by removing the trace back algorithms that is used to find the correct paths. The survivor path algorithm used, the address of the memory unit to select the correct path which specify the output code

References

[1] Prof. Siddeeq Y. Ameen , Mohammed H. Al-Jammas and Ahmed S. Alenezi," FPGA Implementation of Modified Architecture for Adaptive Viterbi Decoder", IEEE,2011.

[2] S. W. Shaker, S. H. Alramely and K. A. Shehata, "Design and implementation of low- power Viterbi decoder for software-defined WiMAX receiver", 17th Telecommunication Forum TELFOR, Serbia, Belgrade, 2009

[3] Janne Maunu, Mika Laiho, Tero Koivisto, Karti Virtanen, Mikko Pankaala , Ari Paasio, "Mixed-Signal Viterbi Decoder for a MB-OFDM Receiver",IEEE,2008.

[4] H. .S, Suresh and B.V, Ramesh, "FPGA implementation of Viterbi decoder", Proceedings of the 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Greece, February 16-19, 2007.

[5] J. S, Reeve, and K. Amarasinghe "A parallel Viterbi decoder for block cyclic and Convolution codes", Journal of Signal Processing, vol. 86, page 278, 2006.

6] Obeid A. M., Ortiz A. G., Ludewig R., and Glenser M, "Prototype of a high performance generic Viterbi decoder", Proceedings, 13th IEEE International Workshop on Rapid System Prototyping I 2002

7] Sriram Swaminathan, Russell Tessier, Dennis Goeckel and Wayne Burleson "A Dynamically Reconfigurable Adaptive Viterbi Decoder" FPGA'02, February 24-26, 2002, Monterey, California, USA

8] J. Bhasker "VHDL Primer" PHI publication third edition

[9] K.S. Arunlal Dr. S.A.Hariprasad "An Efficient Viterbi Decoder" IJAIT vol 2 No 1, February 2012

[10] Samirkumar Ranpara, Dong samHa "A low power Viterbi Decoder Design for Wireless Communication Applications". 1999 IEEE

[11] Byonghyo shim sungmin cho and Jung Chul Suh "An improved VLSI architecture for viterbi decoder", 1999 IEEE.

[12] Byonghyo shim and Jung Chul Suh "Pipelined VLSI architecture of the Viterbi Decoder for IMT-2000" 1999 IEEE

[13] Sung_woo_choi, Sang_Sung choi, "200 Mbps Viterbi decoder for UWB"

[14] Sunil P. Joshi and Roy Paily"Low power Viterbi Decoder by Modified ACSU architecture and clock Gating method", 2011 IEEE

[15] Jinjin He, Huaping Liu, Zhongfeng Wang' Ximming Huang,and kai Zhang."High-speed low power Viterbi Decoder Design for TCM Decoders", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS

[16] Usana Tuntoolavest and Pongpisut Noradee "Suitable Mobile Channel Conditions for a Concate noted Codind Systems with List-of-2 Viterbi Inner Decoder" 2010 IEEE .ISCIT 2010

[17] Lin Gui(Member),Yin Xu, Bo Liu, Liang gong and Ying Li "An Iterative Decoding Technique and Architecture for RS Transactions on Consumer Electronics, vol. 56 No.3,August 2010.

[18] Zhou Meng and Gao Minglun "A High-Speed ACS Design Based on 4:2 Compression Array"@2010 IEEE 2nd International Conference on Signal Processing Systems (ICSPS).

[19] Chih-Jhen chen, Chu Yu,Mao-Hsu Yeu, Pao-Ann Hsinng ,and Sao-Jie Chen "Design of a low power Viterbi Decoder for Wireless Communication Applications", @2010 IEEE

Author Profile

Rupali Dhobale received her Diploma in Electronics& Communication from Priyadarshini Polytechnic Nagpur under M.S.B.T.E and currently doing B.E. degree in Electronics Engineering from K.D.K. College of Engineering, Nagpur under the R.T.M. Nagpur University. She is currently doing project work on "Implementation of Adaptive Viterbi Decoder".

Kalyani Ghate is currently doing B.E. degree in Electronics Engineering from K.D.K. College of Engineering, Nagpur under the R.T.M. Nagpur University. She is currently doing project work on "Implementation of Adaptive Viterbi Decoder".

Nikhil Pimpalgaonkar is currently doing B.E. degree in Electronics Engineering from K.D.K. College of Engineering, Nagpur under the R.T.M. Nagpur University. He is currently doing project work on "Implementation of Adaptive Viterbi Decoder".

R. B. Khule received his B.E. degree in Electronics Engineering from B.D. College of Engineering, Sevagram, Wardha, under the R.T.M. Nagpur University also M-tech degree in VLSI from Priyadarshini college of Engineering, under the R.T.M. Nagpur University. He is currently working as an Asst. Professor in K.D.K College of Engineering. He has published more than 4 papers in recognized journals and conferences.