Implementation of Space Time Block Codes for Wimax Applications

M Ravi[1], A Madhusudhan[2]

[1]M.Tech Student, CVSR College of Engineering
Department of Electronics and Communication Engineering
Hyderabad, Andhra Pradesh, India
ravi.mydreams@gmail.com

[2]Assistant Professor, CVSR College of Engineering
Department of Electronics and Communication Engineering
Hyderabad, Andhra Pradesh, India
madhu.akku@gmail.com

Abstract: ***This paper describes the concept, architecture, development and demonstration of a real time, maximum likelihood Alamouti decoder for a wireless 4-transmit 4-receiver multiple input and multiple output (MIMO) Smart Antenna Software Radio Test System (SASRATS) platform. It is implemented on a Xilinx Vertex 2 Pro Field Programmable Gate Array (FPGA). Hardware, firmware, use of the Xilinx Core Generator Intellectual Property modules and experimental verification of the decoder are discussed.***

Keywords: real-time implementation, Alamouti, FPGA, maximum likelihood decoder, MIMO

1. Introduction

The proposed system implementation is developed on an existing MIMO Smart Antenna Software Radio Test System (SASRATS) platform [1], [2] designed to test and verify various space time architectures and algorithms. The4 receivers complement a 4-transmitter space time (ST) encoding platform [3] designed and developed for real-time testing of ST coding schemes developed by Alamouti [4] and others mentioned in [5]. The primary objective is to increase system capacity and performance through the use of multiple antennas, employing spatial multiplexing and ST coding and decoding. Spatial multiplexing and diversity techniques are currently adopted in the IEEE 802.11n draft specification to fully exploit the benefit of MIMO channels. The focus of this paper is on the digital baseband portion of the system, particularly the real-time implementation of the Alamouti decoder on a Xilinx Vertex 2 Pro FPGA. Other MIMO test beds [6], [7] typically perform post processing operations such as channel estimation and Alamouti decoding in Mat lab after capturing large batches of data. Real-time implementation of a 2 × 1 Alamouti decoder was briefly described by [8]. Our work describes in detail, the real-time implementation of a maximum likelihood 2 × 2 Alamouti decoding implementation extending to a 2 × 4 system on the SASRATS platform.

2. Proposed scheme

Realization of multi input and multi output (MIMO) systems is highly essential for Wimax networks. Space–time block coding is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. In wireless communications the transmitted signal must traverse a potentially difficult environment with scattering, reflection, refraction and so on and may then be further corrupted by thermal noise. In the receiver STBC redundancy results in a higher chance of being able to use one or more of the

received copies to correctly decode the received signal. The space–time coding combines all the copies of the received signal in an optimal way to extract as much information from each of them as possible.

In this project a computationally efficient algorithm for space time block decoding will be implemented for FPGA based applications. The VHDL will be used for realization of the decoding algorithm and other communication blocks.

The algorithm will be realized for Phase Shift Keying modulation (BPSK) scheme. The STBC encoder will also be realized in MATLAB/OCTAVE which generates the required appropriate codes for decoder. The work involves FPGA implementation of STBC decoder, and demodulator. Various sub blocks such as SIN/COS generators, multipliers, adders, encoding look up tables, complex arithmetic units etc will be implemented. These blocks will be realized in generic style to ensure scalability and reconfigurability of the STBC decoder design.

Modelsim Xilinx edition (MXE) tool will be used for simulation and functional verification. Xilinx Synthesis technology (XST) will be used for FPGA synthesis. Timing analysis will be carried out to predict the maximum achievable clock speeds for choosen Xilinx Spartan 3E FPGA device.

3. Overview of Alamouti Scheme

The Alamouti scheme is the only orthogonal space-time block code using complex signals for two transmit antennas which provides full diversity of 2 and full rate of 1. For more 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications than two transmit antennas, the goal is to design transmission codes that achieve full diversity at the highest possible rate with low decoding

complexity. In our 2 x 2 MIMO implementation, we use two distinct training codes over 2 time multiplexed preamble slots at the transmitter. When one transmitter is sending training data in one time slot, the other is off. These 26-bit preambles are GSM training sequence codes (TSC) 0 and 1 [11]. The two transmitters then transmit 128 space-time encoded data symbols simultaneously before the cycle repeats. At the transmitter, the SASRATS transmitters are programmed to run a 2 transmit Alamouti encoding scheme, where two symbols, $s0$ and $s1$, are transmitted simultaneously from two transmitters at time instant t. At time instant $t + T$, the symbols $-s_1^*$ and s_0^* are transmitted simultaneously from the transmitters where * represents the complex conjugate. The transmission matrix is represented by

$$S = \begin{bmatrix} s_0 & s_1 \\ -s_1^* & s_0^* \end{bmatrix}$$

The transmitted symbols travel through 2 independent channels $h0$ and $h1$ to a receiver where noises $n0$ and $n1$ are added to the received signals. $h0$ and $h1$ are complex multiplicative distortions assumed constant across two consecutive symbols. Implementation of a MIMO 2 transmitter and 2 receiver Alamouti system, requires the estimation of 4 channel $(\hat{h}_0, \hat{h}_1, \hat{h}_2 \text{ and } \hat{h}_3)$, 2 at each receiver as shown in Figure 2.1. In this situation, the output of combiner yields 2 outputs.

$$\tilde{s}_0 = \hat{h}_0^* r_0 + \hat{h}_1 r_1^* + \hat{h}_2^* r_2 + \hat{h}_3 r_3^*$$

Where $\hat{h}_2$ and $\hat{h}_3$ are channel estimates from the second receiver. In the case of a 2 x 2 Alamouti implementation using PSK signals, the ML decoder remains unchanged except for the combiner. The combined output $\tilde{s}_0$ is actually the sum of $\tilde{s}_0$ from receiver 0 and $\tilde{s}_0$ from receiver 1. Likewise, $\tilde{s}_1$ is actually the sum of $\tilde{s}_1$ from receiver 0 and $\tilde{s}_1$ from receiver 1. Thus a 2 x M Alamouti implementation can be easily implemented by summing together the appropriate combiner outputs from M receivers before feeding one ML detector. In an extended version of Alamouti for 4 transmitters, full rate is achieved but the system is half rank (quasi-orthogonal) with some loss in diversity as transmitted symbols cannot be fully decoupled. Tarokh's STBC scheme for 4 transmitters on the other hand, achieves complete orthogonality at half the full rate. Tarokhs scheme suffers no loss in diversity and receiver decoding is simpler as the transmitted symbols can be fully decoupled.

The decoding of the Alamouti encoded signals is a linear process and our SASRATS receiver system design implements the combiner and maximum likelihood detection on the Xilinx Vertex 2 Pro FPGA board using the Xilinx Integrated System Environment (ISE) Foundation design tool.

$$S = \begin{bmatrix} s_0 & s_1 \\ -s_1^* & s_0^* \end{bmatrix} \qquad (1)$$

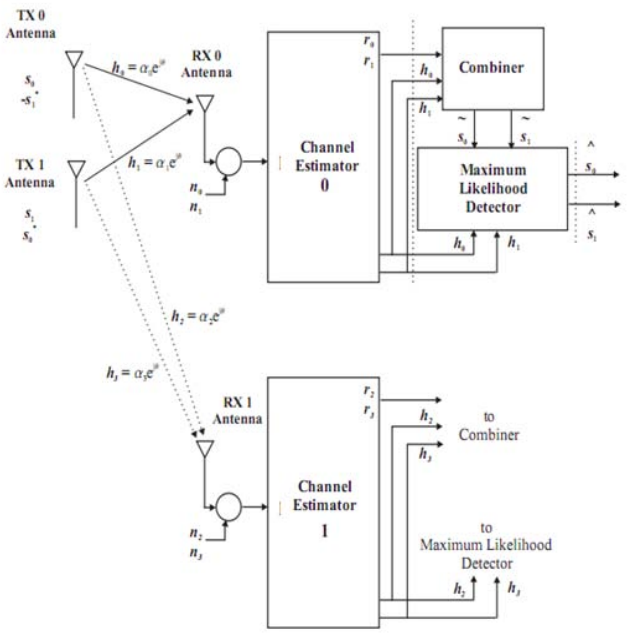

Figure 1: Block diagram of alamouti decoding implementation

4. Implementation of the Alamouti Combiner and ML Decoder

We begin by first describing the overall architecture of the Alamouti 2×1 decoding scheme for QPSK modulated received symbols as shown in Figure 1.

The architecture consists of several blocks; the pre combiner, combiner, ML detector and output data formatter. The inputs into the pre-combiner block consist of 16-bit I and Q data and channel estimates $\hat{}h0$ and $\hat{}h1$ which remain static for the duration of 128 data symbols.

On receipt of the Data Valid (DV) pulse from the channel estimator, the pre-combiner circuitry latches to capture $r0$ and $r1$ over two symbol periods and calculates the complex conjugates of $\hat{h}_0, \hat{h}_1$ and $r1$ needed in the combiner.

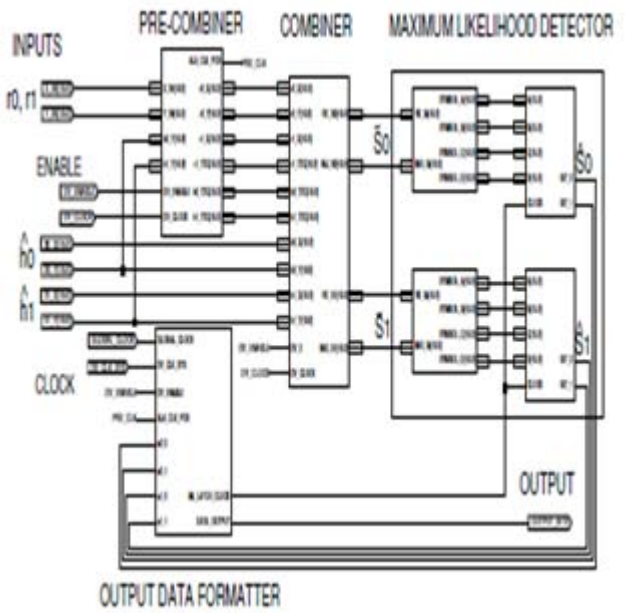

Figure 2: Block diagram of alamouti combiner and ML detector implementation

The combiner block as shown in Figure.2 calculates $\tilde{s}_0$ and $\tilde{s}_1$. The product terms $\hat{h}_0^* r_0, \hat{h}_1 r_1^*, \hat{h}_1^* r_0$ and $\hat{h}_0 r_1^*$ are first calculated in 4 separate Xilinx Complex Multiplier v2.0 IP blocks. The product terms $\hat{h}_0 r_1^*$ and $\hat{h}_1 r_1^*$ are then summed to compute $\tilde{s}_0$. The signal $\tilde{s}_1$ is then formed by taking difference between $\hat{h}_1^* r_0$ and $\hat{h}_0 r_1^*$ by two properly configured Xilinx Adder/Subtracter v7.0 IP cores respectively.

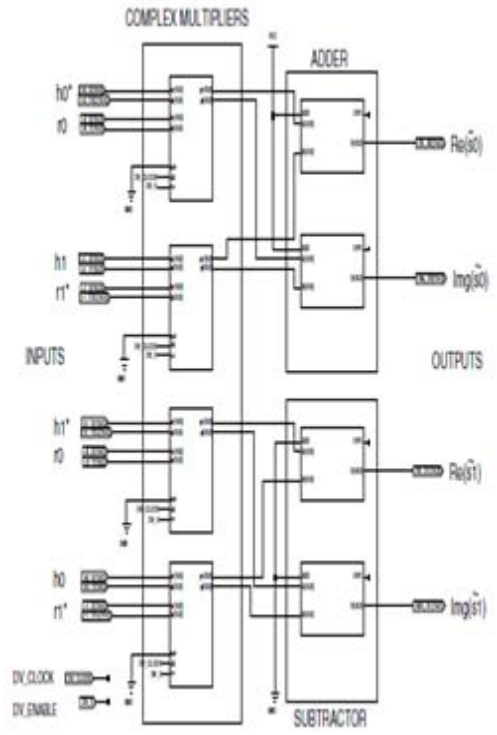

Figure 3: Block diagram of combiner

The outputs $\tilde{s}_0$ and $\tilde{s}_1$ are then fed into the maximum likelihood (ML) detector processing block. The ML block consist of 2 parallel and independent sets of Euclidean distance calculators and minimum distance comparators as shown in Figure 2.1.3 where the decision statistics, $\tilde{s}_0$ and $\tilde{s}_1$ are processed independently.

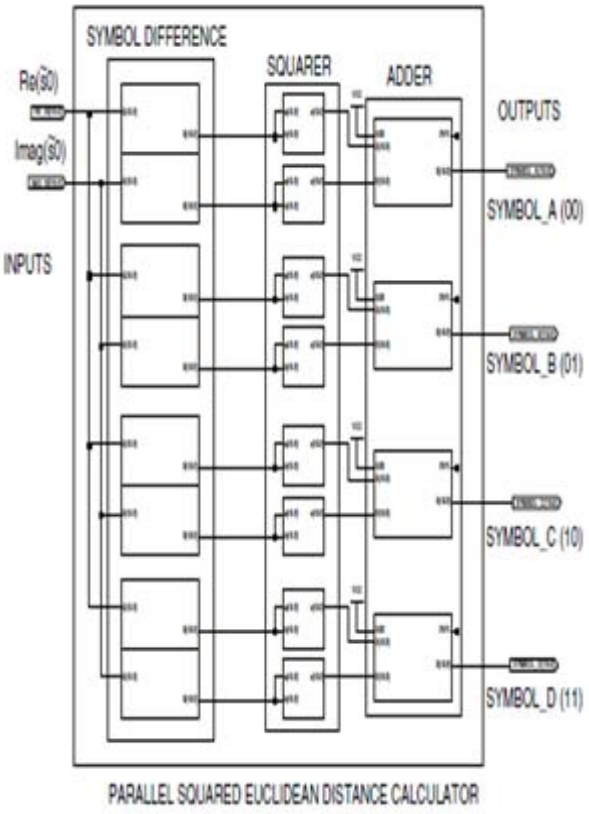

Figure 4: Block diagram of scaled Euclidean distance block in the ML detector

The Euclidean distance calculator block shown in Figure.3 first calculates in parallel, the difference between the symbol decision statistic and 4 pre stored QPSK symbols ($\pm 0.707 \pm j0.707$). The real and imaginary parts of each symbol are then squared and added together. The 4 squared Euclidean distance outputs (A, B, C and D) are fed into the minimum Euclidean distance comparator block shown in Figure 4.

At the SASRATS receivers, the I and Q outputs are fed into a Xilinx University Program Vertex 2 Pro Development System board based on the Vertex 2 Pro XC2VP30 with 30,816 logic cells. This low cost development board from Diligent Inc. has four 20-bit wide ports which are ideal for our 4 receiver system. The minimum Euclidean distance comparator is implemented using 6 two-input magnitude comparators. There are two outputs ($x > y$, $< y$) from each comparator. The outputs from the various comparators are AND'ed together and latched based on the following minimum magnitude selection criterion which chooses A iff $(A < B)$ & $(A < C)$ & $(A < D)$, B iff $(A > B)$ & $(B < C)$ & $(B < D)$, C iff $(A > C)$ & $(B > C)$ & $(C < D)$, D iff $(A > D)$ & $(B > D)$ & $(C > D4)$. Only one of the four outputs goes high when the criterion is met. Then the latched outputs are fed into two OR gates to decode the estimated QPSK symbol into bits. Thus each magnitude comparator for $\hat{}s0$ or $\hat{}s1$ has one 2-bit output which represents 00, 01, 10 or 11.

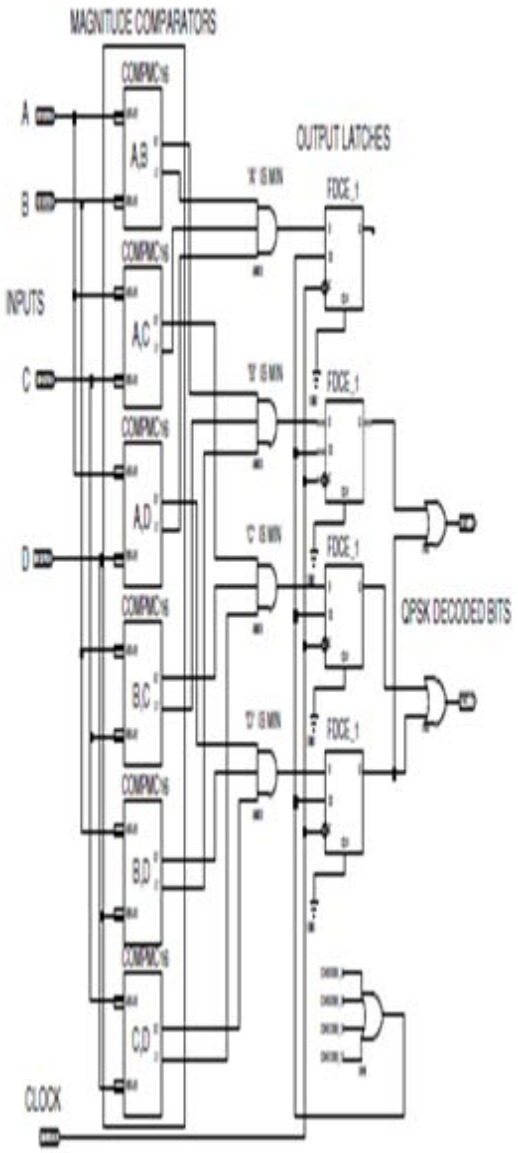

Figure 5: Block diagram of the minimum distance comparator block in the ML detector

The inputs are rst, master_clk, data_bit and outputs are ant0_out and ant1_out. The data bit is given to symbol mapper that will convert data bit to i_sym and q_sym these output's will be shifted to pipo block so that with the same clock the data is processed to next state, used as a select pin to S block it works as a mux according to select bit the operation will be selected selected_i_sym_ant0.In other results selected_i_sym_ant1, selected_q_sym_ant0 and selected_q_sym_ant1 will be generated.

Using the phase_inc_word the phase_acc section generates address to the LUT_cos and lut_sin, LUT_cos and lut_sin generates the amplitude according to address amplitude signals will be supplied to the multiplier blocks for further process. Frame clk is used to generate the enable signals to the multiplier section this is shown in below figure

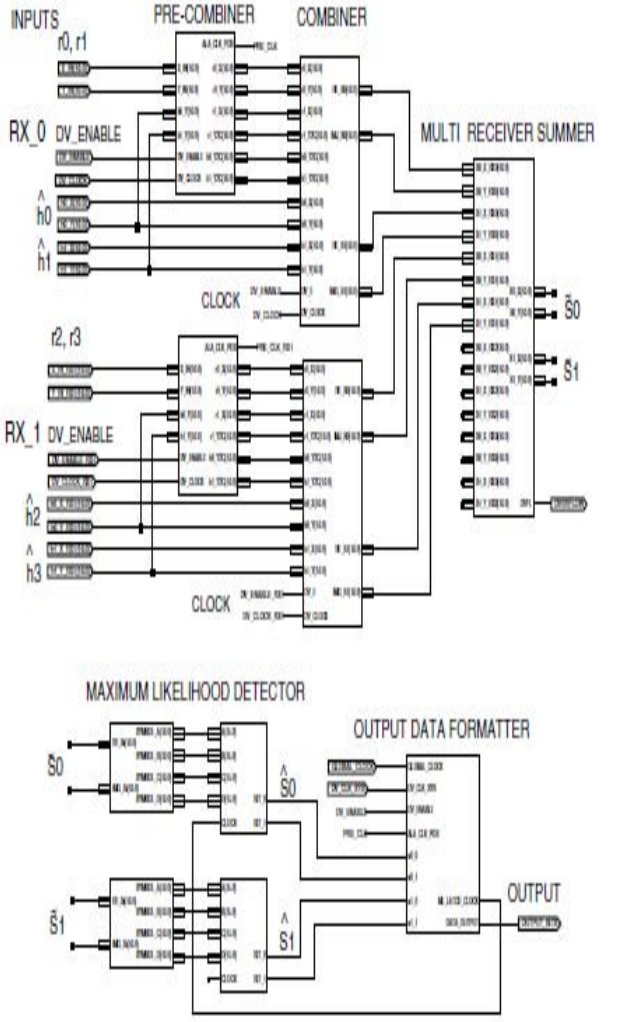

Figure 6: Block diagram of 2 x 2 alamouti implementation

When the enable signal is given by frame-sync_ant0 then multiplier will perform the multiply operation on inputs and result of both multiply section.

5. Conclusion

We have described the implementation of a real time maximum likelihood Alamouti decoder for use on our MIMO platform implemented on an FPGA using the Xilinx ISE tool and Core Generator IP modules. We have also experimentally verified the operation of the decoder in a closed Altamonte 2 x 1 diversity scheme using an RF channel simulator and also in an open 2 x 2 and 2 x 4 antenna based system under correlated channel conditions.

References

[1] P. Green and D. Taylor, "Smart antenna software radio test system," Proceedings of the First IEEE International Work-shop on Electronic Design, Test and Applications.,vol.1,pp. 68–72, Jan. 2002.

[2] "Experimental verification of space-time algorithms using the smart antenna software radio test system (sasrats) platform," Personal, Indoor and Mobile Radio Communications, 2004. PIMRC 2004. 15th IEEE International Symposium on, vol. 4, pp. 2539–2544, 2004.

[3] "Implementation of a high speed four transmitter space-time encoder using field programmable gate array and parallel digital signal processors," Proceedings of the Third IEEE International Workshop on Electronic Design, Test and Applications., pp. 466–471, Jan. 2006.
[4] S. Alamouti, "Space block coding: A simple transmitter diversity technique for wireless communications," IEEE J. Select. Areas. Communication, vol. 16, pp. 1451–1458, Oct. 1998.
[5] D. Gesbert et al., "From theory to practice: An overview of mimo space-time coded wireless systems," IEEE Journal on Selected Areas in Communications, vol. 21, pp. 281–302, Apr. 2003.
[6] R. M. Rao et al., "Multi-antenna testbeds for research and ed-ucation in wireless communications," IEEE Communications Magazine, vol. 42, no. 12, pp. 72–81, 2004.
[7] S. Caban et al., "Vienna MIMO testbed," EURASIP Journal on Applied Signal Processing, vol. 54868, pp. 1–13, 2006.
[8] P. F. P. Murphy and C. Dick, "An fpga implementation of alamoutis transmit diversity technique," University of Texas WNCG Wireless Networking Symposium, Oct. 2003
[9] P. Green and D. Taylor, "Implementation of four real-time software defined receivers and a space-time decoder using xilinx virtex 2 pro field programmable gate array," Proceedings of the Third IEEE International Workshop on ElectronicDesign, Test and Applications., pp. 89–92, Jan. 2006
[10] "Implementation of a real-time multiple input multiple output channel estimator on the smart antenna software radio test system platform using the xilinx virtex 2 pro field programmable gate array," Proceedings of the 2006 IEEE In- ternational Conference on Field Programmable Technology., pp. 257–260, Dec. 2006.
[11] ETSI/GSM, "Multiplexing and multiple access on the radio path," GSM Recommendations Document 05.02 Version 3.8, Dec. 1995.
[12] M. Rupp and C. Mecklenbrauker, "On extended alamoutischemes for space-time coding," Wireless Personal Multime-dia Communications, 2002. The

Author Profile

M. Ravi received the B. Tech degree in Electronics and Communication Engineering from Nagarjuna Inst of Science and Technology, JNTU University, Hyderabad in 2009, and currently pursuing the M. Tech degree in VLSI System Design from CVSR College of Engineering, JNTU University, Hyderabad respectively. His research implementation of space time blocks codes for WiMax applications.

A. Madhu Sudhan received the B. Tech degree in Electronics and Communication Engineering from NCE, 2005, and the M.Tech degree in VLSI System Design from Anna University, 2009 respectively. He is currently an Assistant Professor with the CVSR College of Engineering with 4 years of experience. He was with the Department of Electronics and Communication Engineering, JNTU University. His research implementation of space time blocks codes for WiMax applications.