

# Low Noise Amplifier (LNA) Design for 57 GHz to 63 GHz EHF Narrow Band Systems

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**Abstract:** *Low Noise Amplifier (LNA) of single stage on inductive source degeneration structure for Extremely High Frequency (EHF) is proposed in this paper. The presented LNA for 57GHz-63GHz narrow band system is implemented on 90nm CMOS technology. The proposed technique not only minimizes noise Figure but also achieves high gain. The simulated prototype has measured a gain magnitude of 18V and achieves input third order intercept point (IIP3) of -5.06dBm, Noise Figure of less than 1dB (525.20 mdB) and good input matching with small signal amplification (500nV to 500mV).*

**Keyword:** LNA, Low Noise Amplifier, 60 GHz, source degenerated.

## 1. Introduction

Wireless Communications with high speed and high data rates have inspired intense industrial and academic research in Extremely High Frequency (EHF). EHF systems are capable of offering very high data rates and high security. 57-59.3GHz is used for space monitoring and climate sensing. 60 GHz is used for unlicensed short range with throughput of 2-3Gbits/sec on which the LNA yields +18dB gain with least noise Figure and used for low power transmission. Though 60GHz suffer from a problem of oxygen absorption, upcoming Wi-Fi 802.11 will work on (V band) 60GHz only with transfer rate of 7Gbits/sec and Wireless HD technology that also runs near 60GHz.

LNA design is the most challenging task while designing a receiver as it must meet several characteristics like providing sufficient gain to overcome noise while adding as little noise as possible. LNA should provide good input/output matching. Low noise Figure of LNA improves sensitivity and LNA is expected to be fairly efficient. Different topologies have been used in LNA design among them resistive shunt feedback [4], multi-stage cascaded amplifiers (common gate-common source) topology, distributed topology [5] and the LC matching and filtering topology [11]. What topology one want to design on is generally based on demanded noise performance and power dissipation.

Here designed and simulation of a modified single stage source degeneration inductor LNA for narrow band receiver using 90nm standard RF CMOS technology process is presented. The paper is organized as follows. Section 2 depicts the design go about of the proposed amplifier. Section 3 compares between different LNAs and Section 4 presents the conclusion work.

## 2. Circuit Design of LNA

In this paper, the proposed LNA rely on the filter techniques which have an output inductor and a load capacitor in order to achieve optimum noise Figure and gain on Extremely High Frequency. The proposed design is simulated and optimized CADENCE VIRTUOSO6.1.5 Schematic Editor. All the parasitic values are taken in

account as gpd90 library is used for simulation and analog library is used for modeling all the RLC circuits.

Although single stage cascode and interstage technologies have been used, but they are limited to 2GHz and 5 GHz of frequency range. In this work this technology has been studied carefully and further simulated for EHF operations. The proposed technology can be viewed in Figure 1. It can be viewed as a common source (CS) amplifier which produces an optimum gain at the frequency of 60 GHz by using inductive degeneration. Figure 2 shows the AC analysis of the Circuit.

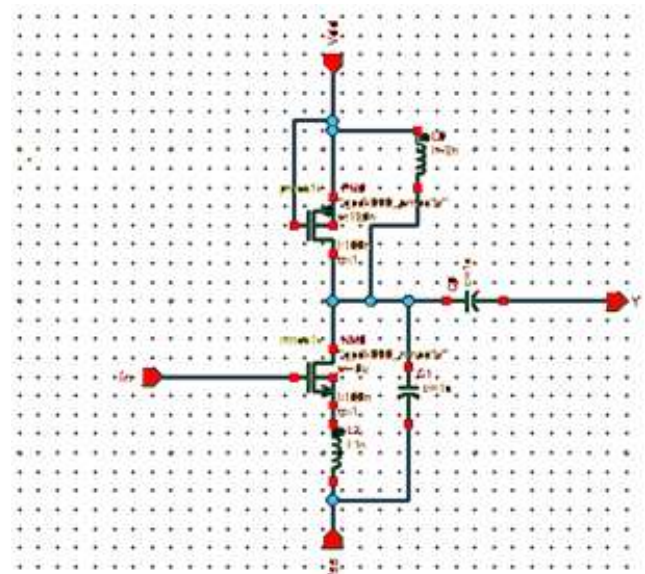


Figure 1: LNA Schematic

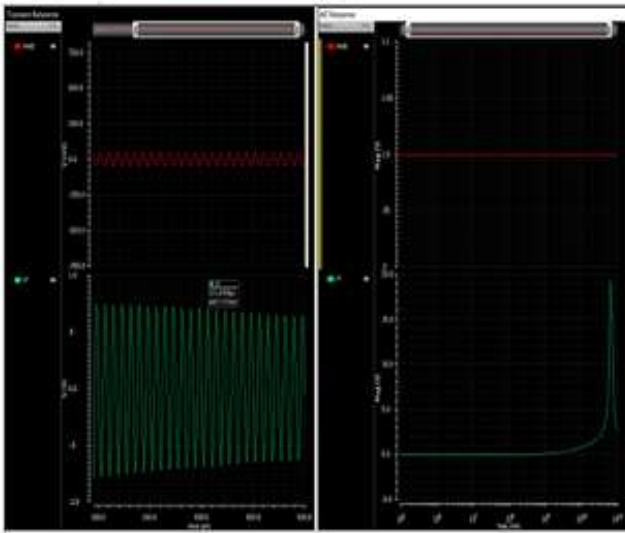


Figure 2: AC Analysis

By ignoring the Miller effect gate drain capacitance of transistor nmos1v, the input impedance is given by [2]:

$$Z_{in1} = j\omega L2 + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1} \cdot L2}{C_{gs1}} \quad (1)$$

where the transconductance and gate source capacitance of nmos1v are gm1 and Cgs1 respectively.

L2 is the source degeneration inductor.

We can give the real part of input impedance as:

$$Re\{Z_{in1}\} = \frac{g_{m1} \cdot L2}{C_{gs1}} \quad (2)$$

The input impedance can be set by to match the Rs (50Ω) by setting the value of L2 accordingly. The resonating frequency is approximated by:

$$\omega_0 = \sqrt{\frac{1}{L2 C_{gs1}}} \quad (3)$$

Output impedance of the Common Source stage is as follows [1]:

$$Z_{out1} = \frac{r}{jr\omega C_{ds1} + 1} \quad (4)$$

Where r stands as parallel connection between the parasitic channel resistance and the small signal resistance and Cds1 is the drain source capacitance of nmos1v.

L2 is added in common source amplifier to match noise and input simultaneously. The transistor of common source (nmos1v) is chosen to be 90nm in channel length and width is kept high as 6um. The channel length is kept small for optimization at higher frequencies while the large width provides high gain to the circuit. After selecting the nmos transistor we need to select the L2 inductor of optimum size carefully since it enhances linearity and stability but reduces gain at the same time [1]. Chip area must be kept small so the optimum size

selected for L2 is 1nH. The frequency response which was simulated in during AC analysis is shown in Figure 2. We can put a inductor in series to input 50Ω port for improved matching, there is nothing fancy about it so it is not shown and simulated here in this circuit. In Figure 3, we can depict the gain is 18dB at 60 GHz.

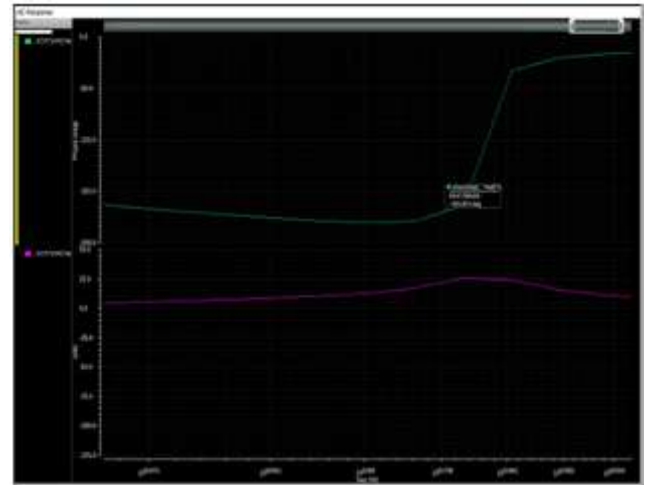


Figure 3: Phase and Gain of Circuit

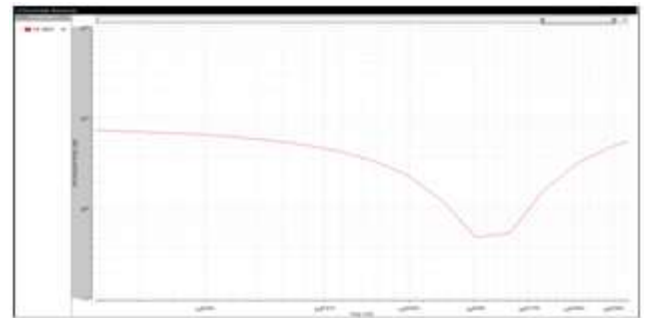


Figure 4: Noise Figure

Here we have used the inverter amplifier topology using common source amplifier and a pmos (pmos1v) amplifier. The phase difference is almost -1 at 60 GHz as we can see in Figure 3. The pmos transistor is biased carefully and the channel length is kept 90nm only.

In output stage, an Inductor L0 is place of 2nH as shunt peaking inductor resonating with pmos and load capacitor around 57-63Ghz. It also works as RF choke and blocks any RF leaking. In practice large size of pmos transistors are used to provide high gain and current to the amplifier when used at higher frequencies. But large transistors can lead to high power consumptions and large area and then one have to use higher value of L0. Large size of transistor can also lead to higher current by increasing the velocity of carriers which will lead to higher power consumption as stated above [10]. Therefore the transistor width is kept to 120nm to limit current and length at 90nm. The on chip inductors lead to large chip area which is the expense but here higher gain and very low noise is produced. The 1nH of inductor will occupy approximately a space of 1.3 nm<sup>2</sup>. Hence it will be easier to put a bondwire spiral inductance on-chip. The nmos used here is uni-fingered thin gate oxide. For ease on wafer all the inductors must be used as on chip spiral inductors.

Finally, for DC block a capacitor C0 is placed at output. No resistive elements are used in order to minimize the noise. The pmos is biased with Vdd (supply Voltage).

Further on-chip design can be carried out on CADENCE ASSURA layout editor.

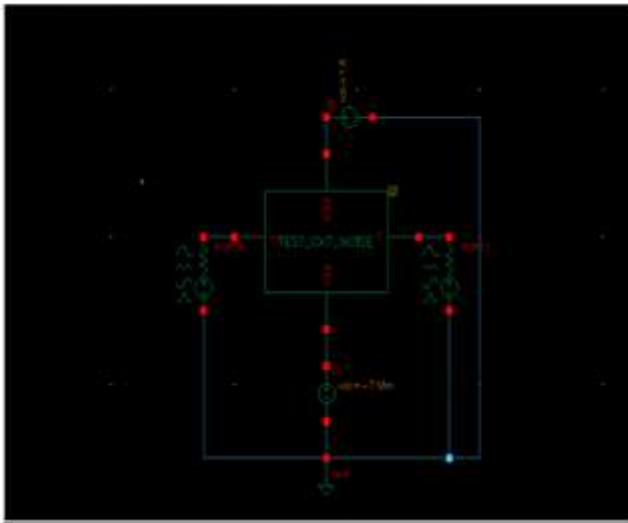


Figure 5: Port analysis and biasing

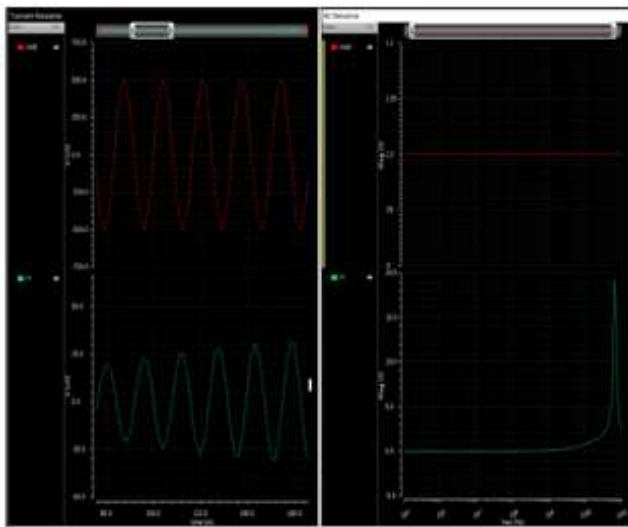


Figure 6: Small Signal AC analysis

As we can see in Figure 6, that the amplification is still very high for signal range of 500nV. Hence the circuit will work fine for low voltage input signals with minimum optimized noise. This approach provides better performance as compared to conventional cascade and multistage approaches.

### 3. Simulated Results

The simulation for the circuit that has been designed are carried out for gain, input/output return loss, 1dB gain compression, noise Figure, and third order intercept point. The simulated S-parameter is shown in Figure 7 and Figure 8.

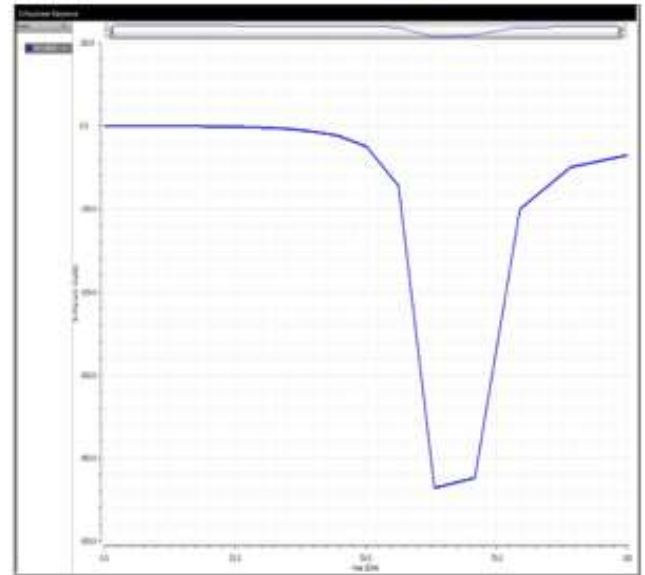


Figure 7: S11 S-Parameter Analysis

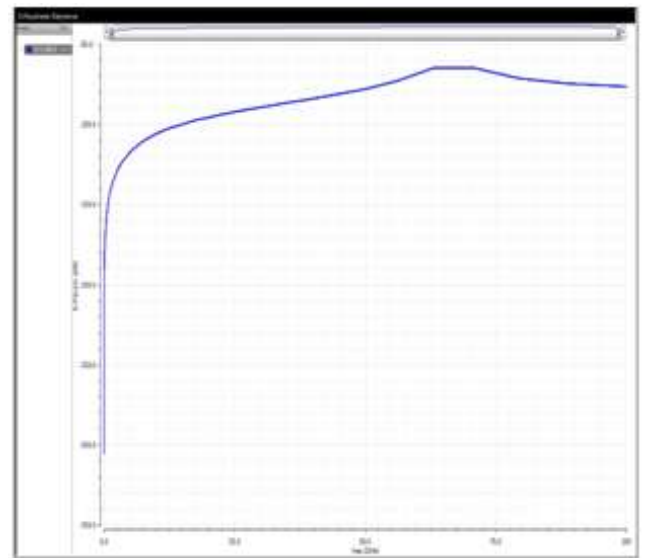


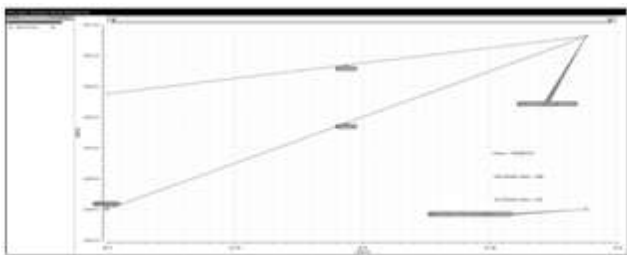
Figure 8: S12 S-Parameter Analysis

The simulated results show that the LNA has a maximum gain of +18dB at 60GHz and 6dB bandwidth covers 57GHz to 63GHz. The minimum input return loss occurs at 50GHz to 70GHz, which if necessary can be improved by using external components. A high reverse isolation is taken in account and maintained across 55GHz to 65GHz. Stability can be calculated using the S-Parameter data and the circuit is conditionally stable as it gives a value of  $K > 0.9$  which means we have to take care of the circuit while matching the input and output impedances. This stability condition can also be resolved by using an inductor at input which is ignored in order to minimize chip area. This is a major trade-off we face during analog design.

The simulated Noise Figure is shown in Figure 4. The measurement is around 525mdB at 60GHz. The periodic S-Parameter and power compression is performed in Cadence in order to calculate IIP3 (Input IP3) which is -5.06dBm, as shown in Figure 9. Table 1 compares the previous reported work by and summarizes the simulated results using 90nm Technology.

**Table 1:** Comparison between different LNAs: Reported and published works

Ref.	Tech. (nm)	BW (GHz)	NF (dB)	IIP3 (dBm)	SUP-PLY (V)	Remarks
[9]	180	0.4 to 10	4.4-6.5	-6	1.8	Multi Stage
[11] (Simulated)	180	2.8 to 5	0.6	+18	1.8	LC filters (2-Stage)
[5]	180	1 to 8	2.9-4	-3.4	1.8	Distributed (3-Stage)
[4]	180	2 to 4.6	2.3-5.2	-7	1.8	Resistive Feedback
This work (Simulated)	90	57 to 63	0.525	-5.06	1.8	Common Source Amp. (1-Stage)



**Figure 9:** Simulated IIP3

#### 4. Conclusion

The size of the circuit will occupy very less area (in mm<sup>2</sup>) and the size can be further reduced by using off-chip inductors, these off-chip inductors will also improve the gain and performance of the circuit. The circuit becomes very cost effective by using bondwire spiral inductors. The proposed CMOS LNA in this work is systematically designed and simulated on 90nm technology for narrow band of EHF (Extremely High Frequency) systems. Using conventional common source single stage amplification with source degeneration and output/load LC components we have achieved a gain of +18dB and a significantly low noise Figure (NF) of 525mdB at 60GHz (3dB bandwidth of 58.5GHz to 61.5GHz), and the purpose of design and simulation at 60 GHz was due to the fact that 60GHz is unlicensed short range with throughput.

#### 5. Acknowledgement

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#### Author Profile



**Jitendra P. Singh** is completing his M.Tech degree in VLSI from Suresh GyanVihar University, Jaipur. He worked as a trainee at Electronics Corporation of India Limited in 2013 where he worked on analog design in VLSI domain. He also worked in UTL technologies, Bengaluru on 90nm technology.