Design and Analysis of Energy Efficient Semi-Serial Link for On-Chip Communication

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Abstract*: Now a days in network-on-chip (Noc) different type of communication links are used like parallel, serial and semi-serial links. In this project low energy semi-serial on-chip communication link is designed. In this project protocol used for this proposed semi-serial link is defined. And key elements of this semi-serial link communication like serializer, deserializer, driver, receiver, and data validity decoder are designed. The energy efficiency of the proposed semi-serial link, (which consists of bit-serial links in parallel), mainly comes from the sharing of the novel's serializer's control circuit among the bit semi-serial links. In addition the integration of pulse signaling with wave-pipelining, the use of new low-complexity data decoding logic causes for the power reduction. The links are designed and simulated using cmos 180nm, 120 and 65 nm technologies in microwind 3.1 cadtool. When technology scale down from 180nm to 65nm, power decreased from 22.216mw to 10.464mw, delay decreased from 0.247ns to 0.115ns and power-delay product varies from 5.487pw-sec to 1.203pw-sec.*

Keywords: Differential current-mode signaling, network-on-chip (noc), pulse signaling, wave-pipelining.

1. Introduction

Technology scaling in to the nanometer regime creates an opportunity to integrate hundreds of cores on a single chip. In this many core era, network-on-chip (NoC) is emerging as a scalable and modular solution to provide communication between cores [1] [2]. NoC needs to be designed efficiently to maximize system performance and minimize power consumption and area. Large latencies of networks cause performance degradation in high performance systems. The power consumption of NoC implemented with current techniques is too high, by a factor of 10, to meet the expected needs of future applications [3]. However, the long-range links have to be designed in a performance and energy efficient manner. Thus, the main goal of this work is to design a high-throughput, low-power and smaller area global on-chip interconnect that can be used as long-range link in NoC. This in turn increases the overall network throughput and decreases its power consumption besides minimizing traffic congestion. NoCs with a globally asynchronous locally synchronous (GALS) clocking style are used in most of the proposed network designs and is expected to be an attractive approach to overcome many of the timing problems [4]. GALS simplifies the clock tree design and results in easily scalable clocking systems. It also allows improved energy savings since each functional unit can easily have its own independent clock and voltage [5]. Furthermore, it enables easy implementation of a distributed power management system for the entire chip [6]. Due to these advantages, the proposed long-range link design is based on self-timed design principles. Specifically, it uses two-phase handshaking and delay-insensitive data encoding and transfer techniques. Delay-insensitive data encoding and transfer is a viable solution to communicate reliably in the presence of signal propagation delay variations, which occur due to crosstalk, process, voltage, and temperature (PVT) variations. The proposed serial link communication protocol along with the design of its circuits is presented in section 2. Transistor-level simulation results and analysis of proposed link are presented in section 3.Finally the conclusion drawn from this work is discussed in section 4.

2. Low-Power Serial on-Chip Communication Link

A high-throughput and low-power serial on-chip communication link employing integration of pulse dual-rail data encoding, wave-pipelining, pulse signaling and differential current-mode signaling is presented. Two-phase pulse dual-rail encoding is performed at low cost using two *AND* gates, one for data bit '1' and the other for '0'. This encoding enables usage of pulse signaling along with differential signaling directly. Furthermore, both the latency and the power consumption are reduced because data decoding logic is not needed at the receiver. The ability to detect each bit through pulse signaling in the wave-pipelined communication makes the link delay-insensitive and also enables acknowledging the transmission per word instead of per bit, improving throughput and saving energy. The semi-serial link consists of serializer and deserializer, dual-rail encoder, driver, receiver, and data validity decoder, as shown in Fig.2.1. In the subsequent subsections, the communication protocol, design details of the link circuits and the signaling technique are discussed.

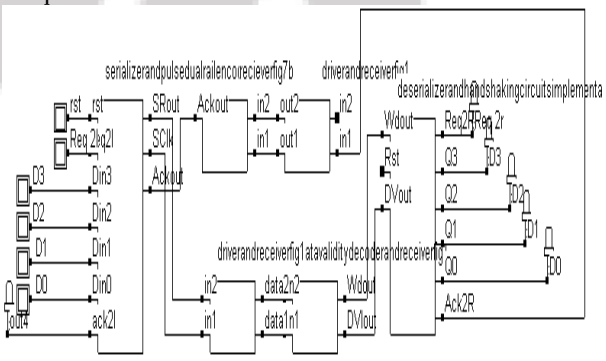

Figure 2.1: Block diagram of the proposed serial on-chip link

2.1. Communication Protocol

It is assumed that the sender and receiver modules have two-phase bundled-data interface. As soon as there is a request from the sender module which informs the data to be sent are ready and stable, the data will be loaded into the shift register. In addition to the data, the *Stop* bit is also loaded which will be used to stop the shifting in the deserializer without the need for additional control logic such as data bit counter. The locally generated clock starts running after parallel data loading is completed. It is used for data shifting and dual-rail data encoding. It is a stoppable clock that runs only when there is data in the shift register to be transmitted and stopped at all other time, saving the communication power significantly. Data is shifted at the negative edge of the clock and encoded when the clock is in *high* state. The counter counts at the negative edge of the clock and signals the completion of data shifting when it reaches the maximum count value, which in turn stops the clock. Dual-rail and differential pulse current-mode signaling is used for data transmission through the wire. Acknowledgment is sent per word instead of per bit thanks to the devised delay-insensitive wave-pipelining in the wire. In the receiving side, the transmitted data is retrieved directly from the receiver without the need for data decoding logic. The extracted data validity indicator is used as a clock for shifting the data in the deserializer. Shifting is performed at both edges of the data validity indicator signal. The arrival of *Stop* bit at the last flip-flop of the deserializer indicates that shifting is completed and the data are ready for parallel bit out. At this point, request to the receiving router will be sent. The deserializer shift register will be cleared when an acknowledgment from the data receiving module is received. The deserializer consists of a shift register and interfacing circuit between the serial link and receiving router. The data receiver output *Wdout* is shifted in the deserializer shift register at both edges of data validity indicator signal, *DVIout*. The shifting process will be stopped when the *Stop* bit reaches to the shift register's last flipflop. *Req2R* and *Ack2R* are the bundled-data interface between the link and receiving block (Figure 2.1). *RstH* signal resets the deserializer's shift register.

2.2. Serializer and Pulse Dual-Rail Encoder

The bit parallel data from the sender is serialized using a novel shift register which uses the locally generated clock to shift the stored data. As shown in Fig 2.2, the serializer consists of shift register, counter, clock generating circuit and other interfacing elements. The shift register is shown in Fig.2.4 and the counter is shown in Fig.2.3. The design of the shift register is based on True Single-Phase-Clocked (TSPC) flip-flops [7] and customized to have parallel data loading ability. TSPC is chosen because of its ability to embed logic, parallel data loading in this case, with very little delay overhead. In addition, it has much smaller setup time and propagation delay compared to other dynamic flip-flops, making it the most suitable to realize high-speed shift registers. The customized TSPC circuit with parallel loading is shown in Fig.2.2. In the loading phase, transistors *Mns* and *Mnr* are used to load bit '1' and bit '0', respectively and transistor *Mps* decouples *D* from node *L1* (preventing error when *D* is '0' and data to be loaded is '1'). The tri-state weak inverter is used as a keeper for the loaded data. There are two 3-input upper asymmetric C-elements (*C1* and *C2*) in the serializer circuit, shown in Fig.2.2, that are used to generate the local clock and keeper enable signals. The output of the NOR gates act the active-low reset signal for C1 and C2. The implementation of 3-input upper asymmetric c-element is shown in Fig.2.6.

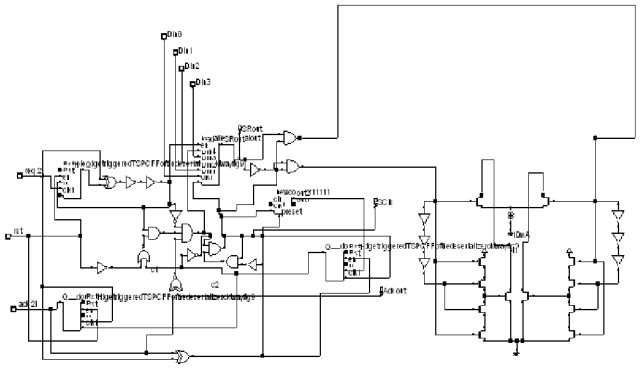

Figure 2.2: Serializer and Pulse dual-rail encoder

One-hot counter is designed from shift register so that its delay becomes equivalent to the data shift register in the serializer. As in the serializer's shift register, the counter shifts its one-hot code at the negative edge of the clock. Its shift register is designed from TSPC flip-flops which are customized to support active-low reset. For *N*-bit word counter, *N* TSPC flip-flops are connected in series and the last flip-flop's output is inverted and feedback to the first flip-flop's input.

The delay-insensitive data transfer, such as the dual-rail encoded interconnect, is a necessity in global interconnects of a nanometer SoC [8]. The delay-insensitivity makes the data transfer robust, because the sender and the receiver modules can communicate reliably regardless of delays in the transceivers and wires. Delay-insensitive data encoding technique requires *2N* wires to transmit *N*-bit data. Pulse dual-rail encoding, where the presence of a new valid bit is represented by a pulse instead of voltage transitions or levels, is formulated and used in the presented serial link. This encoding enables straightforward use of pulse signaling. Furthermore it has simpler and faster encoding/decoding logic when it is used along with differential signaling than the transition based protocols. When the clock is *high*, the dual-rail encoder, shown in Fig. 2.2, encodes each bit into Pulse and No Pulse (*P*, *NP*) pair depending on its value. For example, when the output of the shift register is bit '1', and the clock is *high*, there is a pulse at the output of *AND1* and no pulse at the output of *AND0*.

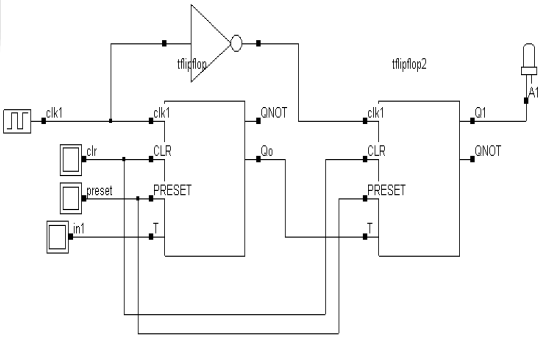

Figure 2.3: Counter

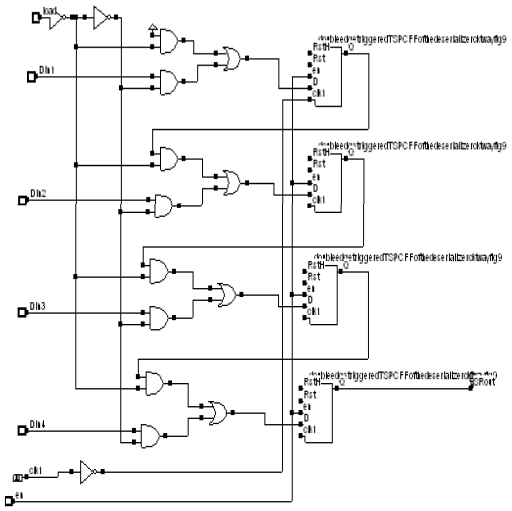

Figure 2.4: Parallel in serial out shift register

2.3 High-Speed Differential Pulse Current-Mode Signaling

In pulse signaling only a small portion of the wire is charged during pulse propagation, significantly reducing the amount of capacitance need to be charged and hence, saving considerable amount of power over level-based signaling. It has been shown that the use of pulse signaling can save up to 50% of energy compared to level-based signaling with repeater insertion [9]. Furthermore, it has been demonstrated through analytical models that more than 70% power saving could be achieved by combining pulse signaling with wave-pipelining technique without penalties of data throughput [10]. Since the main goal of this work is to achieve both high-speed global communication and low- power consumption, pulse signaling along with wave-pipelining is employed. In addition, differential current-mode signaling is used because of its high performance, better energy efficiency and noise immunity features [11][12][13]. Integration of dual-rail encoding and differential signaling has been realized using only two wires per link instead of four(two for dual-rail and two for dif- ferential signaling). This further reduces both power and required area of the link. In addition to power saving, pulse current-mode signaling mitigates the effect of dispersion due to its return-to-zero signaling scheme in which sharp current pulses are used to transmit data and receiver termination is employed. To make use of these promising advantages, the wires need to be modeled with consideration of the lossy on-chip environment. Wider and thicker wires with larger spacing than the minimum is preferred to ease attenuation and preserve pulse integrity. This can be realized with smaller area overhead in a serial link than in parallel links.

2.3.1. Driver

In this link, a source-coupled differential current-steering driver, shown in Fig. 2.7, is used. It is fast because it has an extremely sharp transient response. The driver has also an advantage of reducing the AC component of the power supply noise because the circuit draws constant current from the supply

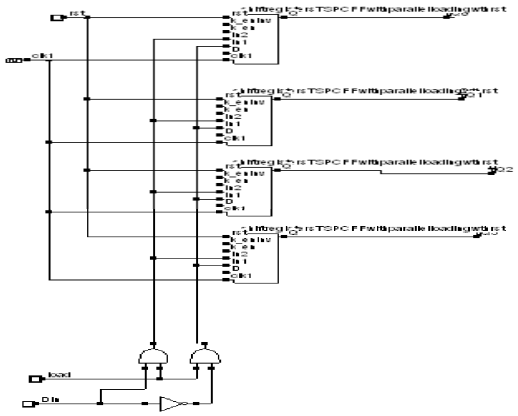

Figure 2.5: Shift register's TSPC FF with parallel loading

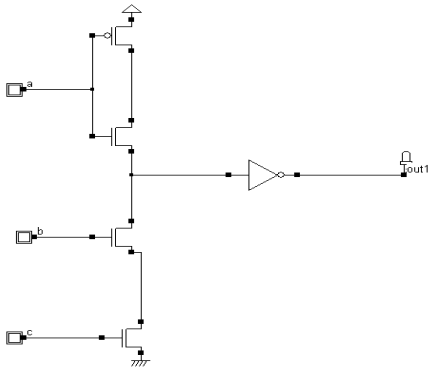

Figure 2.6: Upper asymmetric c-element

When it is operating. This driver is naturally suited to drive a balanced differential pair of wires. The complementary outputs of the driver are attached to the two wires. The other end of the transmission is parallel terminated into a positive voltage. Depending on the output of the dual-rail encoder, in other words input to the driver, current will be steered in one of the wires from the current source. When bit '1' is transmitted, a voltage pulse drives the gate of Mnp1 this in turn steers current pulse in wire1 and no current in wire0. And when bit '0' is transmitted, the current pulse is steered through Mnp0, which in turn steers the current pulse in wire0 and no current in wire1.

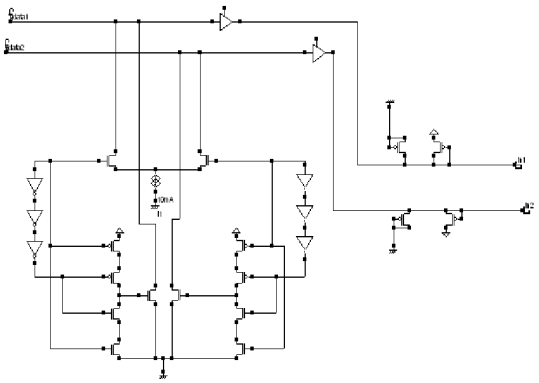

Figure 2.7: Driver and Pre-emphasis

2.3.2 Receiver

The termination load and receiver design is shown in Fig. 2.8. Diode connected Mpt0 and Mpt1 transistors are used as termination load. In ad- dition to termination, they are also used to mirror the wire current which will be needed to decode out data validity indicator. The transconductance of these transistors has been regulated through the use of Mpr0

and Mpr1. The receiver needs to have high common-mode noise rejection capability in order to take full advantage of differential signaling. Due to this, a high- speed self-biased differential amplifier is used. The differential amplifier used in this design has less sensitivity to process, temperature and supply voltage variations. It operates at high speed because its output switching currents are significantly greater than its quiescent current. Furthermore, the adopted amplifier has higher differential-mode gain than conventional amplifiers and a large common-mode input range because its bias condition adjusts itself to accommodate the input swing [14] [15].

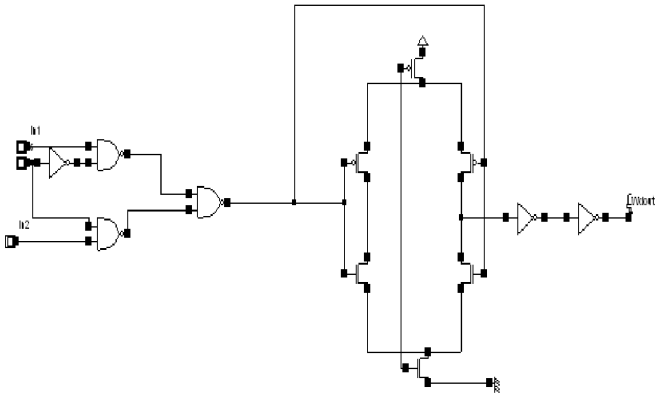

Figure 2.8: Receiver

2.3.3Data Validity Decoder

In delay-insensitive transmission, decoding of data and data validity in- dicator at the receiving end is necessary. The transmitted data is received and decoded out directly in the receiver without the need for separate data decoding logic. This is due to the novel integration of pulse and differential signaling. The remaining issue is data validity indicator, which will also be used as a clock to shift the data bit in the deserializer. From the encoding, it is known that there will be current only in one of the wires when there is valid bit transmission and no current in both wires between two consecutive bit transmissions. Each wire's current is compared with a reference current using a current comparator and the output of the two current comparators is fed to a differential amplifier. The output of the differential amplifier is the data validity indicator (DVIout). This way of completion detection makes the communication robust to both delay variations and noise because it takes into account both wires and the used differential amplifier, which has a high common-mode noise rejection ratio. Both edges of DVIout signal indicate the availability of valid and new data at the receiver output. The circuit of the data validity decoder is shown in Fig.2.9.

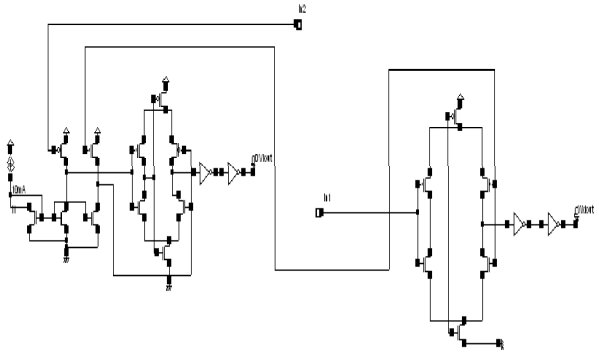

Figure 2.9: Data Validity decoder

2.4. Deserializer

The deserializer consists of a shift register and interfacing circuit (between the receiving module and the deserializer) as shown in Fig .10. In shift register data is shifted out at both edges of the DVIout signal. The shift register is designed from double-edge-triggered flip-flops. This flip-flop is designed by tying together the outputs of a negative and a positive edge-triggered TSPC flip-flops, obtaining multiplexer function for free. It stores dynamically during opposite clock phases and drives its output actively on both clock edges. The circuit of a double-edge-triggered flip-flop is shown in Fig.2.11. Mnrs1 and Mnrs2 transistors are used for resetting the flip-flop. When Stop bit reaches the last FF, the shifting will be stopped and data can be read out in parallel. The bundled-data two-phase request signal for parallel data receiving module is generated using a D-FF as shown in the interfacing circuit Fig.2.10. As soon as an acknowledgment is received, the deserializer's shift register will be cleared (resetted).

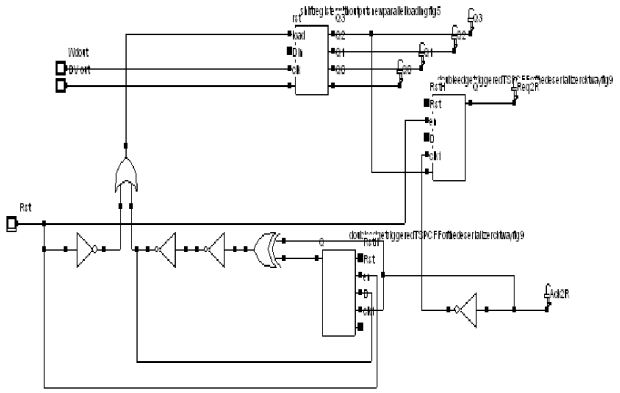

Figure 2.10: Deserializer and handshaking Circuits Implementation

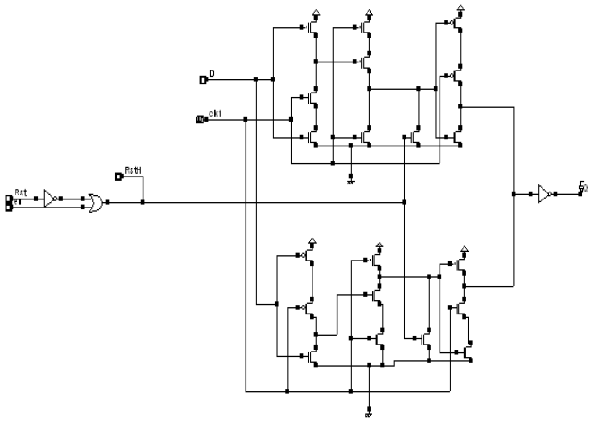

Figure 2.11: Double-edge triggered TSPC FF of the deserializer

3. Simulation Results and Analysis

The performance, power consumption, and energy per bit of the presented serial link are discussed in this section. The performance, power consumption, and energy per bit of the presented serial link are discussed in this section. The simulation results are shown in below.

Table 3.1: Serializer

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	14.573 Mw	0.259 ns	3.774 pw-sec	1487689 λ^2	Iddmax=13.554mA Idd avr=3.818mA
Cmos 012.rul	7.185 Mw	0.141 ns	1.013 pw-sec	1500696 λ^2	Iddmax=11.207mA Idd avr=3.136mA
Cmos 65n	4,509 mW	0.064 ns	0.288 pw-sec	1471680 λ^2	Idd max=9,391mA Idd avr=2.362mA

Table 3.2: Counter

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	97.424 µW	0.038 ns	3.702x 10^{-15}w-sec	59823 λ^2	Idd max=4.096mA Idd avr=0.186mA
Cmos 012.rul	26.252 µW	0.015 ns	0.997x 10^{-15}w-sec	59041 λ^2	Idd max=4.148mA Idd avr=0.229mA
Cmos 65n	14.831 µW	0.009 ns	0.133x 10^{-15}w-sec	60522 λ^2	Idd max=3.497mA Idd avr=0.205mA

Table 3.3: Parallel in Serial Out Shift Register

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	4.934 mW	0.096 ns	0.473 pw-sec	dx=2196 λ dy=496 λ =1089216 λ^2	Iddmax=7.304mA Idd avr=1.675mA
Cmos 012.rul	2.716 mW	0.043 ns	0.116 pw-sec	dx=2189 λ dy=489 λ =1070421 λ^2	Idd max=7.588mA Idd avr=1.578mA
Cmos 65n	1.673 mW	0.035 ns	0.058 pw-sec	dx=2191 λ dy=486 λ =1064826 λ^2	Idd max=5.740mA Idd avr=1.153mA

Table 3.4: Shift Register's TSPCFF with Parallel Loading

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	1.384 mW	0.063 ns	0.087 pw-sec	338910 λ^2	Idd max=8.592mA Idd avr=0.330mA
Cmos 012.rul	70.626 µW	0.026 ns	1.836 x 10^{-15}w-sec	374220 λ^2	Idd max=2.338mA Idd avr=0.009mA
Cmos 65n	0.488 mW	0.017 ns	0.008 pw-sec	350472 λ^2	Idd max=6.073mA Idd avr=0.356mA

Table 3.5: Upper Asymmetric C-Element

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	4.362 mW	0.033 ns	0.143 pw-sec	444564 λ^2	Idd max=9.286mA Idd avr=0.472mA
Cmos 012.rul	0.646 mW	0.011 ns	0.001 pw-sec	468046 λ^2	Idd max=6.082mA Idd avr=0.538mA
Cmos 65n	1.527mW	0.007 ns	0.010 pw-sec	439318 λ^2	Idd max=8.146mA Idd avr=0.561mA

Table 3.6: Driver

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	4.510 mW	0.045 ns	0.202 pw-sec	241301 λ^2	Idd max=5.580mA Idd avr=0.884mA
Cmos 012.rul	2.032 mW	0.015 ns	0.030 pw-sec	270643 λ^2	Idd max=4.583mA Idd avr=0.655mA
Cmos 65n	1.656 mW	0.010 ns	0.016 pw-sec	244352 λ^2	Idd max=4.445mA Idd avr=0.665mA

Table 3.7: Data validity Decoder

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	26.031 µW	0.050 ns	1.301x10^{-15} w-sec	92518 λ^2	Idd max=0.058mA Idd avr=0.001mA
Cmos 012.rul	3.972 µW	0.018 ns	0.071x10^{-15} w-sec	94010 λ^2	Idd max=0.029mA Idd avr=0.000mA
Cmos 65n	2.225 µW	0.012 ns	0.026x10^{-15} w-sec	96188 λ^2	Idd max=0.036mA Idd avr=0.000mA

Table 3.8: Receiver

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	56.608 µW	0.054 ns	3.056x 10^{-15}w-sec	49200 λ^2	Idd max=0.791mA Idd avr=0.009mA
Cmos 012.rul	11.531 µW	0.026 ns	0.299x10^{-15} w-sec	53111 λ^2	Idd max=1.031mA Idd avr=0.004mA
Cmos 65n	4.985 µW	0.038 ns	0.189x10^{-15} w-sec	52438 λ^2	Idd max=0.553mA Idd avr=0.002mA

Table 3.9: Double-Edge Triggered TSPC FF of the Deserializer

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	1.001 mW	0.038 ns	0.038 pw-sec	80229 λ^2	dd max=0.791mA Idd avr=0.009mA
Cmos 012.rul	0.451 mW	0.014 ns	0.006 pw-sec	84862 λ^2	dd max=1.031mA Idd avr=0.004mA
Cmos 65n	0.352 mW	0.008 ns	0.002 pw-sec	75870 λ^2	dd max=0.553mA Idd avr=0.002mA

Table 3.10: DESERIALIZER

Technology	Power	Delay	Power-delay product	Area	Idd max & Idd avr
Cmos 018.rul	2.532 mW	0.151 ns	0.382 pw-sec	49200 λ^2	Idd max=4.293mA Idd avr=0.608mA
Cmos 012.rul	1.150 mW	0.067 ns	0.077 pw-sec	1032264 λ^2	Idd max=4.449mA Idd avr=0.526Ma
Cmos 65n	0.738 mW	0.052 ns	0.038 pw-sec	1022070 λ^2	Idd max=3.923mA Idd avr=0.412mA

Table 3.11: Semi Serial Link

Technology	Power	Delay	Power-delay Product	Area	Idd max & Idd avr
Cmos 018.rul	22.216 mW	0.247 ns	5.487 pw-sec	3944790 λ^2	Idd max=17.969mA Idd avr=5.583mA
Cmos 012.rul	6.518 mW	0.043 ns	0.280 pw-sec	4144628 λ^2	Idd max=11.586mA Idd avr=3.333mA
Cmos 65n	10.464 mW	0.115 ns	1.203 pw-sec	3989131 λ^2	Idd max=13.887mA Idd avr=4.341mA

4. Conclusion

The design and analysis of a high-throughput and low-power serial on-chip communication link is presented. The combination of pulse dual rail encoding, wave-pipelining, pulse signaling and differential current-mode signaling besides customization of serializer/deserializer circuits leads to a realization of high-throughput serial link with low power consumption. Our simulation results showed in the above. The links are designed and simulated using cmos 180nm, 120 and 65 nm technologies in microwind 3.1 cadtool. When technology scale down from 180nm to 65nm, power decreased from 22.216mw to 10.464mw, delay decreased from 0.247ns to 0.115ns and power-delay product varies from 5.487pw-sec to 1.203pw-sec. This link is a promising candidate for long-range NoC channels, which are needed inherently due to topologies or through customization of regular 2D networks.

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