Performance Evaluation of 1-Bit Full Adder Using Hybridizing PTL and GDI Techniques

K. Mallikarjuna[1], V. Lakshmi Vasudha[2]

[1] Associate Professor, School of Electronics & Communication Engineering,
RGMCET, Nandyal-518 501, Kurnool (dist), Andhra Pradesh, India

[2] M. Tech (ES), student, RGMCET, Nandyal-518501,
Kurnool (dist), Andhra Pradesh, India

Abstract: ***Most of the VLSI applications, such as DSP, image & video processing, and microprocessors, extensively use logic gates and arithmetic circuits. 1-bit full adder cell is the extensively use in arithmetic circuits. Gate diffusion input (GDI)—a new technique of low-power digital combinational circuit design—is described. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. In this paper an area and power efficient 9T adder design has been presented by hybridizing PTL and GDI techniques. The proposed adder design consist of 5 NMOS and 4 PMOS. A PTL based 5T XOR-XNOR module has been proposed to improve area at 65nm technology and compared with the previous XOR-XNOR design. The proposed Hybrid full adder design is based on this area efficient 5T XOR-XNOR module design. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the proposed full adder. Also the simulation of layout and parametric analysis has been done for the proposed full adder design. The performance of the proposed technique is evaluated and compared by implementing it in 8-bit CLA adder,4-bit RCA adder, 4-bit CSkA adder,4-bit CSelA adder,4-bit CSaA adder,, . Several logic circuits have been implemented in various design styles. Their properties are discussed; simulation results are reported, and presented.***

Keywords: Gate Diffusion Input, Pass transistor logic, CMOS, VLSI

1. Introduction

In most VLSI applications, arithmetic operations play an important role. Commonly used operations are addition, subtraction, multiplication and accumulation, and 1-bit Full Adder is the building block for most implementations of these operations. Obviously, enhancing the building block performance is critical for enhancing overall system performance and in present, the power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques, Second battery life in portable electronics [1]. Design of full adder by using conventional CMOS design style has been presented. To generate the output transistor level design of CMOS full adder contains total of 14 PMOS and 14 NMOS transistors and two CMOS inverter. All NMOS and PMOS transistors used in this circuit have the same W/L ratio. It is required to adjust the transistor dimensions individually to get optimized time domain performance of the circuit. In [2], [3], [4] the area and power delay performance of full adder designs by different logic styles have been investigate.

1.1. Full Adder

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the next less significant stage. The one-bit full adder's truth table is shown in table 1.

Table 1: Full Adder Truth Table

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	[illegible]	1	0
0	1	0	1	0
0	1	[illegible]	0	[illegible]
1	0	0	1	0
1	0	[illegible]	0	[illegible]
1	1	0	0	[illegible]
1	1	[illegible]	1	[illegible]

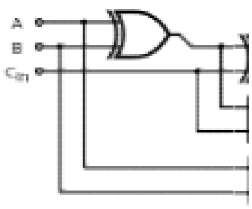

Figure1.1: Full Adder

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. One example implementation is with $S = A \oplus B \oplus C_{in}$ and

$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B))$$

In this implementation, the final OR gate before the carry out output may be replaced by an XOR gate without altering the resulting logic

In this way, Cout can be implemented as $C_{out} = (A \cdot B) \oplus (C_{in} \cdot (A \oplus B))$

2. Different Types of Full Adder Circuit

2.1 Conventional 28T CMOS Full adder

Working principle: Cout is generated first using above Cout equation. Then the sum is derived from the sum equation as shown in above.

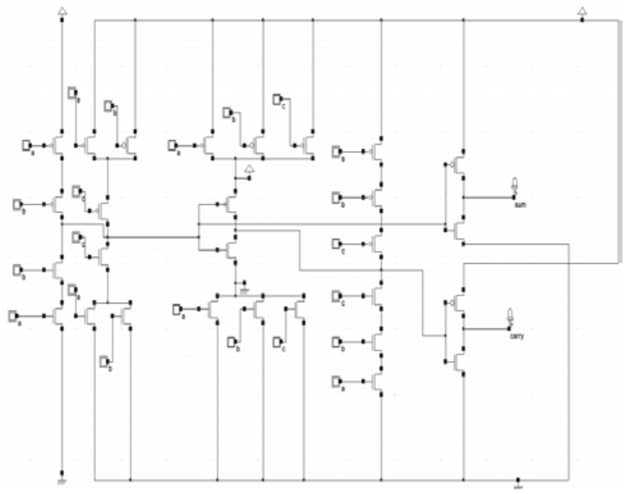

Figure2.1: 28TCMOS based Full Adder

Advantages: One of the most significant advantages of this full adder was its high noise margins and thus reliable operation at low voltages. The layout of CMOS gates was also simplified due to the complementary transistor pairs.

Disadvantages: But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

2.2 20T Transmission Gate Full Adder

It produces buffered outputs of proper polarity for both sum and carry with the disadvantage of high power consumption.

Working Principle: In the circuit we have 2 inverters followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. To generate sum; **cin** and are multiplexed which can controlled either by (**a b**) or (**a**⊗**b**).Similarly the Cout can be calculated by multiplexing **a** and **cin** which is controlled by (**a b**).

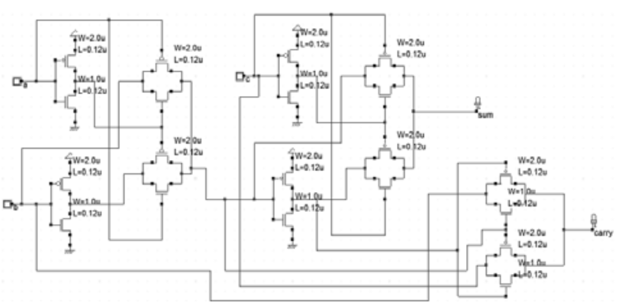

Figure2.2: Transmission Gate based Full Adder

Advantage: It is the fastest adder so far been reported. The circuit is simpler than the conventional adder.

Disadvantage: The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster [5].

2.3 14T Full Adder

The 14T full adder contains a 4T PTL XOR gate, shown in Fig 2.3, an inverter and two transmission gates based multiplexer designs for sum and C_{out} signals.

Working Principle: This circuit has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and $C_{out.}$ The signals C_{in} and are multiplexed which can controlled either by (a ⊕ b) or (a ⊗ b). Similarly the C_{out} can be calculated by multiplexing a and c_{in} controlled by (a⊕ b).

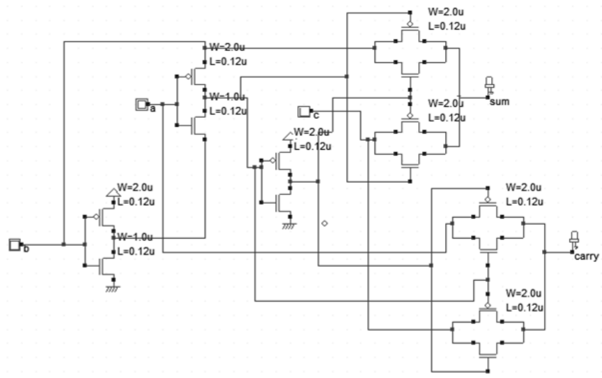

Figure2.3: 14T Full Adder

Advantage: It is the fastest adder so far been reported. The circuit is simpler than the conventional adder.

Disadvantage: The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster [6].

3. Basic Gate Diffusion Input(GDI Cell) Function

Gate Diffusion Input (GDI CELL) method is based on the use of a simple cell as shown in Figure below. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences:

1. Gate Diffusion Input (GDI CELL) contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
2. Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.

It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS technologies. A simple change of the input configuration of the simple Gate Diffusion Input (GDI) CELL as shown in Figure 3.1 corresponds to six different Boolean functions [7].

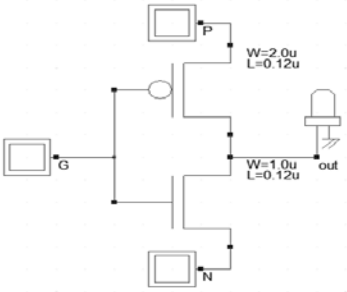

Figure3.1: Basic Gate Diffusion Input Cell

Table 2 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method. In this paper, most of the designed circuits were based on the F1 and F2 functions. The reasons for this are as follows.

1. Both F1 and F2 are complete logic families (allows realization of any possible two-input logic function).
2. F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any NMOS is constantly and equally biased.
3. When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to out are directly polarized and there is a short between N and P, resulting in static power dissipation and V_{out} ~0.5Vdd [7].

Table 2: Various logic functions of GDI cell for different input configurations

N	*P*	*G*	*D*	*Function*
‘0’	B	A	A`B	F1
B	‘1’	A	A`+B	F2
‘1’	B	A	A+B	OR
B	‘0’	A	AB	AND
C	B	A	A`B+AC	MUX
‘0’	‘1’	A	A`	NOT
B`	B	A	A`B+ B`A	XOR
B	B`	A	A`B` +AB	XNOR

3.1 10TFull Adder realized by Gate diffusion input (GDI) structures

XOR function is the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. In this new cell, we have used the Gate Diffusion Input (GDI CELL) technique for generating of XOR function.

Working Principle: 1-bit full adder circuit requires two XOR gate and one MUX. Gate Diffusion Input (GDI CELL) XOR gate which can be implemented by 4-transistor and MUX function which can be implemented by 2-transistor. Gate Diffusion Input (GDI CELL) 1-bit full adder requires only 10-transistor. Hence attempt to create 10-transistor based full adder is achieved. 10-transistor full adder is shown in Figure 3.2.

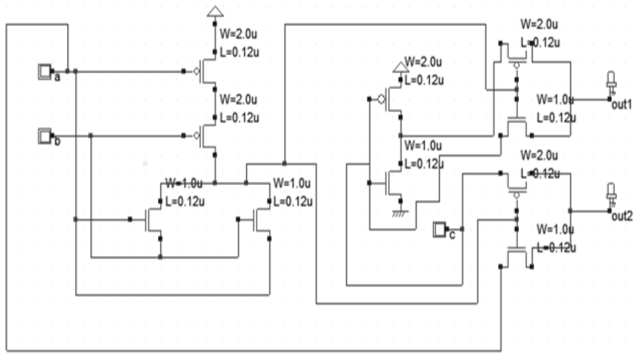

Figure3.2: 10T Full adder

Advantage: These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count.

Disadvantage: The major problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more expensive to realize a GDI chip. Moreover if only standard p-well CMOS process is used, the GDI scheme will face the problem of lacking driving capability which makes it more expensive and difficult to realize as a feasible chip [7].

3.2 Proposed Adder Schematic

The design of propose full adder consists three modules. Module1 comprises 5T XOR –XNOR module. Module 1 produces two intermediate signals which are passed to the module 2 and module 3 to obtain sum and carry output as shown in Fig 3.3. Module 2 and 3 are GDI 2x1 MUX with different input and select lines which produce carry and sum output respectively.

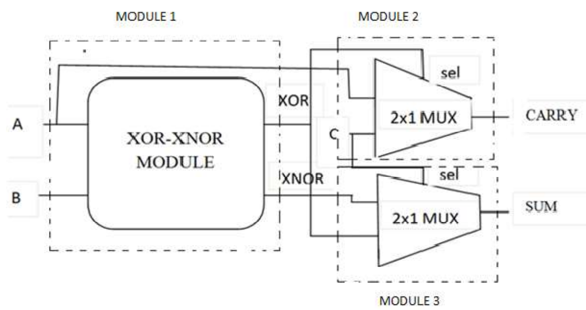

Figure 3.3: Logic Block Diagram of Proposed Full Adder

Proposed full adder has been implemented by using only 9 transistors i.e. five transistors in module1 [2], [3], [8] and module 2and 3 [8] has been implemented by using 2T GDI cell. This proposed adder is shown in Figure 3.4

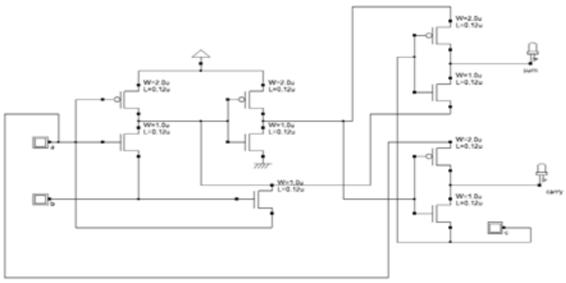

Figure3.4: Proposed 9T Hybrid Full Adder Design

Proposed hybrid full adder and its timing simulation have been shown in Figure 3.4 and 3.5

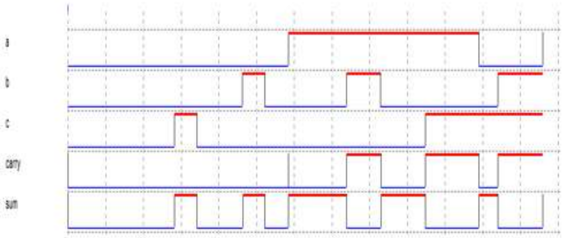

Figure3.5: Timing Simulation of Proposed Hybrid Full adder

Advantage of 9T Full adder: It consumes less power higher speed compared to previous Full adders. It is more efficient in terms of No of transistors required.

3.3 Layout Analysis

Before the actual layout design it necessary to validate the schematic of logic circuit. DSCH and MICROWIND designing tools works parallel. Firstly the design is simulated in DSCH designing tools to know the exact functionality of the circuit. The schematic diagram has firstly designed and validated using DSCH tool at logic level. Although at logic level DSCH have feature to analyze timing simulation as well as power consumption but accurate layout information is still missing. Verilog file is generated by the DSCH tool which is understandable by the MICROWIND to construct the corresponding layout with exact desired design rules. The advantage of this approach is to avoid any design rule error. W/L can be adjusted by the MOS generator option on microwind tool.

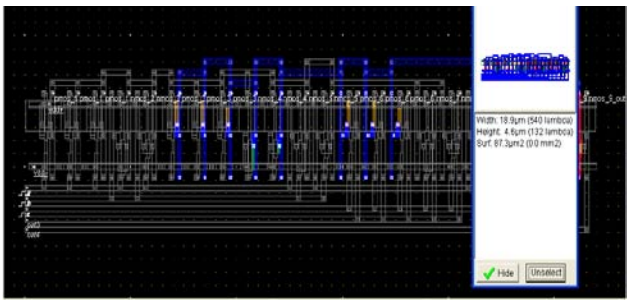

Figure3.6: Layout of Proposed Full Adder on 65nm

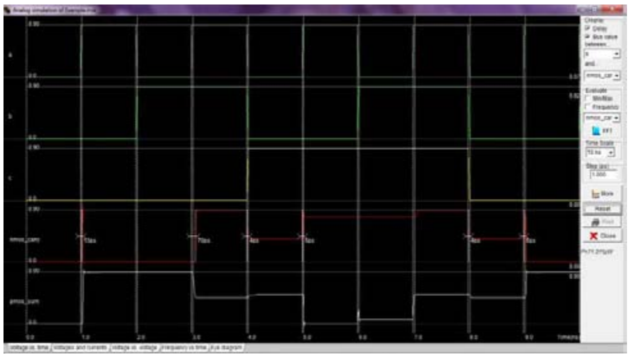

Figure3.7: Analog Simulation of proposed full adder on 65nm

The simulation of proposed hybrid adder design is shown in Table 3 and comparisons of full adders are also shown in Table 4.

4. Different Types of High Level Adders Design

Arithmetic functions such as addition and multiplication have a special significance in VLSI designs. Many applications require these basic operations, but good silicon implementations have been a challenge since the early days digital chip building. This section presents the design of adders. In this work the following adder structures are used.

4.1 Ripple Carry Adder (RCA)

Working Principle: The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. The digital schematic of RCA is shown in Figure 4.1.

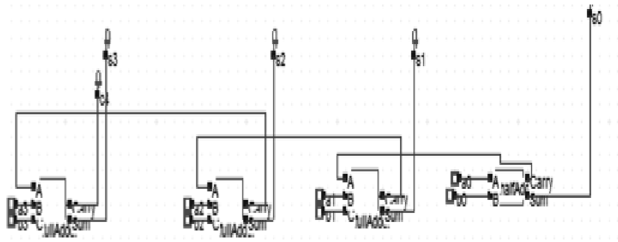

Figure4.1: Design of Ripple carry adder

Advantage: The RCA are lower power consumption as well as compact layout giving smaller chip area.

Disadvantage: Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length.

Worst case: The worst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by:

$$t = (n - 1)\, t_c + t_s \quad (1)$$

where t_c is the delay through the carry stage of a full adder, and t_s is the delay to compute the sum of the last stage[9].

4.2 Carry Look-Ahead Adder

Working principle: This adder consists of three stages: a propagate block/ generate block, a sum generator and carry generator. The generate block can be realized using the expression

$G_i = A_i . B_i$ for i=0, 1, 2, 3 (2)

Similarly the propagate block can be realized using the expression

$P_i = A_i \oplus B_i$ for i = 0,1,2,3 (3)

The carry output of the (i.1) th stage is obtained from

$C_i (C_{out}) = G_i + P_i C_{i-1}$ for i=0, 1, 2, 3 (4)

The sum output can be obtained using

$S_i = A_i \oplus B_i C_{i-1}$ for i= 0,1,2,3 (5)

The digital schematic of CLA is shown in Figure 4.2.

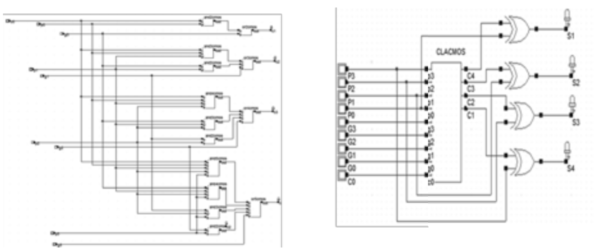

Figure 4.2: Design of carry look ahead adder

Advantage: Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. The propagation delay occurred in the parallel adders can be eliminated by carry look ahead adder. These adders is based on the principle of looking at the lower order bits of the augends and add end if a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate.

Disadvantage: In this carry logic blocks gets complicated for more than 4 bits.

Worst case: Timing simulation is difficult and also it is difficult to determine the delay of the sum bits and the carry out bits Cout [10], [11].

4.3 Carry Skip Adder (CSkA)

Working Principle: The carry-skip circuitry consists of two logic gates. The AND gate accepts the carry-in bit and compares it to the group propagate signal

$P[i, i + 3] = p_{i + 3} \bullet p_{i + 2} \bullet p_{i + 1} \bullet p_i$ (6)

using the individual propagate values. The output from the AND gate is ORed with cout of RCA to produce a stage output

$carry = c_{i + 4} + p[i, i + 3] \bullet c_i$ (7)

If p[i, i + 3] =0, then the carry-out of the group is determined by the value of $c_{i + 4}$. However, if p[i , i + 3] =1 when the carry-in bit is c_i =1, then the group carry-in is automatically sent to the next group of adders. The design schematic of Carry Skip Adder is shown in Figure 4.3.

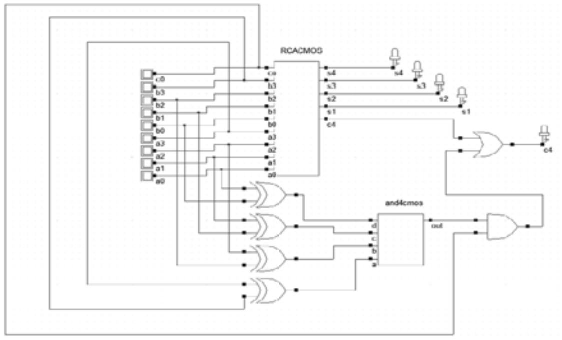

Figure 4.3: Design of Carry skip adder

Advantage: Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place, low in cost, low chip area, low power consumption. It improves the delay of RCA.

Disadvantage: The carry skip adder is more complicated circuit.

Worst case: If ripple adders are used then the worst case situations is where this bit emerges as C4=1, and then skips the next segment groups and enters the final blocks [10].

4.4 Carry Select Adder (CSelA)

Working Principle: A carry-select adder is divided into sectors, each of which except for the least-significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The Digital schematic is shown in Figure 4.4.

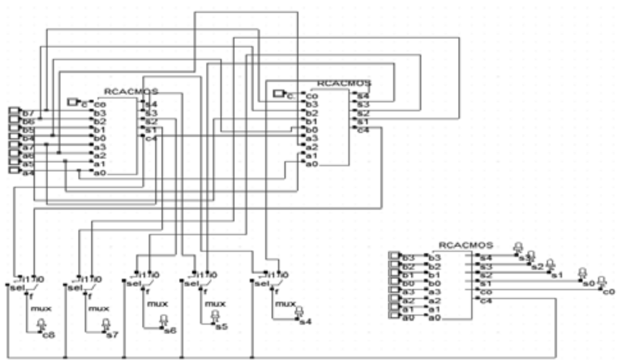

Figure4.4: Design of Carry select adder

Advantage: The carry-select adder is simple but rather fast, having a gate level depth of O ($\sqrt{n}$).It performs fast arithmetic functions, Low power but very fast. It reduces the propagation delay.

Disadvantage: For lower order bits also it covers more area, increases the hard ware cost. Design is complex [12].

4.5 Carry Save Adder (CSaA)

Working Principle: The carry-save unit consists of n full adders, each of which computes a single sum and carries bit based solely on the corresponding bits of the three input numbers. The entire sum can then be computed by shifting the carry sequence left by one place and appending a 0 to the front (most significant bit) of the partial sum sequence and adding this sequence with RCA produces the resulting n + 1 bit value. The design schematic of Carry Save Adder is shown in Figure 4.5.

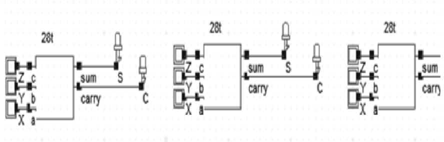

Figure4.5: Design of Carry save adder

Advantage: The carry save adder allows high clock speed. . The main application of carry save algorithm is, well known for multiplier architecture is used for efficient CMOS implementation of much wider variety of algorithms for high speed digital signal processing .CSA applied in the partial product line of array multipliers will speed up the carry propagation in the array The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is 3 gates regardless of the number of bits [9].

5. Simulated Results and Discussion

5.1 Comparisons and Results

For each technique, average power, area, and number of transistors were measured. The results are given in Table below.

5.2 Number of transistors comparison

Among all the design techniques, GDI proves to have the minimal number of transistors. Each GDI gate was implemented using only two transistors. The worst case, with respect to transistor count, is for the CMOS MUX gate (multiplexers are the well-known domain of pass-transistor logic). In this sense, the PTL techniques prove to be inferior compared to GDI.

5.3 Power dissipation comparison

Results are given for power dissipation in different gates. Consistently for all design techniques, the MUX gate has the largest power consumption because of its complicated implementation (CMOS) and the presence of additional input. On the other hand, AND's power dissipation is the minimal among all the gates. Still, most GDI logic gates prove to be the most power efficient among the four compared design techniques.

5.4 Discussion

Among the presented design techniques, GDI proves to have the best performance values and lowest transistor count. Even in the cases where power or area parameters of some GDI gates are inferior, compared to TG or CMOS, the power, area and transistor count of GDI are lower. Only the TG design method is a viable alternative for GDI if high-frequency operation is of concern.

Table 3: Simulation results of proposed Hybrid Full Adder Design

Design Technology	5T PTL XOR-XNOR Module and GDI MUX based Hybrid Full Adder On **65nm**
Area(μm2)	A=87.3(μm2) W=18.9(μm) L= 4.6(μm)
Threshold Voltage	**1.4v**
Supply Voltage(V)	1.2V
Power Dissipation (μW)	71.3 μW
Temperature (^0C)	27^0 C
NMOS	5
PMOS	4

Table4: Comparison of all Full adders

Adders	*Power (μW)*	*Area (μm2)*	*NMOS*	*PMOS*
CONVENTIONAL 28T CMOS FULL ADDER	1.211mw	259.6 μm2	14	14
20T TRANSMISSION GATE FULL ADDER	0.358mw	243.5 μm2	10	10
14T FULL ADDER	77.509μw	137.8 μm2	7	7
10T FULL ADDERS REALIZED BY GATE DIFFUSION INPUT (GDI)	73.582μw	105.0μm2	5	5
9T HYBRID FULL ADEER	71.3μw	87.3 μm2	5	4

Table 5: Simulated results of GDI and CMOS adders

Adders	*Power(mw)*		*Area(μm^2)*		*CMOS*		*GDI*	
	CMOS	*GDI*	*CMOS*	*GDI*	*NMOS*	*PMOS*	*NMOS*	*PMOS*
RCA	8.746	0.643	1148.2	281.0	56	56	20	16
CLA	13.707	0.132	2148.6	1448.7	60	60	30	30
CSkA	9.445	7.179	1529.8	466.8	78	78	32	28
CSelA	31.494	2.948	3406.1	1949.0	172	172	65	53
CSaA	4.899	0.476	578.2	207.2	56	56	20	16

6. Conclusion

An alternative hybrid full adder design by using PTL based XOR-XNOR module and GDI MUX has been introduced which consist only 9 transistors. Proposed full adder has been implemented by using 5 NMOS and 4 PMOS transistors. A new area efficient XOR-XNOR module has been proposed which is designed by only 5 transistors. Proposed hybrid full adder model consume 71.3μw power at 65nm. Area and simulation of proposed full adder has been shown on 65nm technology. Area of proposed design is 87.3μm2 on 65nm technology. A GDI technique for low-power adders was presented. Implementations of different kinds of high level adder circuits are presented and also to determine the area and power of these adders both in CMOS and GDI Thus we can say GDI is superior over other styles.

7. Future Scope

The proposed techniques consumes less power higher speed compared to previous Full adders .We plan to come up with a suitable application in Digital signal processing. The issue of sequential logic design is currently being explored, as well as technology compatibility for CMOS and GDI process. More work is required in the automation of a logic design methodology based on GDI cells.

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Author Profile

Kethepalli Mallikarjuna received his B.E degree from Gulbarga University in Karnataka, India in the year 1991 and M.Tech (DSCE) from JNT University, Hyderabad in the year 2003. He is pursuing Ph.D in digital image processing field with JNT University, Kakinada, AP, India. He has more than two decades of teaching experience in Engineering. He has published several research papers which figured in International Journals.

V.LakshmiVasudha received her B-tech degree from Rajeev Gandhi Memorial College of Engineering And Technology in Electronics and Instrumentation and pursuing M-tech Degree in Rajeev Gandhi Memorial College of Engineering And Technology in the specialization Embedded System. Her research interest on high speed, low power VLSI designs.