

A Fibonacci Coding Technique to Avoid Crosstalk on On-Chip Data Bus

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Abstract: As VLSI technology has scale down to the deep sub-micrometer (DSM) technology the global interconnect delay is becoming a large fraction of the overall delay of a circuit. Additionally, the increasing cross-coupling capacitances between wires on the same metal layer create a situation where the delay of a wire is strongly dependent on the electrical state of its neighboring wires. So the crosstalk delay on a data bus is highly dependent on the data patterns transmitted on the data bus. Different crosstalk avoidance coding schemes have been proposed to increase the bus speed by decreasing the interconnect delay. By exploiting Fibonacci number a family of Fibonacci coding Techniques is proposed for crosstalk avoidance. The properties of the Fibonacci coding techniques which are used for crosstalk avoidance are analyzed and show that mathematically, a mapping scheme exists based on the presentation of numbers in the Fibonacci numeral system. Compared to the existing techniques these coding techniques require only 23 wires for 16 bit data. The proposed techniques evaluate the performance details of the Fibonacci coding techniques which avoids the crosstalk Class 4 and Class 3 completely. Hence crosstalk delay reduces which intern improves the overall performance of the system.

Keywords: Deep sub-micrometer technology, Crosstalk, Fibonacci number system

1. Introduction

As VLSI technology has grown into the deep sub-micrometer (DSM) regime, new challenges are presented to circuit designers. As one of the key challenges, the performance of bus based interconnects has become a bottleneck to the overall system performance. In large designs [e.g., systems-on chip (SoCs)] where long and wide global busses are used, interconnect delays often dominate logic delays.

Once negligible, crosstalk has become a major determinant of the total power consumption and delay of on-chip busses. Fig. 1.1 illustrates a simplified on-chip bus model with crosstalk. The impact of crosstalk in on-chip busses has been studied as part of the effort to improve the power and speed characteristics of the on-chip bus interconnects. C_L denotes the load capacitance seen by the driver, which includes the receiver gate capacitance and also the parasitic wire-to-substrate parasitic capacitance. C_1 is the inter-wire coupling capacitance between adjacent signal lines of the bus. For DSM processes, C_1 is much greater than C_L [4]. The delay, which determines the maximum speed of the bus, is limited by the maximum crosstalk that any wire in the bus incurs. It has been shown that reducing the crosstalk can boost the bus performance significantly [1] [2].

1.1. Crosstalk Classification

As stated in Section 1, the degree of crosstalk in an on-chip bus is dependent on data transition patterns on the bus. This model shown in Figure.1.1, the delay T_j of the j^{th} wire is given in equation (1) as in [1].

$$T_j = abs(k.C_L.\Delta V_j + k.C_1.\Delta V_{j,j-1} + k.C_1.\Delta V_{j,j+1}) \quad (1)$$

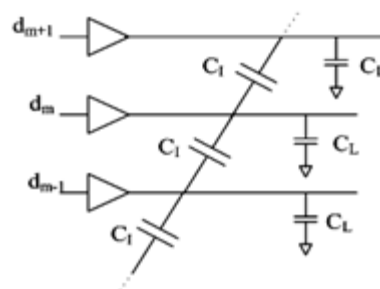


Figure.1.1: On-chip bus model with crosstalk

Depend upon the transmission patterns on the wire of interest and as well as its immediate neighbours on either side the crosstalk patterns can be classified into 0C, 1C, 2C, 3C, and 4C patterns, respectively.

Table 1: Crosstalk classification

Class	C_{eff}	Transition patterns
0c	C_L	000 \rightarrow 111
1c	$C_L(1+\lambda)$	011 \rightarrow 000
2c	$C_L(1+2\lambda)$	010 \rightarrow 000
3c	$C_L(1+3\lambda)$	010 \rightarrow 100
4c	$C_L(1+4\lambda)$	010 \rightarrow 101

Several techniques have been proposed in literature to eliminate crosstalk transitions. A simple technique to eliminate crosstalk transitions is to insert a shield wire between every pair of adjacent wires [3]. As there is no activity on shield wires, the shielding (SHD) technique completely eliminates crosstalk transitions. This technique can reduce the bus delay by nearly 50%. However, it requires doubling the number of wires and hence incurs a 100% area overhead.

*Forbidden pattern coding (FPC) technique [5] prohibits 010 and 101 patterns from code words, which in turn eliminates crosstalk transitions. It requires 52 wires for a 32-bit bus.

* By exploiting Fibonacci number system, a family of Fibonacci coding techniques for crosstalk avoidance [6] are proposed, give a generalized framework to generate crosstalk avoidance codes. For 32-bit data, these coding techniques require 40 and 46 wires, respectively, as compared to 63 wires required by the SHD technique. For 16-bit data, these coding techniques require 23 wires, respectively, as compared to 31 wires required by the SHD technique.

2. Fibonacci Number System

This works reports a systematic Crosstalk-free CODEC design approach which is based on the Fibonacci Numeral System (FNS). Fibonacci number system of order $s, s \geq 2$, is defined as $S=(F_s, \{0,1\})$, where $F_n = (f_n)_{n \geq 0}$ such that

$$f_i = 2^i \text{ for } 0 \leq i \leq s-1$$

$$f_i = f_{i-1} + \dots + f_{i-s} \text{ for } i \geq s.$$

An integer may have multiple representations in Fibonacci number system of order $s, s \geq 2$. To overcome the ambiguity in representing integers in Fibonacci number system of order $s, s \geq 2$, a *normal-form* [8] is defined, wherein each integer has a unique representation which does not contain s consecutive bits equal to 1.

3. Exploiting Fibonacci Representation For Crosstalk Avoidance

Throughout the paper, we use notation *dataword* and *codeword* for data to be encoded and encoded data, respectively. For every data word, we give a codeword using Fibonacci number system of order 2 such that the decimal equivalent of the data word is same as that of the codeword.

3.1 Normal-Form Fibonacci (NFF) Coding Technique

The NFF technique is described in two parts, namely, *data encoding* and *data transmission*. For data encoding, we use normal-form Fibonacci number system of order 2. For a n -bit data word, using the NFF technique, the unique m -bit codeword, can be generated using NFF encoding algorithm as shown in Table 2. Let NFF_m be the set of m -bit code words and it can be generated as follows.

$$NFF_0 = \phi$$

$$NFF_1 = \{0, 1\}$$

$$NFF_{m+2} = \{0x, 10y \mid \forall x \in NFF_{m+1}, \forall y \in NFF_m\}.$$

For example, transmission of NFF code words 0001 and 0010 results in crosstalk transitions in the least significant two bits. In order to avoid crosstalk transitions, NFF code words are transmitted using *transition signaling* (TS) technique, wherein data to be transmitted is XOR ed with the data present on the bus.

Table 2: NFF Encoding algorithm

```

Input: d;
r_m = d;
for k = m - 1 to 1 do
if r_{k+1} < f_k then
c_k = 0;
else
c_k = 1;
end if
r_k = r_{k+1} - f_k * c_k;
end for
c_0 = r_1;
Output: c_{m-1}c_{m-2}.....c_0;
    
```

3.2 Redundant Fibonacci (RF) Coding Technique

We now present a coding technique which does not require the TS technique to eliminate crosstalk transitions. In the case of NFF technique, Fibonacci numbers are considered as the basis elements to generate m -bit codewords. Similar to the NFF technique, in *redundant Fibonacci* (RF) coding technique we consider Fibonacci numbers as the basis elements with the exception that f_0 is used twice. That is, in order to generate m -bit RF codewords, we consider f_{m-1}, \dots, f_0, f_0 as the basis elements. As f_0 is considered twice in the RF technique, we get two sets of RF codewords; each is a complement of the other. We consider these two sets as *redundant Fibonacci* (RF) and *complement redundant Fibonacci* (CRF) codeword sets. Let RF_m be the set of m -bit RF code words. Then

$$RF_0 = \phi$$

$$RF_1 = \{0, 1\}$$

$$RF_{2m+2} = \{0x, 11y \mid \forall x \in RF_{2m+1}, \forall y \in RF_{2m}\}$$

$$RF_{2m+3} = \{1x, 00y \mid \forall x \in RF_{2m+2}, \forall y \in RF_{2m+1}\}.$$

The encoding logic given in [7] can be used for implementing the RF technique.

3.2 Complement Redundant Fibonacci (CRF) Coding Technique

CRF codewords are generated by taking bit-wise complement of each codeword from the set of RF codewords. Let CRF_m be the set of m -bit CRF codewords. Then

$$CRF_m = \{\bar{x} \mid \forall x \in RF_m\}.$$

The CRF Encoding algorithm shown in Table3. The code words for different coding technique are shown in Table 4.

Table 3: CRF Encoding algorithm

```

Input:  $\mathbf{d}$ ;
 $r_m = \mathbf{d}$ ;
for  $k = m - 1$  to  $1$  do
if  $r_{k+1} < f_{\lfloor \frac{k-1}{2} \rfloor}$  then
 $c_k = 0$ ;
else
 $c_k = 1$ ;
end if
 $r_k = r_{k+1} - f_{k-1} \cdot c_k$ ;
end for
 $c_0 = r_1$ ;
Output:  $c_{m-1}c_{m-2}\dots\dots\dots c_0$ ;
    
```

Table 4: Different coding technique code words

Data-word	Fibonacci codeword			
	NFF_4	NFF_4^{TS}	RF_4	CRF_4
010	0010	0010	0100	0011
101	1000	1010	1100	1011
011	0100	1110	0101	1000
110	1001	0111	1101	1110
111	1010	1101	1111	1111
000	0000	1101	0000	0000
001	0001	1100	0001	0010
010	0010	1110	0100	0011

4. Results

The proposed techniques performance is evaluated by applying 1000 random input patterns for different bus width (i.e. 3-, 8-, and 16-bit).

Figure4.1 describes the performance of NFF coding technique by applying 1000 random input patterns for different bus width (i.e. 3-, 8-, and 16-bit).

Figure4.2 describes the performance of RF coding techniques by applying 1000 random input patterns for different bus width (i.e. 3-, 8-, and 16-bit).

Figure4.3 describes the performance of CRF coding technique by applying 1000 random input patterns for different bus width (i.e. 3-, 8-, and 16-bit).

Table 4: The 4c and 3c Cross talk classes comparison between uncoded and coded bus for 1000 random inputs.

Bus width	Un-coded		coded					
	4C	3C	NFF		RF		CRF	
			4C	3C	4C	3C	4C	3C
3	451	138	0	0	0	0	0	0
8	442	597	0	0	0	0	0	0
16	1176	671	0	0	0	0	0	0

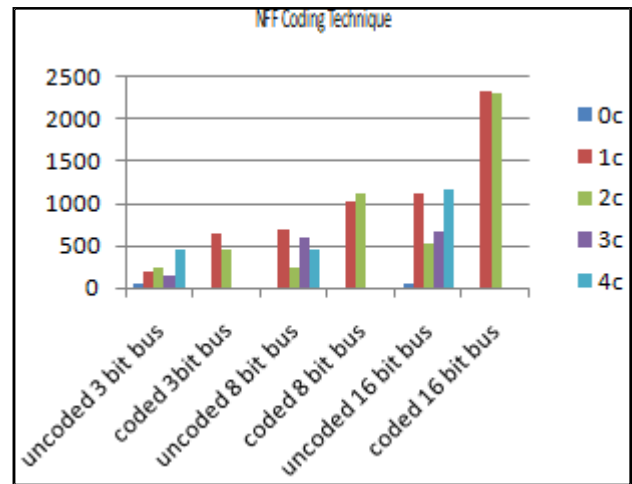


Figure 4.1: crosstalk classes count for 1000 inputs using NFF TS coding Technique.

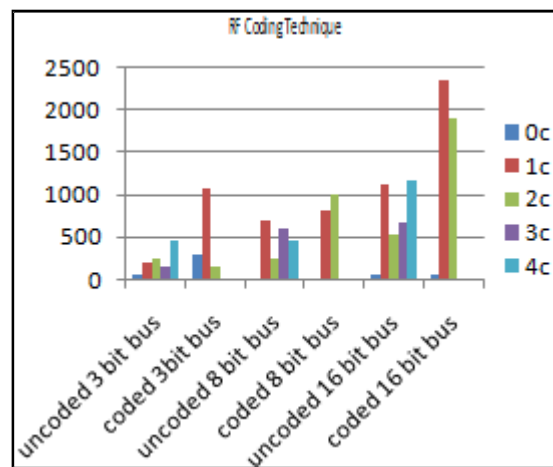


Figure 4.2: crosstalk classes count for 1000 inputs using RF coding Technique.

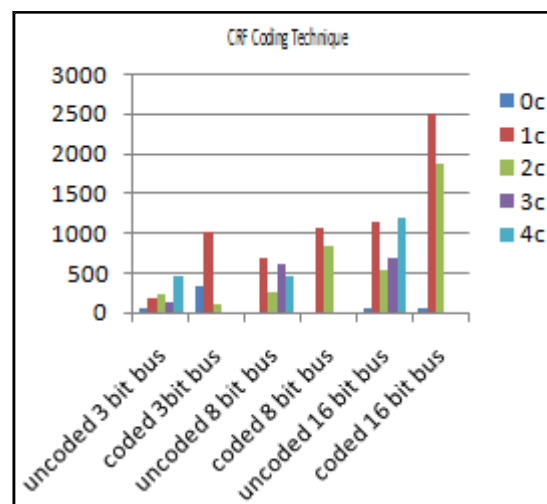


Figure4.3: crosstalk classes count for 1000 inputs using CRF coding Technique.

5. Conclusion

By exploiting Fibonacci number system, we proposed a family of Fibonacci coding techniques for crosstalk avoidance. Crosstalk avoidance codes have been developed to reduce the inter-wire crosstalk and therefore boost the

maximum speed on the data bus. These coding techniques require 23 wires for 16-bit data. So the number of wires requirement is less comparing to shielding technique and FPF-CAC. Hence the proposed techniques have the advantage of consuming less area overhead than shielding technique and FPF-CAC. The proposed techniques avoid the 3c and 4c crosstalk classes completely. The efficiency to avoid the 3c and 4c crosstalk classes for the proposed techniques is 100%.

6. Future Scope

The proposed techniques eliminate the 3c and 4c crosstalk classes completely. We plan to come up with a suitable mechanism to minimize the Energy dissipation using these Fibonacci codes.

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