Interleaved Voltage Source Converters Based Enhanced Asymmetric Space Vector Modulation for Total Harmonic Distortion Diminution

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Abstract: ***This paper presents the comparison between improved asymmetric space vector modulation (ASVM) and sinusoidal pulse width modulation (SPWM) for voltage source converters (VSCs) when the switching frequency is as low as 9 times of line frequency. By enumerating two pulses in every line cycle at the time of fundamental voltage reaches zero, the total harmonic distortion (THD) of output current can be condensed considerably. In high power factor operating areas the forfeit of reckoning switching loss is very circumscribed. The improved asymmetric vector modulation application in a single voltage source converter is shown. With the optimization of the duration and position of the additional pulses, the THD of ac current can be condensed to as below as 25% for single VSC. Such THD reduction has precise affiliation with space vectors' position and modulation index. Amplitude of the circulating current can also be condensed by improved ASVM, governing to smaller inter-phase inductors. The examination outcomes are confirmed by experiments on a demo system.***

Keywords: Voltage Source Converter (VSC), Total Harmonic Distortion (THD), Asymmetric Space Vector Modulation (ASVM).

1. Introduction

Asymmetric space vector modulation (ASVM) is a popular pulse-width modulation (PWM) scheme used for voltage source converters (VSCs) operated with low carrier ratio (Rc), which is denoted as the relationship between the switching frequency and operating ac frequency. When Rc is very low, ASVM, compared with symmetric SVM, has many benefits such as keeping the PWM waveforms symmetric in a line cycle, avoiding even order harmonic currents. Limited by the switching frequency of current power semiconductor devices, Rc, in high power applications, cannot be high. Particularly, for applications involving high speed generator or motor, Rc will be extremely low such as around 9. In many situations, still if the devices can operate at higher switching frequency, it is also enviable to use lower switching frequency, in order to decrease loss and amplify power capability. Low carrier ratio outcomes in lower order voltage harmonics. To circumscribe the current harmonics, large ac line inductors are normally essential, which can have cost and size penalty.

Therefore, it is very desirable to improve the ASVM algorithm for better harmonic performance, so lesser passive components can be used to meet the total harmonic distortion (THD) requirement for ac currents. The studies mainly focused on the impact of space vector sequence on the performance of space vector modulation and the harmonic current performance of these space vector modulations are very similar. But these methods cannot be used directly to the system with very low carrier ratio. In addition, how to maximize the current THD reduction in a VSC system and ASVM is still unknown. This paper presents a method to improve the harmonic current performance of ASVM with very limited penalty. With synchronized PWM, the THD of output current can be reduced by 50% compared with traditional ASVM when modulation index is high. With asymmetric, the THD of output current can be further reduced by more than 50% and additional benefit, reduced circulating current, is also presented.

For this paper, it is assumed that the modulating signal (triangular carrier) of the equivalent SPWM method has twenty per unit frequency. The switching transitions for each and every quarter period are therefore distributed between the converter levels according to the modulation index of SPWM. It is confirmed that the proposed technique offers significantly higher converter bandwidth and higher dc bus utilization for the same switching transitions. Finally, the potential benefit of such improved ASVM in increasing system power density is demonstrated by inductor physical design comparison.

Some papers have studied the performance of PWM with low carrier ratio. [6] and [7] compared four kinds of space vector modulations, including traditional asymmetric space vector modulation. [6] also investigated synchronized space vector modulation for active front-end rectifiers in high-power current-source drive. However, these studies mainly focused on the impact of space vector sequence on the performance of space vector modulation and the harmonic

current performance of these space vector modulations are very similar. [7]-[9] proposed methods to optimize the harmonic performance of converters under space vector modulation control. Section II explains the principle of the sinusoidal pulse width modulation (SPWM).

Section III explains the basic idea and principle of the proposed improved ASVM. Based on that, the method to apply such improved ASVM in a single VSC is shown in Section IV. With sinusoidal PWM, the THD of output current can be reduced by 50% compared with traditional PWM, when modulation index is high. With asymmetric interleaving [11], the THD of output current can be further reduced by more than 50% and additional benefit, reduced circulating current, is also presented.

Finally, the potential benefit of such improved ASVM in increasing system power density is demonstrated by inductor physical design comparison in Section V. All analyses are verified by experimental results in Section VI.

2. Principle Of Sinusoidal Pulse Width Modulation

Sinusoidal PWM (SPWM) has a relatively robust harmonic spectrum, i.e., the harmonic spectrum of the resulting waveform is tied to the selected switching frequency. In contrast, space vector modulation (SVM), which is a relatively new approach to waveform synthesis using a VSC, offers several degrees of freedom that can be used effectively to design an improved harmonic spectrum and obtain the desired waveform quality.

In PWM methods, the reference voltage is approximated by a number of voltage pulses at the converter output. The approach to determine the duration of such pulses is what constitutes the difference among various PWM methods. For example, in conventional SPWM, which is an analog domain method, the duration of each pulse is found through comparison of a sinusoidal reference waveform and a triangular carrier waveform as shown in fig.

A digital domain variation of PWM, which is the SVM, on the other hand, directly computes the duration of voltage pulses using the amplitude and angular location of the reference vector. When p < 21, it is recommended that synchronous PWM be used, which means that the T_C and the template should be synchronized. In addition, to keep away from sub harmonics, it is also preferred that p be an integer. If p is an odd number then surely, even harmonics will be eliminated.

If p is a multiple of 3, after that the PWM modulation of the three phases will be identical. When m increases, after that the amplitude of the fundamental voltage increases proportionally, but some harmonics decrease. Under over modulation (m > 1), the fundamental voltage does not increase linearly, and more harmonics appear.

Low order harmonics. n < (mf -2) are eliminated as shown in Fig. 2. Third Harmonic Injection is used in the circuit as shown in Fig. 3. Due to this, the triplen harmonics in line to line voltages, says V_{AB}, V_{BC}, V_{CA}, are eliminated.

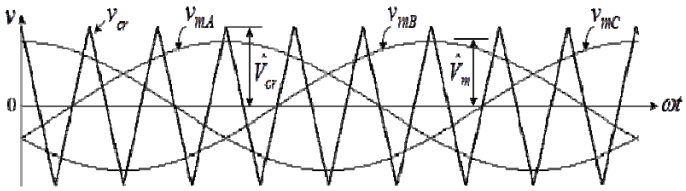

Fig.1: Comparison of a sinusoidal reference waveform and a triangular carrier waveform

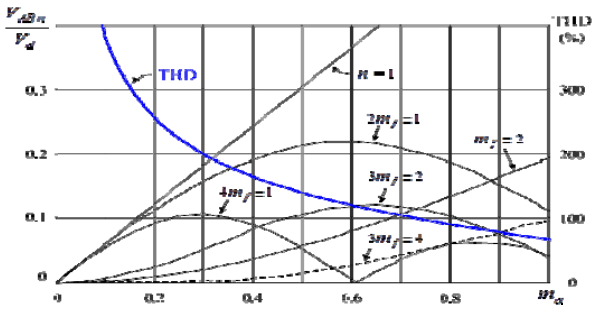

Fig. 2: Harmonic content

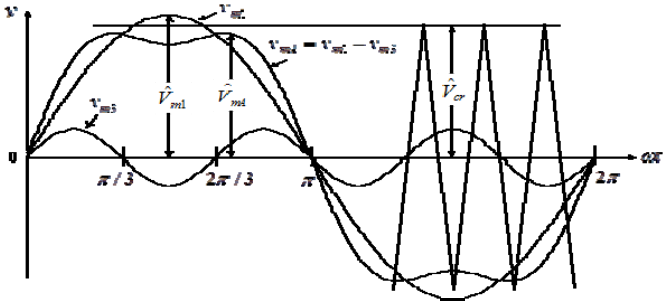

Fig. 3: Third Harmonic Injection PWM

The simulation circuit for the system under study with the gate pulses generated by using sinusoidal pulse width modulation is shown in Fig. 4. The THD obtained for this circuit is around 42.37%. So in order to reduce the THD valve, we are going on for space vector modulation technique. In order to reduce the THD value further, we are moving on to Improved ASVM technique.

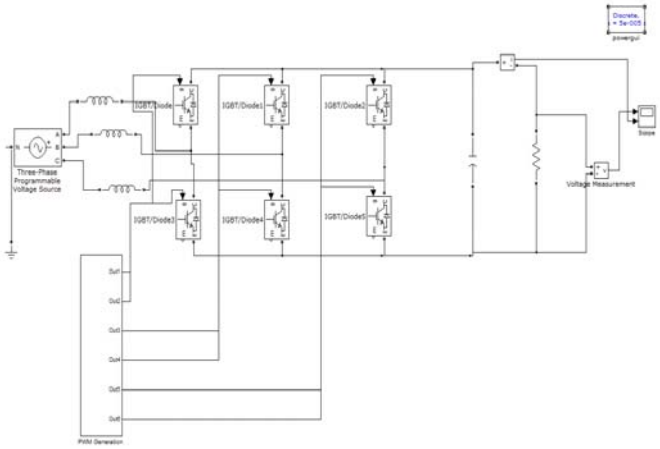

Fig. 4: Circuit for Sinusoidal PWM

3. Principle of Improved ASVM

Without loss of generality, the work in this paper is based on the example system shown in Fig. 5. The power flows from the generator (modeled as a voltage source connected

in series with a boost inductor) to the dc load (shown as a dc resistor). In the system under study, the ac line-to-neutral rms voltage is 230 V, the apparent power is 300 kVA, the dc bus voltage is 700V, the fundamental frequency varies between 500 Hz and 2 kHz, and ASVM is used. Following the conventional wisdom, an odd triplen R_C is preferred [9-10]. In this paper,

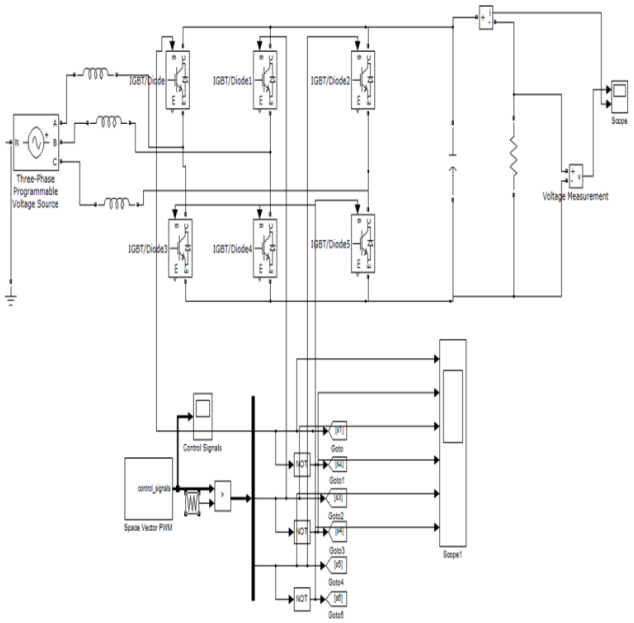

Fig. 5: Circuit diagram (VSI with SVPWM)

R_C is assumed to be 9. As a result, 18 vectors can be generated in one line cycle as shown in Fig. 6. Since lower switching frequency usually means higher system harmonic currents, the lowest switching frequency 4.5 kHz is selected for study. The corresponding fundamental frequency is 500 kHz.

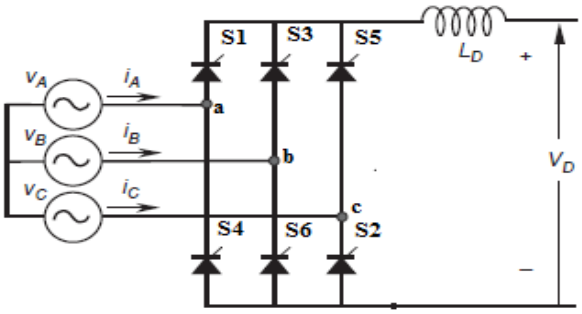

Fig. 6: Single VSC system under study

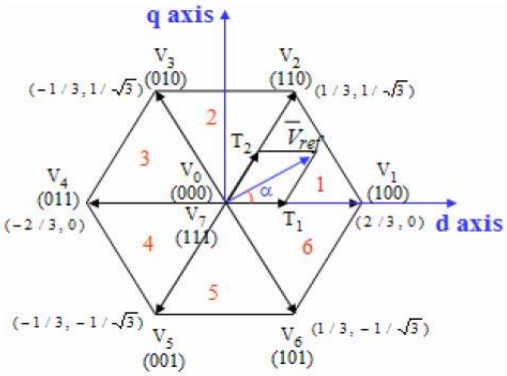

Fig. 7: Output vectors of ASVM (Rc=9)

4. Improved ASVM in a Single VSC

For the improved ASVM, k_1 and k_2 can be optimized to minimize the THD of output current in a single VSC system. However, the analytical analysis for calculating the optimized k_1 and k_2 is still under study. In this paper, the optimized k_1 and k_2 are obtained by exhaustive searching method. However, the optimized k1 is always around 0.2 and k_2 is always around 0.8 for vector 90 °. As a result, k_1 and k_2 are kept to be 0.2 and 0.8 for vector 90 °in all simulation and experiment. The optimized k_1 and k_2 and the corresponding minimized THD of output current has close relationship with modulation index and the position of vectors. Modulation index is determined by the system operating condition and it is assumed to be 0.9 for the analysis in this section, corresponding to rectifier applications or inverter applications under rated conditions. The THD in all cases are normalized to the value when traditional ASVM is used and V_{init} is at 1°. The cases when V_{init} is at 0° and 20° are not analyzed, since in these cases the output vectors can be on the boundary of adjacent sectors which should be avoided. The simulation circuit for Improved ASVM is shown in Fig.

5. Inductor Weight Reduction with Improved ASVM

For the example system shown in section IV, the simulations for VSC topology are performed for traditional and improved ASVM. From the simulation results, the THD of output current can be reduced from 4.3% to 2.1% with improved ASVM. In addition, the amplitude of circulating current is also reduced from 194A to 80A. Inductor physical design is done and summarized in Table I for each case to reduce the THD of output current to the same level 2.1%. In the design, Metglas amorphous Alloy 2605SA1 is used for core design, the temperature rise is limited within 100 °C, EE core is used for three inductor design and CC core is used for inter-phase inductor design. From Table I, improved ASVM can reduce the weight of required inductor significantly.

TABLE 1: Comparison of inductor weight

Case	Single VSC with Sinusoidal PWM	Single VSC with Improved ASVM
Additional inductors needed	one 300uH 3φ inductor	one 100uH 3φ inductor
Weight of total inductors	140kg (100%)	47kg (34%)

6. Experimental Results

The experiment is designed to verify key point that, the improved ASVM can reduce the THD of output current dramatically. Since in the analysis, the harmonic current is assumed to be only determined by inductance and harmonic voltage, the resistor load may change the amplitude of harmonic currents especially when switching frequency is low and the power factor is high.

However, the same setup is used for all PWM schemes, so the relative THD reduction of output current is still very close to the analysis results. The experimental setup comprises of 6-pack IGBT intelligent power modules (IPMs) from Fuji (6MBP20RH060) for two VSCs power stage, one common DSP-FPGA digital controller, three inter-phase inductors, one three phase inductor and three 6Ω resistors as load.

The ac line inductor is 400μH and the inter-phase inductor used to limit circulating current is 3mH. The dc voltage is 100V, and the fundamental and switching frequency are chosen as 500Hz and 4.5 kHz respectively. Synchronized PWM and close loop control are used for all cases. The reference RMS value of fundamental current in the resistor load is 6A with corresponding modulation index of 0.9.

The control signals and gate triggering pulses foe improves ASVM is shown in Fig. 8. and Fig. 10. respectively. The experimental waveforms for single VSC case with sinusoidal PWM and improved ASVM are shown in Fig. 9 and Fig. 11. The current THD value and RMS value of fundamental components are summarized in Table.

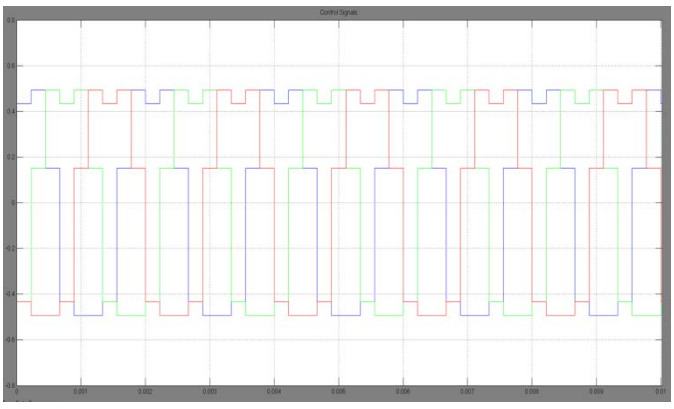

Fig. 8: Control Signals of improved ASVM

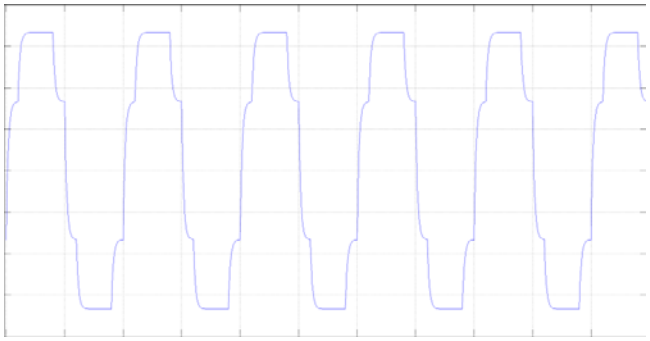

Fig. 9: Sinusoidal PWM

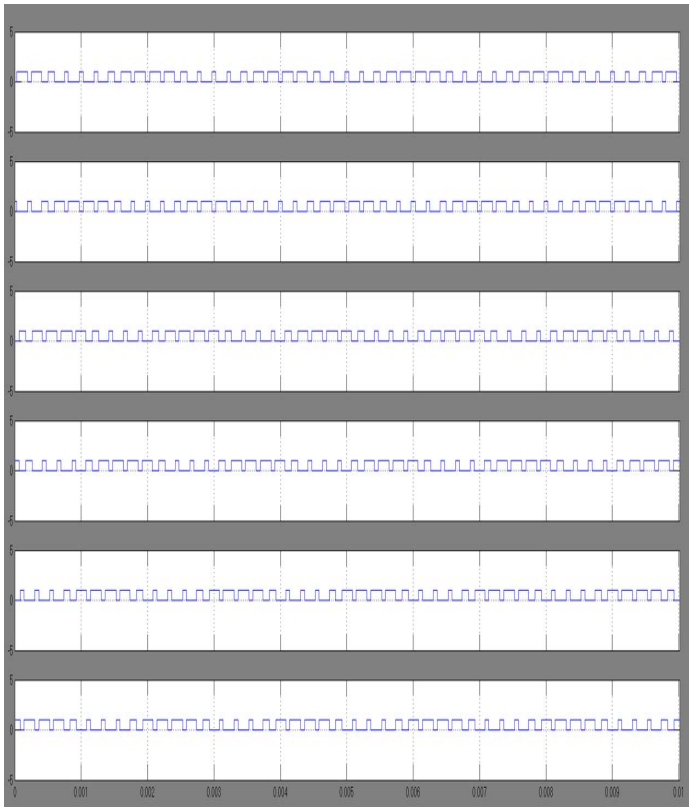

Fig. 10: Gate triggering pulses

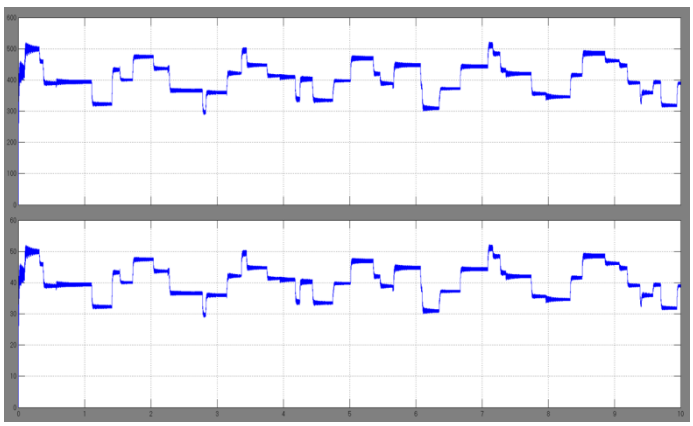

Fig. 11: Improved ASVM

TABLE 2
Summary Of Experimental Results (M=0.9 Or M=0.75)

		M=0.9	M=0.75
SINUSOIDAL PWM	RMS of I_A	22A	20A
	THD of I_A	39.8% (100%)	42.37% (100%)
IMPROVED ASVM	RMS of I_A	5.93A	4.95A
	THD of I_A	10.7% (60%)	14.9% (100%)

7. Conclusion

This paper presented the comparison between the performances of improved asymmetric space vector modulation (ASVM) and sinusoidal pulse width modulation for two level voltage source converters operated with low carrier ratio. By adding two pulses for each phase in one fundamental cycle, the THD of output current can be reduced as much as 50%. The THD can be further reduced by more than 50% if improved ASVM is used together with interleaving in a paralleled VSC system.

The THD reduction depends highly on the modulation index, but improved ASVM always minimize the THD of output current. In addition, it can also reduce the amplitude of circulating current, which can help to reduce the size and weight of inter-phase inductor. Since the additional pulses are added when fundamental voltage crosses zero, the resulted extra power loss is very limited especially if system power factor is high. The benefit of improved ASVM is also demonstrated by inductor weight comparison in different PWM schemes and all of the analyses are verified by experimental results.

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