Design and Implementation of DDR SDRAM Controller using Verilog

Priyanka Bibay[1], Anil Kumar Sahu[2], Vivek Kumar Chandra[3]

[1]Student, M.E. (VLSI Design), CSVTU University, Electronics & Telecommunication Dept., SSCET, Bhilai Chhattisgarh, India
bibay.priyanka@gmail.com

[2]Assistant Professor, Electronics & Telecommunication, SSCET, Bhilai Chhattisgarh, India
anilsahu82@gmail.com

[3]Associate Professor, HOD (EEE), CSIT, Durg Chhattisgarh, India
vivekchandra1@rediffmail.com

Abstract: ***Double Data Rate Synchronous DRAM (DDR SDRAM) has become a mainstream memory of choice in design due to its speed, burst access and pipeline features. The DDR SDRAM is an enhancement to the conventional SDRAM running at bus speed over 75MHz. The DDR SDRAM (referred to as DDR) doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal. The designed DDR Controller supports data width of 64 bits, Burst Length of 4 and CAS (Column Address Strobe) latency of 2. DDR Controller provides a synchronous command interface to the DDR SDRAM Memory along with several control signals. In this paper, the implementation has been done in Verilog HDL by using Xilinx ISE 9.2i and Modelsim 6.4b.***

Keywords: Double Data Rate, Column Address Strobe (CAS), Synchronous Dynamic RAM**.**

1. Introduction

With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. Thus doubling the data transfer rate of the memory device. The DDR is available in a very low cost that's why it is widely used in personal computers where they are basically used to provide the functions of storage and buffers. The DDR SDRAM supports the data widths of 16, 32 and 64 bits. It automatic refresh during the normal and power down modes. The DDR is a complete synchronous implementation of controller. It increases the throughput using command pipelining and bank management. This improvement allows the DDR module to transfer data twice as fast as SDRAM. As an example, instead of a data rate of 133MHz, DDR memory transfers data at 266MHz.DDR modules, like their SDRAM predecessors, arrive in there. Although motherboards designed to implement DDR are similar to those that use SDRAM, they are not backward compatible with motherboards that support SDRAM. You cannot use DDR in earlier SDRAM based motherboards, nor can you use SDRAM on motherboards that are designed for DDR.

A. Random Access Memory

Random access memory (RAM) is the best known form of computer memory. RAM is considered "random access" because you can access any memory cell directly if you know the row and column that intersect at that cell. RAM data, on the other hand, can be accessed in any order. All the data that the PC uses and works with during operation are stored here. Data are stored on drives, typically the hard drives. However, for the CPU to work with those data, they must be read into the working memory storage (RAM).

B. Types of Random Access Memory

i. Static Random Access Memory

Static Random Access Memory uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes four or six transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes up a lot more space on a chip than a dynamic memory cell. Therefore, you get less memory per chip. Static Random Access Memory uses multiple transistors, typically four to six, for each memory cell but doesn't have a capacitor in each cell. It is used primarily for cache. So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. So, static RAM is used to create the CPU's speed-sensitive cache, while dynamic RAM forms the larger system RAM space.

ii. Dynamic Random Access Memory

Dynamic Random Access Memory has memory cells with a paired transistor and capacitor requiring constant refreshing. DRAM works by sending a charge through the

appropriate column (CAS) to activate the transistor at each bit in the column. When writing the row lines contain the state the capacitor should take on. When reading the sense amplifier determines the level of charge in the capacitor. If it is more than 50 percent, it reads it as a 1 otherwise it reads it as a 0.

A memory chip rating of 70ns means that it takes 70 nanoseconds to completely read and recharge each cell. It is one of the most common types of computer memory (RAM). It can only hold data for a short period of time and must be refreshed periodically. DRAMs are measured by storage capability and access time. Storage is rated in megabytes (8 MB, 16 MB, etc). Access time is rated in nanoseconds (60ns, 70ns, 80ns, etc) and represents the amount of time to save or return information. With a 60ns DRAM, it would require 60 billionths of a second to save or return information. The lower the speed, the faster the memory operates. DRAM chips require two CPU wait states for each execution. Can only execute either a read or write operation at one time. The capacitor in a dynamic RAM memory cell is like a leaky bucket. It needs to be refreshed periodically or it will discharge to 0. This refresh operation is where dynamic RAM gets its name.

Memory is made up of bits arranged in a two-dimensional grid. In which memory cells are fetched onto a silicon wafer in an array of columns (bit lines) and rows (word lines). The intersection of a bit line and word line constitutes the address of the memory cell. Memory cells alone would be worthless without some way to get information in and out of them. So the memory cells have a whole support infrastructure of other specialized circuits. Identifying each row and column (row address select and column address select) Keeping track of the refresh sequence (counter) Reading and restoring the signal from a cell (sense amplifier) Telling a cell whether it should take a charge or not (write enable) Other functions of the memory controller include a series of tasks that include identifying the type, speed and amount of memory an checking for errors. The traditional RAM type is DRAM (dynamic RAM). The other type is SRAM (static RAM). SRAM continues to remember its content, while DRAM must be refreshed every few milliseconds.

iii. Double Data Rate Synchronous Dynamic Random Access Memory

Double Data Rate Synchronous Dynamic Random Access Memory is the original form of DDR SDRAM. It is just like SDRAM except that is has higher bandwidth, meaning greater speed. Maximum transfer rate to L2 cache is approximately 1,064 MBps (for DDR SDRAM 133 MHZ). DDR RAM is clock doubled version of SDRAM, which is replacing SDRAM during 2001- 2002. It allows transactions on both the rising and falling edges of the clock cycle. It has a bus clock speed of 100MHz and will yield an effective data transfer rate of 200MHz. DDR come in PC 1600, PC 2100, PC 2700 and PC 3200 DIMMs. A PC 1600 DIMM is made up of PC 200 DDR chips, while a PC 2100 DIMM is made up of PC 266 chips. Go for PC2700 DDR. It is about the cost of PC2100 memory and will give you better performance. DDR memory comes in CAS 2 and CAS 2.5 ratings, with CAS costing more and performing better.

This paper is organized as follows. In Section 2, Block diagram of DDR controller will be described. The architecture of DDR controller will be described in Section 3. In Section 4, different functional blocks will be explained. Finally the Result and Conclusion will be given in Section 5 and Section 6 respectively.

2. DDR controller Block Diagram

Figure 1 shows the different blocks in top level reference design. The user interface module contains the I/O registers to latch system signals coming into the FPGA. The DDR controller module contains the DDR SDRAM controller, including I / Os to interface with the DDR SDRAM.

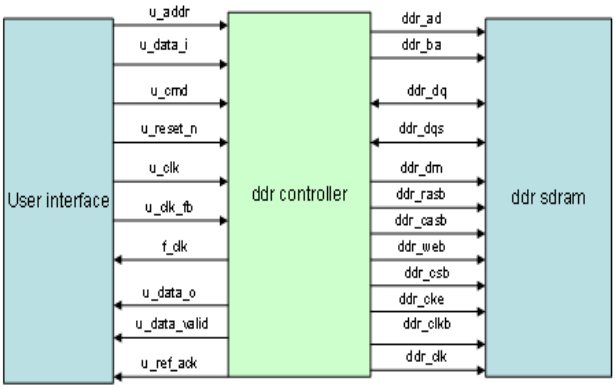

Figure 1: Top Level block diagram

3. DDR Controller Architecture

The DDR Controller mainly consists of four functional blocks:

1. Address Latch
2. Data Path
3. Controller
4. Counter

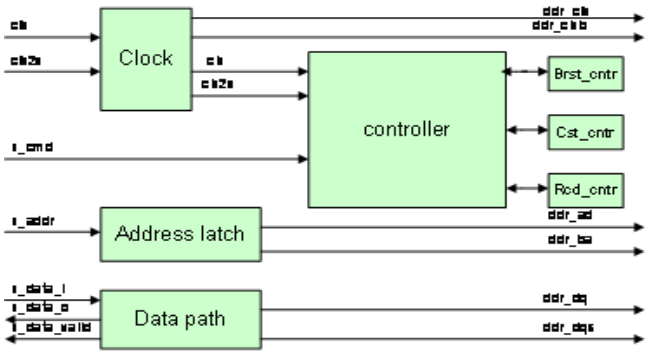

Figure 2: DDR Controller Architecture

4. Different Functional Blocks

4.1 Address Latch

The basic function of address latch module is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

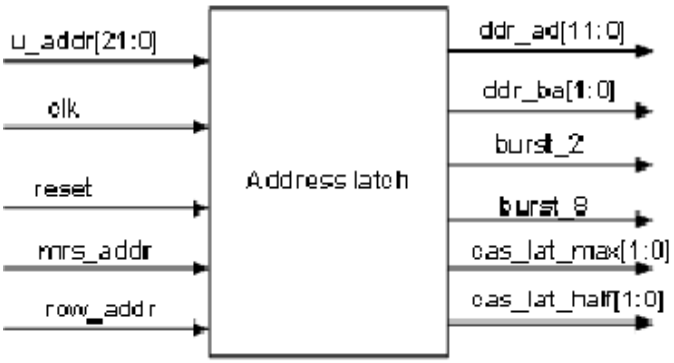

Figure 3: Address Latch Module

4.2 Data Path

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path.

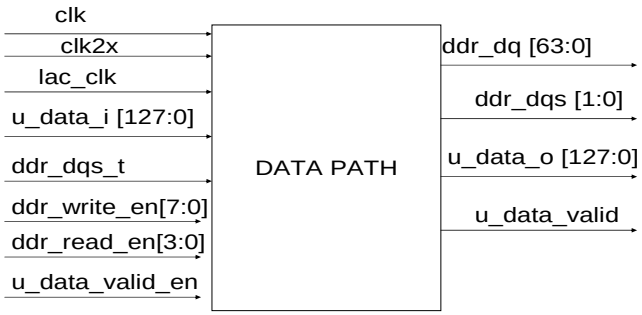

Figure 4: Data Path Module

Data path module handles all the data generation and sampling task of DDR controller. For Read access, data is sampled by data path. Data is then synchronized with the internal clock and transferred to the user interface one-word per clock cycle as normal data rate. For Write access, data is received from the user interface at the normal one word per clock data rate. The DDR controller's data path then resynchronized the data and transfers them using the double data rate.

4.3 Controller

The controller consists of a state machine which performs DDR SDRAM read and write accesses based on user interface request. The controller consists of a high performance timing & control state machine that observes all timing requirements and issues the commands to the memory devices at the shorted time possible. The pin diagram of controller is shown in figure 5:

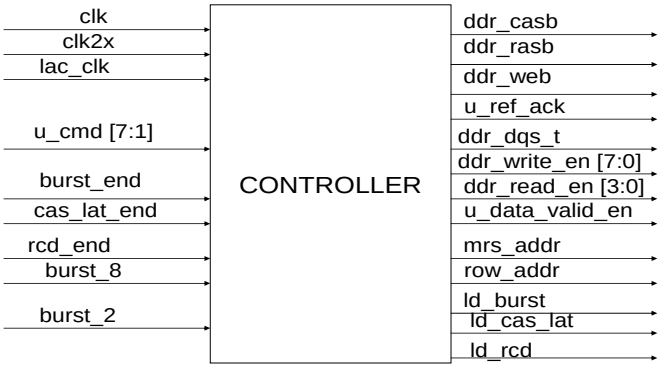

Figure 5: Controller Module

The DDR controller consists of a high performance memory controller for system requiring access to external devices with lowest latency and highest throughput. The controller accepts and decodes user interface commands and generates read, write, refresh commands. It also generates signals for other modules. The memory is initialised and powered up using a defined process. The controller state machine handles the initialization process upon power up.

4.4 Controller state machine diagram

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank is pre charged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.

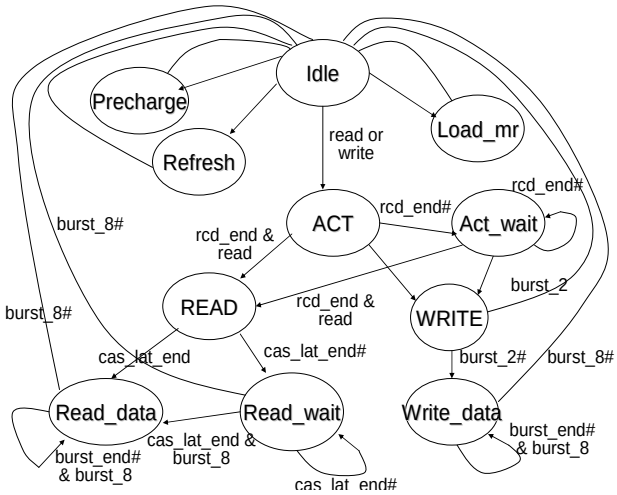

Figure 6: controller state machine diagram

The controller next state could be PRECHARGE, LOAD_MR, REFRESH or ACT, depending upon the required command. The ACT command is used to open a row in a bank before starting any read or write operation. The controller state machine diagram is shown in figure 6.

4.4 Counter

The task of Burst Count is to count when there are consecutive READ and WRITE operations. While doing consecutive READ and WRITE operations, the Burst_count value determines when the next READ and WRITE command should be issued.

5. Results

Figure 7 shows the RTL schematic of designed DDR SDRAM controller.

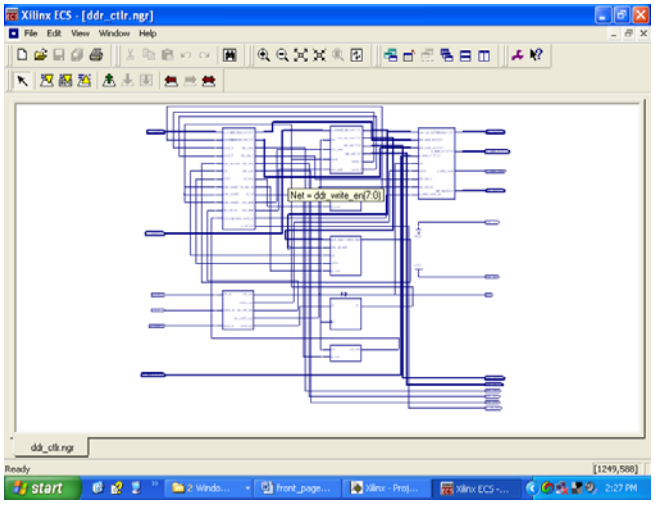

Figure 7: RTL schematic of DDR Controller

The following figures are the simulation result of controller, controller Write cycle and controller Read cycle obtained by using Modelsim 6.4b.

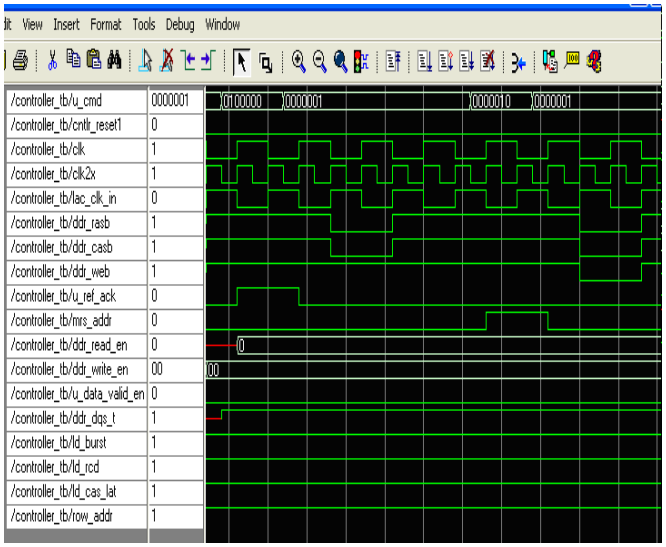

Figure 8: Simulation waveform for Controller

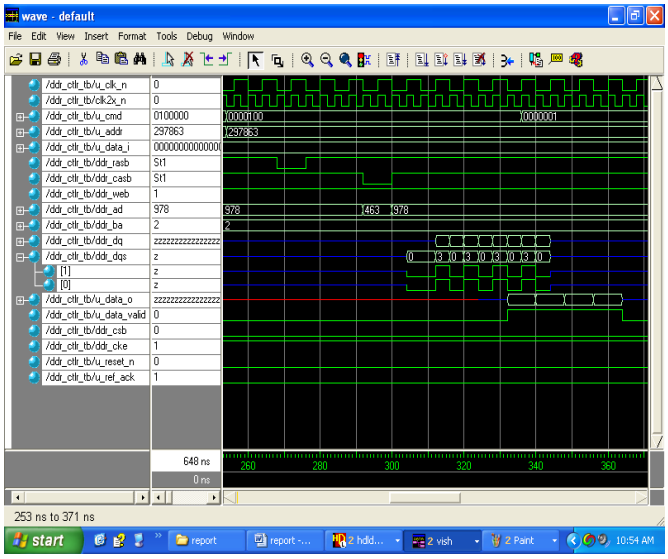

Figure 9: Simulation waveform for Controller Read Cycle

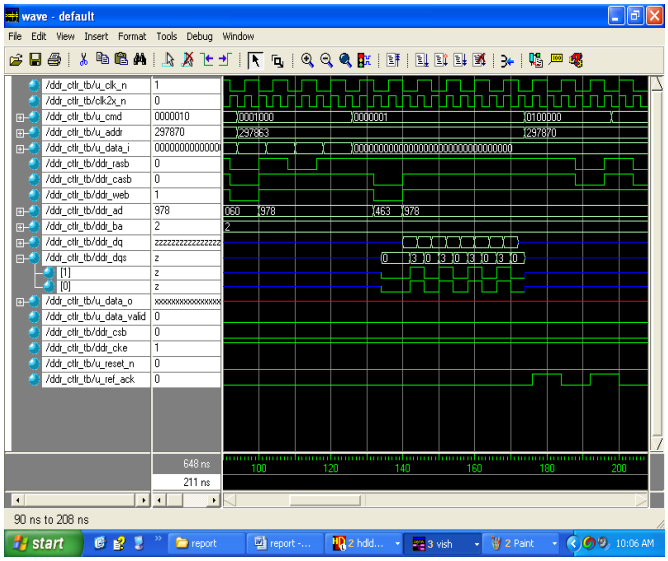

Figure 9: Simulation waveform for Controller Write Cycle

6. Conclusion

In this paper an efficient fully functional DDR SDRAM controller is designed. The controller generates different types of timing and control signals, which synchronises the timing and control the flow of operation. The memory system operates at double the frequency of processor, without affecting the performance. Thus we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay.

References

[1] Micron Technology Inc. Double Data Rate (DDR) SDRAM, Datasheet, 1999
[2] Synthesizable DDR SDRAM controller, Application note, 2002. (Xilinx Inc., XAPP200)
[3] Using the vertex select I/O Resource, Application note, 1999. (Xilinx Inc., XAPP133)
[4] Using Delay Locked Loops in Spartans-II FPGAs. (Xilinx Inc., XAPP174)
[5] JEDEC, Solid State Technology Association. DDR2, SDRAM Specification.
[6] LatticeSC/M DDR/DDR2 SDRAM Memory interface User'sGuide, TechnicalNoteTN1099, July2008
[7] J.Bhaskar "A verilog HDL primer- 2nd edition"
[8] John Wakerly "Digital system design – 8th edition."
[9] Burchardt, A., Hekstra-Nowacka, E., and Chauhan, A., "A Real-time Streaming Memory Controller", Design,
[10] Automation and Test in Europe 2005 Proceedings, 2005, vol.3, pp. 20-25
[11] Heithecker, S and Ernst, R., "Traffic Shaping for An FPGA Based SDRAM Controller with Complex QoS Requirements", Design Automation Conference 2005, June 2005, pp. 575-578.

Author Profile

Priyanka Bibay has received her B.E. degree in Electronics & Telecommunication Engineering from Chhattisgarh Swami Vivekananda Technical University, Bhilai, India, in 2005. She is pursuing her M.E. (Specialization in VLSI Design) from SSCET, Durg, with the same CSVTU University, Bhilai, India from 2010-2012.