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Theoretical Investigations of Insulator and Semiconductor Interface

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Abstract: ***Metal–Insulator–Semiconductor (MIS) capacitors are widely used for investigating semiconductor surface properties and insulator characteristics. This work presents a comprehensive overview of MIS capacitance theory, ideal and non-ideal MIS capacitor behaviour, and techniques for determining interface state density. The study discusses capacitance-voltage (C-V) characteristics under accumulation, depletion, and inversion conditions, as well as the influence of fixed and mobile charges, work-function differences, and interface states. Various methods for interface state density determination, including Terman's method, Berglund's low-frequency method, quasi-static techniques, Q-V analysis, and conductance methods, are reviewed and compared. The analysis highlights the suitability of high-frequency C-V measurements for evaluating interface characteristics in MIS structures such as Au/CdTe/MCT systems.***

Keywords: MIS Capacitor, Capacitance-Voltage (C-V) Characteristics, Interface State Density (Dit), Semiconductor Interfaces, Terman Method, Conductance Method, Surface States

1. Introduction

The electrical characteristics of a material are crucial, since they determine the potential of a material for application in modern electronic devices. These characteristics of the material are mainly dependent on material structure and process technology. The electrical characterisation includes the electrical (bulk) properties of the deposited thin films and the interface characteristics of the insulator- semiconductor interface and is considered to be one of the potential areas of interest from device point of view. The electrical behaviour of thin films as a function of deposition techniques, conditions and annealing is evaluated in terms of low field resistivity, breakdown field strength, dielectric constant with its dependence on frequency and de insulator leakage current. For photodetector applications, stoichiometric films of high resistivity, low fixed charges and wide gap materials are required. To understand the MIS structure of Au/CdTe/MCT system from its electrical characteristics, we take the Si/SiO_2 MOS structure (1)as an analogy, since this system is known to be one of the best understood MIS structures and has been investigated in great depth, with a lot of information and data available, along with the physical interpretations. In our case the various characterisations and calculations have been made on similar lines as for the Si/SiO_2 system, with relevant modifications made for various parameters in the equations and formulae established for the Si/SiO_2 system. We begin with an overview of MIS capacitance theory and various techniques for determination of interface state parameters with their advantages and disadvantages. This process enabled us to identify the techniques most suitable for analysis of MIS structures investigation.

The Ideal MIS Capacitor

The most important tool to study the semiconductor surfaces and insulator properties in the MIS (Metal Insulator-Semiconductor) capacitor is the C- V characterisation. Whenever charges are separated by a distance, there is a capacitance related to the charge system, e.g. for an MIS capacitor, charges are separated by the insulator. The gate charges are mirrored by several types of charges in the semiconductor. In understanding and deriving the capacitance of the system, we make use of the equation

$$C = \Delta Q_g / \Delta AV_g \quad (1)$$

i.e. capacitance is the ratio of the change in gate charge to the change in the gate voltage. This is referred to as the "incremental" or "differential" capacitance. Measurements of C-V characteristics of MIS capacitors are key to the analysis and monitoring of a device manufacturing process. The most important feature of this measurement is the wealth of information it provides as compared to the simplicity of its execution and analysis. It consists of a semiconductor substrate on which a thin insulator layer is deposited. The metal gates are deposited on top of the insulator layer. The back contact of the structure is provided by a metal film.

Energy Band Diagram for the Ideal Case

Difference, no insulator charge present, and no voltage applied, the energy bands would be perfectly flat and the concentration of holes and electrons does not vary throughout the semiconductor. This condition is termed as the "flat-band condition". The energy band diagram of a typical MIS structure is shown in Figure.1

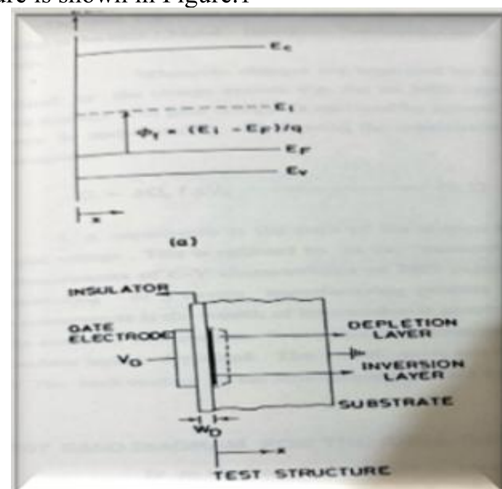

Figure 1: Energy Band Diagram of an MIS Structure for the ideal case exhibiting Flat-band Conditions

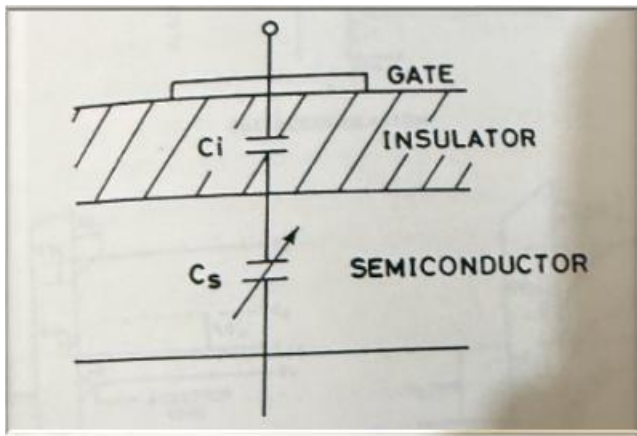

Figure 2: Equivalent Circuit of MIS Capacitors. The Capacitors Labelled C_S is Bias Dependent

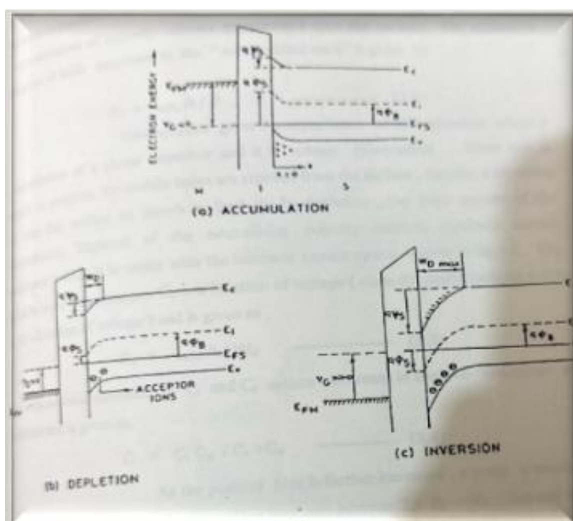

Figure 3: Energy Band Diagram of an MIS system for P-Type Semiconductor

When voltage is applied to the gate with the substrate at ground, there will be bending of bands, dependent on both the polarity of the voltage and the type (p or n) of the substrate. In the case of a p-type substrate, a negative bias will attract mobile holes to the surface, making the material effectively more heavily doped p-type in this region. This is defined as "accumulation condition" as shown in fig 3a. In the accumulation condition, a high concentration of majority carriers accumulates near the surface. The equivalent capacitance of the MIS structure in the "accumulated state" is given by

$$C_i = X_0 X_X A / d \quad (2)$$

This equation gives the capacitance of the MIS structure, which is the capacitance of a planar capacitor, surface, forming a depletion layer near the surface, as shown in Fig. 3b.In depletion, the ionic centres of the semiconductor, depleted of the neutralising majority carriers represent certain capacitance, which is in series with the insulator capacitance as shown in fig.2. The depletion layer capacitance, C_d is a function of voltage (since the depletion layer width W_d is a function of voltage) and is given as,

$$C_d = X_0 X_X A / W_d \quad (3)$$

The total series combination of C_i and C_d causes a decrease in the total capacitance in depletion and is given as,

$$C = C_i C_d / C_i + C_d) \quad (4)$$

As the positive bias is further increased, a point is reached when the insulator/Semiconductor surface becomes intrinsic, i.e. $E_f = E_i$. Beyond this point, a special condition is reached when the amount of band bending us becomes:

$$\Psi_s = (E_i \text{ at the surface} - E_i \text{ at the bulk})/ q = 2\Phi_B \quad (5)$$

This is the inversion condition shown in fig 3c. Any further increase in gate voltage does not increase the band bending significantly because any further increase in the band bending past $2\Phi_B$ would increase the number of inversion layer carriers exponentially, and the increased gate charge due to the additional bias is easily balanced by these charges without any increase in the depletion region width.

At inversion, the depletion region reaches its maximum width, and the capacitance reaches a minimum, labelled.

$$C_{min} = C_i C_{min} / C_i + C_{min} \quad (6)$$

In case of n-type semiconductor a similar process takes place but with a reverse polarity of voltage. The accumulation layer charge comprises of electrons, while the inversion layer charge comprises of mobile holes. It is at inversion, that we must understand how charge densities respond to the changes in gate voltage. Taking the case of p-type MIS capacitor, in depletion, when the gate voltage is increased slightly, only a small amount of additional depletion occurs at the edges of the depletion region. Once the inversion layer forms, then increases in gate charge are balanced by the increases in electron concentration at the surface, if the change in gate voltage is slow enough for the electrons to respond. These electrons are attracted from the bulk and must make the transition through the depletion layer. It is the lifetime of these minority carriers which determines the frequency at which they respond to the signal. The gate voltage variation is incrementally small (a small signal ac voltage) and is superimposed on the dc bias. In response to changes in gate voltage, the surface depletes slightly or accumulates slightly. At low frequencies the mobile charge picture is similar to accumulation except for the presence of minority carriers and the total capacitance reverts to the insulator capacitance. At a high frequency, since the electrons cannot respond to the gate signal variations, the changes in the gate charge are balanced by the changes in the depleted ionic charge i.e. increasing and decreasing the maximum depletion width. The capacitance in this case is simply C_{min} for any value of gate voltage beyond the onset of inversion. A typical curve showing the capacitance-voltage variation is represented in fig. 4.

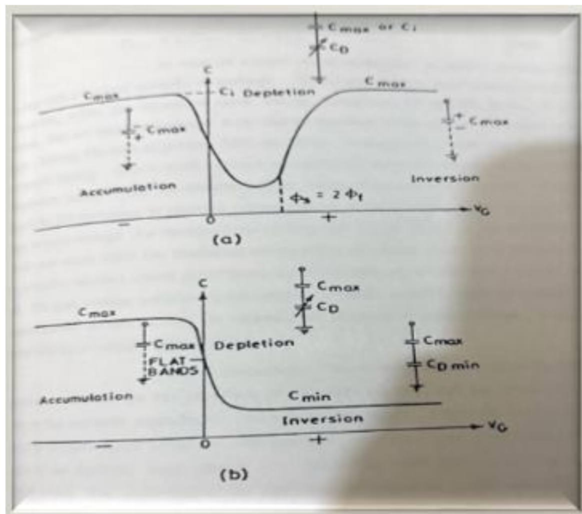

Figure 4: Typical (a) Low Frequency (b) High Frequency C-V Curves for a P-Type MIS Capacitor.

Non-Ideal MIS Capacitor:
In practical MIS capacitor, there are several non-ideal effects perturbing the ideal case, viz. different types of mobile and fixed charges and metal- semiconductor work function difference (Φ_m) causing a parallel shift (2) in the C-V characteristics. Various non- ideal effects are briefly discussed below.

Metal - Semiconductor Work Function Difference(Φ_{ms}): We know that the work function is the energy required to bring an electron from the Fermi level to the vacuum level. In our Au-MCT-CdTe structures the gold work function and mercury cadmium telluride work functions therefore, the work function difference will not be zero voltage VFB would need to be applied to bring the system to the flatband condition. VFB, is called the flatband voltage. are not equal, and an amount of external voltage V_{FB} would need to be applied to bring the system to the flatband condition. V_{FB} is called the flatband Voltage.

Fixed Insulator Charge (Q_{ss}): Most of the insulators are characterised by the presence of some charge, either distributed in the bulk of the insulator or located close to the interface. In device grade insulator films, the charge is mostly fixed and located at the semiconductor -insulator interface. The existence of this fixed positive charge at the semiconductor -insulator interface, with surface charge density Q_{ss} will result in additional band bending and an external voltage needs to be applied to restore the flatband condition. Q_{ss} is independent of the insulator thickness, doping type or doping concentration and arises as a result of an abrupt discontinuity of the material and lattice mismatch at the interface. In order to obtain a true value of Q_{ss} from the C-V curves, special care is not taken to apply gate voltages, which could lead to charge injection into the dielectric and mask the actual fixed charge existing. In either case, a parallel shift is observed in the C-V curve w.r.t ideal C-V curve by an amount ΔV_{FB}.

Mobile Charge (Q_m).: Mobile charges are mainly ionised alkali atoms e.g., Na+, K+, and Lit. The origin of such ions is mainly due to the contamination during fabrication processing, such as gate or contact metallization and general handling of the substrate during the cleaning process etc. These ions move around inside the insulator instability in the threshold voltage of the device. The flatband shift (3) is caused by an arbitrary charge density distribution.

Interface States
The interface states arise mostly as a result of an abrupt discontinuation of the material. These are electronic states distributed across the semiconductor band gap and can act as traps or recombination centres for charge carriers, resulting in electronic charge instabilities at the interface. The origin of interface states could be dangling bonds, strained bonds or impurity effects. The interface states are quantised in terms of interface state density, D_{it}. The interface states are chargeable surface states, unlike $Q_{ss,}$ and the interface traps can be charged or discharged through the filling and emptying processes as a result of changes in band bending. Thus, when a voltage is applied, the interface trap levels move up or down with the valence and conduction bands, while the Fermi level remains fixed. A change of charge in the interface trap occurs when the interface trap level crosses the Fermi level. The interface states give rise to various effects depending on the frequency of measurement. This property is made use of in the determination of the interface state parameters. If the frequency of measurement is very much higher than the reciprocal of the time constant ($1/t_{it}$) of the states, the charge in these states will essentially behave like a fixed charge and hence will lead to a parallel shift in the C-V characteristic. The magnitude of the shift is proportional to the magnitude of the charge residing in the states. At a frequency of measurement much lower than. ($1/t_{it}$) states are in equilibrium with the voltage ramp and have only a capacitance associated with them, but they do not contribute to any loss. However, when frequency of measurements equals ($1/t_{it}$)a capacitance and conductance are associated with them. The equivalent circuit incorporating the effect of the interface are the insulator capacitance and taps (4) is shown in fig.5 C_i and C_D semiconductor depletion -layer capacitance respectively C_s and R_s capacitance and resistance associated with the interface traps and are functions of surface potential. The product C_sR_s is defined as the interface trap response time, which determines the frequency behaviour of the interface traps. The parallel branch of the equivalent circuit shown in Fig. .5b on L.H.S can be converted into a frequency - dependent capacitance C_p in parallel with a frequency - dependent conductance G_p as shown in Fig.5b on R.H.S. Thus, the interface states give rise to different nonidealities which parameter. are the are made use of for the determination of the interface state

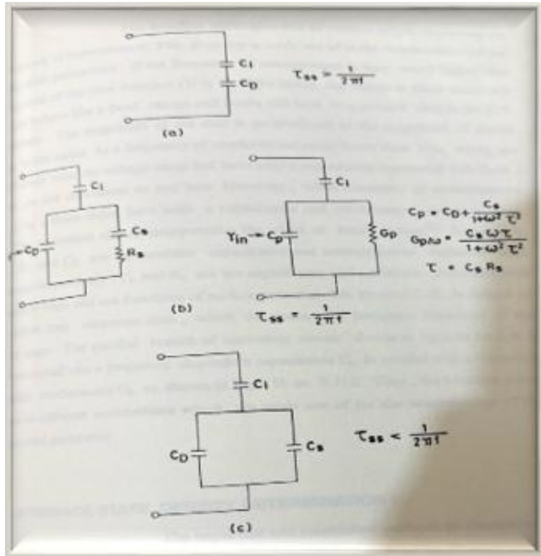

Figure 5: Equivalent Circuits of an MIS Capacitor at different Frequencies incorporating the Effect of interface Trap

Interface State Density Determination:

The important and established methods to determine the characteristics of the interface states, which measure charge in quasi-equilibrium with the applied electric field, are briefly described in this section with their relative merits and demerits. Suitability of these methods to determine the interface state parameter is described at the end. For a quantitative treatment of a C-V curve, it is simpler to choose Ψ_s rather than the gate bias V_g as the independent variable, where (x) is the potential at any point x in the depletion region with respect to its value in the bulk. Ψ(x) is the potential defined by the equation

$$q\Phi(x) = E_f - E_i\,(X) \qquad (7)$$

and Ψ(x) is the band bending given by,

$$\Psi\,(x) = \Phi(x) - \Phi(B) \qquad (8)$$

Deep in the bulk semiconductor (x + - ∞) ,Φ(x)is called the bulk potential Φ(B) and at the semiconductor surface (x = 0) , Φ(x) is called surface potential, so that the interface trap levels located opposite to the Fermi level are at energy Φ_s above the intrinsic level at the semiconductor surface.

Interface Trap Capacitance at Low and High Frequency:

Capacitance measurements indicate the presence of interface traps by way of stretching out of the C-V curve along the gate bias axis, and the stretch out is a measure of the contribution of interface traps to the capacitance. Because interface trap occupancy varies with the gate bias, in an MIS capacitor with interface traps, a change in interface trap charge density, ΔQit it also occurs with any change in band bending. The charge balance satisfies,

$$\Delta Q_G + \Delta Q_{it} + \Delta Q_S = 0 \qquad (9)$$

Consequently, to drive the MIS capacitor from accumulation to inversion requires a larger range of gate charge variation and the C-V curve is stretched out along the gate bias axis. For a slow, infinitesimal change in gate bias dV_G, a change in band bending $d\Psi_S$ is given by the following equation,

$$C_i\, dV_G = [C_i + C_{it}(\Psi_s) + C_s(\Psi_s)\,d\Psi_s \qquad (10)$$

Where $C_{it}(\Psi_s)$,is the capacitance due to interface trap density, and

$$C_{it}(\Psi_s) = - dQ_{it}/d\Psi_s \quad (11)$$

$C_s(\Psi_s)$, is the surface capacitance, and

$$C_s(\Psi_s) = - dQ_s/d\Psi_s \qquad (12)$$

From equation (10) we see that a given gate bias variation dV_G leads to a smaller variation in band bending when C_{it} is present. Equation (11) leads to a low frequency capacitance of the MIS capacitor given as:

$$C_{LF} = (C_S + C_{it})C_i/C_i + C_S + C_{it} \quad (13)$$

$$\text{Or } 1/C_{LF} = 1/C_i + 1/(C_s + C_{it} \qquad (14)$$

i.e. in addition to stretch out, measured capacitance is increased as a result of Cit. The equivalent circuit corresponding to equation (13) . The capacitance given by equation (9) corresponds to a change in the charge dQ_r in response to very slow change in gate bias. Only those interface traps that can capture electrons within the period of the ac gate voltage will respond. Consequently, C_i, become C_{it} (ω) and for ω→Q , C(Ψ)→0. Thus at high frequencies, stretchout is the only effect of interface traps. these are: There are several approaches to extracting Dit from the capacitance

(a) Measurement of strechout of the high frequency C-V cuve by comparison with a theoretical curve.

(b) Measurement of Cit by subtraction of calculated capacitance from a measured low frequency C-V curve.

(c) Comparison of both high and low frequency C-V curves with no need for a calculated curve.

High Frequency Capacitance or Terman's Method:

Terman's method (6)is the oldest method to determine interface state densities. In this method, capacitance is measured as a function of gate bias with frequency fixed at a high enough value so that the interface traps do not respond. At high frequencies, although the surface state charge exchange cannot follow the applied ac signal, it does follow very slow changes in gate bias as the MIS capacitor is swept from accumulation to inversion so that the interface trap charge contributes no capacitance to the high frequency C-V curve, but makes its presence felt by causing the C-V curve to stretch out along the gate bias unlike the other charges which cause a parallel shift in the C-V curve. The interface traps distributed uniformly throughout the semiconductor band gap produce a fairly smoothly distorted C-V curve. At high frequencies C_{it} (ω)=0, because ω is too large for any ac response of interface traps. Hence, high frequency capacitance is given by

$C_{HF} = C_s C_i / C_s + C_i$ (15)

The circuit capacitance corresponding to C_{HF} is shown in Fig.6b. The high-frequency capacitance of an MIS capacitor will be the same as that of an ideal one without interface traps, provided that C_s is the same. However, C_s varies with band bending Ψ_s; the measured C_{HF} will be the same as the ideal one if the band bending is the same.

In Terman's method of measuring interface state density D_{it} , a Ψ_s versus V_G curve is constructed for the capacitor with the interface traps. It is this curve that contains information about D_{it} in high-frequency C-V measurements. A theoretical plot of C_{HF} VS. $\Psi_s$is compared with the measured plot of C_{HF} VS.

V_G. Comparison of these two plots determines Ψ_s Vs. V_G. Interface traps stretch the Ψ_s vs Vs. V_G curve along the bias axis. The amount of stretch out measured by the derivative $d\Psi_s/dV_G$ is obtained by graphical or numerical differentiation of the Ψ_sVs. V_G curve $C_{it}(\Psi_s)$ can be determined as,

$$C_{it}(\Psi_s) = C_i((d\Psi_s/dV_G)^{-1} - 1) - C_S(\Psi_s) \quad (16)$$

Once C_{it} is found, D_{it} is inferred using C_{it} is found, D_{it} is inferred

$$C_{it} = qD_{it} \quad (17)$$

$$D_{it} = 1/q\ (C_i((d\Psi_s/dV_G)^{-1} - 1) - C_S(\Psi_s))$$

$$D_{it} = C_i/q\ (d(\Delta V_G)/d\Psi_s) \quad (18)$$

Where $\Delta V_G = V_G - V_G$ (ideal) is the voltage shift of the experimental from the ideal curve, with V_G being the experimental gate voltage.

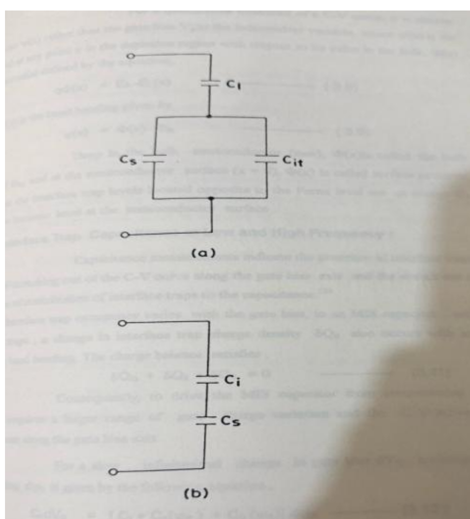

Figure 6: (a) Low and (b) High Frequency Equivalent Circuit of MIS Capacitor

Low Frequency Capacitance Method:

The low frequency method to calculate the interface trap density was developed by Berglund (7) and makes use of a C-V curve measured at a frequency low enough so that the interface trap response is immediate to the ac gate voltage resulting in additional capacitance C_{it} i.e. the differential capacitance is measured at such a frequency that the charge exchange between the surface state and the conduction band is in equilibrium measured curve will be stretched out along the axis. The equivalent circuit in Fig. 6a shows that C_{it} can be extracted from the measured low-frequency capacitance C_{LF} if C_S and C_i are known.

$$C_{it} = (1/C_{LF} - 1/C_i)^{-1} - C_S \quad (19)$$

Where C_i can be measured in strong accumulation. To obtain $C_S(V_G)$, $C_S(\Psi_s)$ is calculated and related to $C_S(V_G)$. A derivative could be taken and used to obtain $C_{it}(\Psi_s)$ just as with the high-frequency C-V curve. In both the high frequency and low frequency methods, the theoretical calculation of $C_S(\Psi_s)$ is necessary. Combined High and Low Frequency Capacitance Method: This method eliminates the need for a theoretical computation of C_S. Here, we use Équations (16) and (19), so that C_{it} is given as.

$$C_{it} = (1/C_{LF} - 1/C_i)^{-1} - (1/C_{HF} - 1/C_i)^{-1} \quad (20)$$

Thus, C_{it} is obtained directly from the measured C-V curves, without the uncertainty introduced by a theoretical C_S. The methods that eliminate the need to measure the capacitance at very low frequencies are briefly discussed below:

Kuhn's Quasi - Static Technique:

A variation of Berglund's low frequency technique described above was suggested by Kuhn (8). This technique called Kuhn's Quasi-Static Technique can be used to determine the low frequency capacitance from the displacement current through the MIS capacitor, In this method, a slowly varying ramp is applied to the MIS capacitor and displacement current is given by,

$$i. = dQ/dt = dQ/dV.dV/dt = C_{LF}\ dV/dt \quad (21)$$

Where dQ is the change in charge in time dt For a constant (dV \dt), the current 'i.' is proportional to the low frequency capacitance C_{LF}

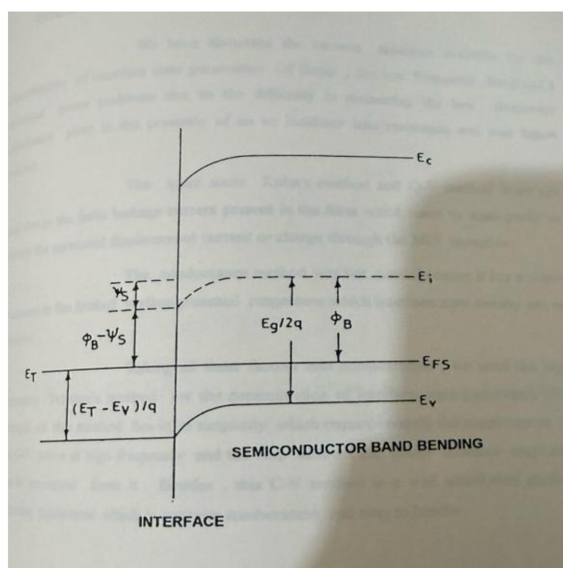

Figure 7: Position of the fermi Level at semiconductor Surface related to Band bending

Q-V Method:

Instead of measuring the charging current as done in the quasi- static method of Kuhn, in Q-V method the charge is measured directly as a function of gate voltage. The method requires knowledge of neither the doping profile, nor the insulator charge density. It is also less convenient than the low-frequency C-V method and has the potential advantage of greater accuracy.

High Frequency Temperature Method:

This method is based on the temperature dependence of the Fermi level (9). The temperature of the capacitor is varied to change the position of the Fermi level. As a result, C-V curve undergoes a shift and the interface state density can be determined. However, only small portion of the band gap can be scanned within reasonable temperature ranges. The temperature ranges are also severely limited by the stability of the insulator and the semiconductor at higher temperature regions.

Conductance Method

In this method, interface trap(10) levels are detected through the loss resulting from the changes in their occupancy

produced by small variations of gate voltage. A small ac voltage is applied to the gate of an MIS capacitor alternately or away from the Fermi level. The majority carriers are captured or emitted, changing the occupancy of interface trap levels in a small energy interval, a few kT/q wide, centred about the Fermi level. The phase shift of the capture and emission process relative to the applied ac voltage causes an energy loss observed at all frequencies except the very lowest (to which interface traps immediately respond) and the very highest (to which no interface trap response occurs). This energy loss is measured as an equivalent parallel conductance. G_P.The technique consists of measuring the admittance of the MIS capacitor at different biases as a function of the applied frequency and extracting the values for equivalent parallel conductance GP from the measured data. Then (G_P/ω) is plotted as a function of ω(angular frequency of measurement) for different bias values. This plot yields the values for surface state density and time constant Interface trap levels are found to be closely spaced in energy and distributed throughout the entire semiconductor band gap. To derive the relation between the measured admittance of MIS capacitor and interface trap properties, the loss associated with a single level interface state i.e. with the interface traps all with the same energy is first derived and then extended to the realistic case of a distribution of interface trap levels. Under small signal ac excitation, interface trap occupancy is perturbed only slightly from its equilibrium value. In equilibrium, the probability that an interface trap level is occupied is given by $f(E_T)$. The capture rate of electron (taken as majority carriers) by a single level interface state is,

$$R_n(t)=N_s.\,C_n\,[1-f(t)]\,n_s(t) \quad (22)$$

and the emission rate of electrons by a single-level interface state is:

$$G_n(t) = N_s.enf(t) \quad (23)$$

The net current out of these states or net electron flow into the states is given by, is

$$I_s(t) = qN_S\,C_n\,[1-f(t)]\,n_s(t) - N_s.e_nf(t) \quad (24)$$

Under small signal approximation, it can be shown that this equation leads to a surface state admittance of.

$$Y_s = j\omega\,(q^2/kT)\,[N_S,\,f_o\,(1-f_o)/(1+j_o\omega f_o)/C_n\,n_{so}] \quad (25)$$

Separating equation (25) into real and imaginary parts leads to an equivalent parallel capacitance of and an equivalent parallel conductance of

$$C_{ps} = C_{ss}/1+\omega^2\Gamma^2) \quad (26)$$

$$G_{PS} = C_{SS}\omega^2\Gamma_s\,(1+\omega^2\Gamma_s^2) \quad (27)$$

$C_{SS} = q^2N_Sf_o\,(1-f_o)\,/\,C_n\,n_{s0}$

And $\Gamma_s = f_o/\,C_n\,n_{so}$

The interface states are comprised of many levels so closely spaced in energy that they cannot be distinguished as separate levels. They appear as a continuum over the band gap. Lehovec (11) was the first to calculate the admittance of the continuum by integrating equation over the entire band gap. The surface state admittance can be represented as.

$$Yss=qNss\,/\omega\Gamma_{ss}\,(In\,(\,I+\,\omega^2\Gamma_{ss}^2\,)+j(\,(qN_{SS})/\Gamma_{SS}\arctan(\,\omega\Gamma_{SS}) \quad (28)$$

Where $\Gamma_{SS} = 1/\,C_nn_{so}$

Concentrating on the real part of the equation, we have

$$G_p = (qN\,ss\,/2\omega\Gamma_{SS})\ln\,(1+\omega\Gamma_{SS}^2) \quad (29)$$

For distribution of interface trap levels over the energy interval a few kT wide about the Fermi level. for an semiconductor band gap, transitions occur between the majority carrier band and the interface trap levels in an Considering the interface trap levels at a particular energy in the band gap appropriate band bending, the Fermi level will lie at these interface trap energy levels. For this band bending a particular majority carrier density prevails at the semiconductor surface that determines the capture rate of the chosen trap levels. If the applied small signal frequency corresponds to this capture rate, a peak loss will occur. The loss is reduced at higher or lower frequencies. Thus, a peak in the loss values as a function of frequency occurs. Each interface trap level in the energy interval a few kT on its wide about the Fermi level contributes a different energy loss depending on the distance in energy from the Fermi level. As a result, each interface trap level in this energy interval has a different time constant. A single-level interface state gives rise to symmetrical G_p/ω Vs. ω curves with a maximum occurring at $\omega\Gamma_{ss} = 1$ and Lehovec's continuum model predicts symmetrical Gp/ω Vs. ω maximum at $\omega\Gamma_{ss} = 1.98$, taking into account the time constant dispersion for distribution levels. The interface state density distribution can be obtained from the experimentalG_p/ω Vs. ω curves measured for different bias values. The interface state density D_{it} is obtained from the value of the peak (G_p/ω)max. and the time constant is obtained from the relation $\omega\Gamma_{ss} = 1.98$ corresponding to the peak value of (Gp /w). Normally, D_{it} is measured as a function of energy in the semiconductor band gap. Hence, the step following the extraction of interface trap level density is to convert Dit as a function of gate voltage V_G to D_{it} as a function of $E_T - E_V$ ($E_C - E_\Gamma$ for n-type). The position of Fermi level with respect to the majority carrier band edges at the semiconductor surface must be determined as a function of gate bias for this step. Fig.3.7 shows how the position of Fermi level at the semiconductor surface is related to band bending for p-type semiconductor. The energy position of the trap level opposite the Fermi level at the interface is located at $E_F = E_T$,

where $(E_T-E_V)/q = E_g/q - \Phi_B - \Psi_S$, for p-type

$(E_C-E_T)/q = E_g/q - \Phi_B + \Psi_S$, for n-type

The band gap is scanned by varying Ψ_S which is accomplished by varying gate bias

Choice of Techniques for the Determination of Interface State Densty:

We have discussed the various methods available for the determination of interface state parameters. Of these the low frequency Berglund's technique poses problems due to the difficulty in measuring the low frequency capacitance plots in the presence of an ac insulator loss resistance and was hence rejected. The quasi static Kuhn's method and Q-V method were not used due to the finite leakage current present in the films which tends to mask partly or entirely the measured displacement current or charge through the MIS capacitor. The conductance method was not used because it has a major weakness in the limited surface potential range over which interface state density can be obtained.

Taking all these factors into consideration, we used the high frequency Terman's method for the determination of interface state parameters. The strength of this method lies in its simplicity which requires merely the measurement of the C-V curve at high frequency and the vital information about interface traps that can be extracted from it. Besides, this C-V method is a well established method requiring equipment which is not very cumbersome and easy to handle.

2. Conclusions

The study demonstrates that C–V characterization is an effective tool for analyzing MIS capacitor behavior and semiconductor–insulator interfaces. Non-ideal effects such as fixed charges, mobile ions, work-function differences, and interface states significantly influence device performance. Several techniques for interface state density determination were examined, each with specific advantages and limitations. Considering measurement complexity, leakage current effects, and practical applicability, the high-frequency Terman method was identified as the most suitable approach for determining interface state parameters. Its simplicity, reliability, and ability to provide valuable information about interface traps make it a preferred technique for the electrical characterization of MIS structures.

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