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Power Efficient Voltage Level Shifter using RCC Network and Stacking Technique

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Abstract: ***This paper presents a power efficient voltage level shifter using regulated cross - coupled network with split inverter. With the use of regulated cross - coupled network, the power dissipation of the pull - up region drastically decreases. Level shifters convert voltage levels below the threshold voltage to acceptable levels by reducing transistor size. A stacking split inverter is used at the output to decrease the short circuit current and leakage current. his paper presents a novel voltage level shifter design utilizing a regulated cross - coupled RCC network and a stacking technique for reduced power consumption in CMOS circuits. By integrating a split inverter and load capacitor at the load, the proposed design effectively minimizes leakage and short - circuit currents, achieving a 23% reduction in power dissipation compared to conventional methods. Simulation results using 180nm Cadence technology and 90nm LT Spice technology demonstrate enhanced speed and efficiency, highlighting the suitability of this approach for high performance VLSI applications.***

Keywords: Level Shifter, Split - Inverter, RCC Network, Threshold Level, Leakage Power, Short - Circuit Power

1. Introduction

A level shifter is a circuit used to convert signals from one logic state to another, which is applicable to circuits like CMOS and TTL. Level shifters are used in various domains like processor applications, sensors and VLSI design circuits. Voltages of 3.3V, 1.8V and even less voltage values are needed. Digital systems use level shifters to provide different voltage level logics to different blocks of a system, without shifters it is difficult to provide different voltages to different blocks within the system. Transition from high to low is often optional, but conversion from low to high is required in most cases. Level shifters are placed at the top, bottom or can be even at midway of circuit.

Power dissipation depends on supply voltage, load capacitance, frequency and on switching activation factor. Reducing these factors, helps to decrease power dissipation. Reducing the supply voltage by half, causes to decreases the power dissipation to 75%, but it affects the performance [5]. By providing different voltages to different blocks using a level shifter is a good choice [3, 4]. Supply voltages for the MOS transistors which are less than its Vth, possible with level shifters. Level shifter using a cross - coupled network drastically reduces the power dissipation and the speed of getting output increases. This LS method is usable for a large range of inputs.

2. Literature Survey

2.1 LS using Current Mirror

Level shifters can be implemented using current mirror, but there is one disadvantage with this design is that, there is no proper interaction between the pull - down transistors and pull - up transistors, it causes to high standby power is present due to static current.

A Level Shifter Current Mirror is a specialized circuit that merges the operations of a level shifter and a current mirror. It is commonly employed in mixed - signal or low - power designs where interfacing between different voltage domains is necessary. The level shifter aspect of the circuit handles the task of adjusting the voltage levels to ensure compatibility between components operating at different voltages. Meanwhile, the current mirror ensures that current is consistently replicated and maintained across the circuit, even when there are changes in voltage levels. This combination is essential in maintaining performance and reliability in complex electronic systems.

2.2 LS Using DCVS

DCVS based LS consists of cross - coupled network at pull - up, it can improve the interaction between pull - up and pull - down transistors which can cause to increase the speed. Standby power decreases as no static current exists, but pull - down transistor decreases when VDDH is less than Vth because NMOS transistor won't go beyond PMOS transistor. To increase the strength of transistors, the size of the transistors is scaled which in turn decreases the efficiency of the circuit [4].

2.3 LS using modified Wilson current mirror

LS using Wilson current mirror helps to maintain proper rise time and fall time but when VDDH and VDDL values are close to each other, the delay increases due to lack of driving. OR gate and delay path is introduced in order to increase the driving strength, as well as to control the leakage current [5].

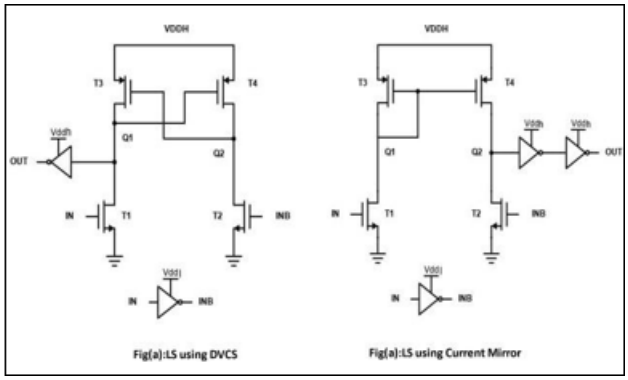

Figure 1: LS using DVCS and Current Mirror

Level Shifter using a Modified Wilson Current Mirror is an advanced circuit design that integrates the voltage level translation capabilities of a level shifter with the precision and enhanced performance characteristics of a modified Wilson current mirror. The Wilson current mirror is known for its improved output impedance and greater accuracy over simpler current mirror designs, making it an effective choice for ensuring consistent current replication. By modifying this topology to also serve as a level shifter, the circuit can translate voltage levels between different domains while still maintaining the key advantages of the Wilson current mirror, such as increased accuracy and stability. This design is particularly useful in applications requiring both efficient voltage interfacing and precise current control in low - power or mixed - signal circuits.

2.4 LS using feedback path

Self - controlled circuity is possible by providing the feedback path from the output to the input. It can convert the sub - threshold voltage to the voltage level above threshold level, ration of pull - up transistor is less compared to pull - down transistor so that pull - down transistor capacity will decrease, which causes to increases the short - circuit current [2, 7].

3. Existing Method

Existing LS uses DCVS structure which consists of RCC pull up network to increase the strength of pull up network and to increase the efficiency of charging and discharging at internal nodes, this will increase the switching speed. The circuit consists split inverter, current limiters and RCC network. The spilt inverter at the output is placed to reduce the short leakage current from pull - up transistors. The main advantage of shifter is, PMOS transistors will never be switched - off when they have gone to the sub - threshold region, with this we can get quick response and contention current can be minimized. A Current limiter is used to reduce the contention current.

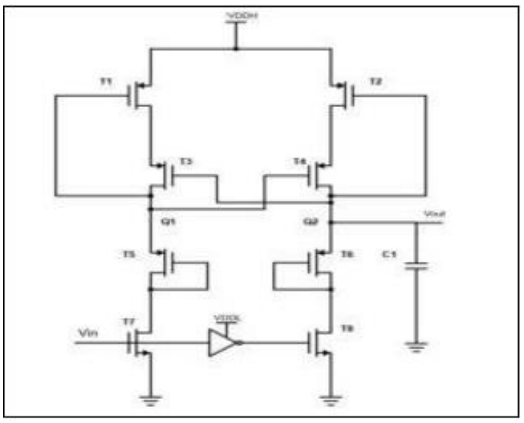

Figure 2: LS with RCC network

4. Implementation of LS with Stacking Split Inverter

Transistor current is decreased in the pull - up region and increased in the pull - down region with auxiliary by modifying the transistor size, with the result we can decrease the delay. A split inverter is used at the output to decrease the short circuit current.

4.1 Static leakage power

Leakage power is occurred due to the P - N junction reverse biased current. Sub - threshold current generated for short channel devices below threshold voltages. Sub - threshold depends on thermal voltage, actual gate voltage and threshold voltage difference.

Reverse biased current is given by

$$ID=IS\ (eV/Vt - 1) \quad \text{....1}$$

& sub - threshold current is given by

$$I_{SUB} = I_O e^{\frac{V_{GS} - V_{THO} - \eta V_{DS} + \gamma V_{BS}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad \text{....2}$$

4.2 Short - circuit leakage power

Short - circuit leakage power refers to the unintended power dissipation that occurs in CMOS circuits when both the PMOS and NMOS transistors are partially on simultaneously during switching events. This results in a direct current path between the power supply (Vdd) and ground (GND), causing power loss

Short - circuit power plays a key role in dynamic power consumption. Due to fall time and rise time of transistors, there exist short - circuit path between VDD to ground and leads to power dissipation.

a) Stacking Inverter

The transistor stacking technique effectively reduces leakage power in both active and standby modes by leveraging the Stack Effect, also known as the Self - Reverse Bias Effect. When two or more off - state transistors are connected in series, the leakage current is significantly lower than through a single off - state transistor due to the reverse bias created

across each transistor in the stack. By increasing the number of transistors in the stack, even greater leakage power savings can be achieved. This technique can be extended to circuits that do not inherently use stacking by implementing forced stacking, where additional transistors are introduced into the circuit to further reduce leakage current and improve power efficiency. In forced stacking, a single transistor of width "W" can be replaced by two transistors of width "W/2" each [13].

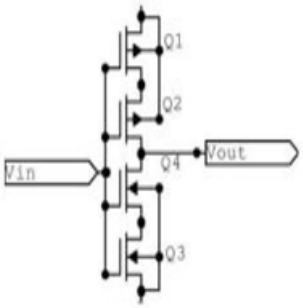

Figure 3: Stacking Inverter

During input transition from 1to0, N1 node is at HIGH and value N2 node is at low, it will switch on T2, T3 and T1, T4 will be OFF. When input transition 0 to 1 T7 will be ON and T8 will be OFF. It will pull the value N1 to low and when it is discharging, T1, T4 will switch ON and T2, T3 are switched OFF. At this instant, the N2 node will start charging, as the output is connected to N2 through the capacitor.

5. Simulation Results

Figure5 displays the schematic of LS with RCC& stacking inverter using 180nm technology, Input pulse is given with rise time & fall time taken as '0', initial voltage is taken as '0', Von voltage taken as '0.3' volts.

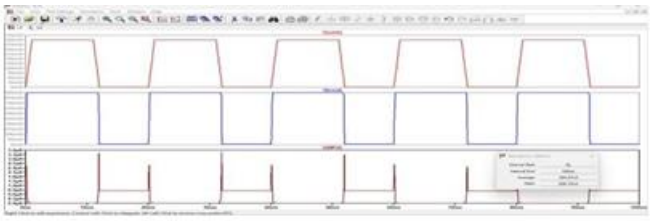

Figure 4: 90nm LT Spice technology - based Simulation of LS using stacking Inverter

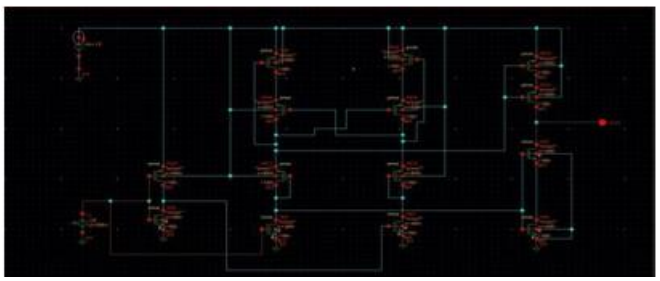

Figure 5:180 Cadence technology - based schematic diagram of LS using stacking Inverter

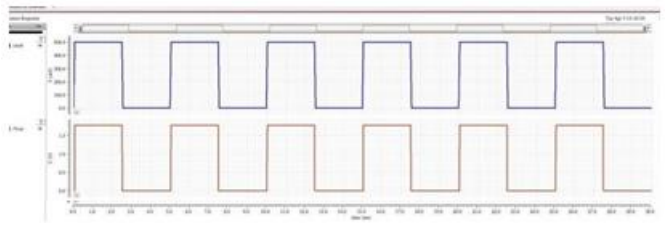

Figure 6: 180 nm Cadence technology - based Simulation of LS using stacking Inverter

6. Conclusion

The proposed voltage level shifter design significantly reduces leakage and short - circuit power dissipation while enhancing speed, making it a suitable choice for modern VLSI applications. The study demonstrates that integrating an RCC network with a stacking technique offers a substantial improvement over traditional designs, providing a 23% reduction in power consumption. Future research could explore further optimizations and applications in other low power electronic systems.

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