

Design of Op-Amp based Comparator

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Abstract: Operational amplifier is a DC coupled electronic voltage amplifier having high gain, consisting of two input terminals viz. inverting input terminal and non-inverting input terminal and is capable to produce a single output potential at V_{out} terminal. This paper is based on op amp as a comparator. In this paper we preferentially go towards the design of op-amp as a comparator. Here we will discuss about its static and dynamic operations, the comparator as a main block design in the sigma delta comparator. The Op-amp as comparator in the design of this type amplifier low power and high speed. The CMOS design of circuit has been verify by using IDE simulator.

Keywords: OP-AMP, Comparator, Modulator

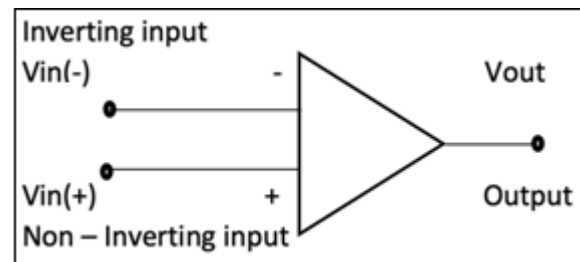
1. Introduction

The comparator is the major component during the designing of sigma delta comparator and also the principle block in this sigma delta comparator. The slightest bit quantizer can be actualized as a comparator whose yield flips among high and low voltage levels, V_{OH} and V_{OL} , in view of the extremity of its info voltage with respect to the reference voltage. To study of all present comparator architectures is outside the choice of the paper; here we bound our discussion to the open-loop comparators which is one of the maximum used structures in Sigma-Delta ADCs. A integrator and comparators satisfied both static and dynamic necessities in the designing part. The names imply static features deal with dc performance of the comparator, i. e. advantage of input resolution v_{in} with minimum and output voltage levels and dynamic characteristics such as slew rate and propagation delay (t_p) define the transient operation of comparator. The main design presented in paper at the architectural level and circuit level of the comparator offerings is taken since the [1-2]. The design steps followed in the paper is from [3], for the design of (W/L) of the transistors in the circuit with parameters of the design at the circuit level. Clock regenerate comparators and mostly used high speed ADCs because of their positive feedback in regenerative latches to take the fast decisions of signal comparison [6]. The digital version of this design has been proposed in the paper [7] which gives FPG and digital implementation of reconfigurable low pass decimation Architecture. The clocked digital comparator design from paper [10] the main concerns of the High-Gain with the low power.

The design of the Sigma-Delta Modulator and blocks and with architecture is in [4]. The strategy part of comparator present in paper is referred from [3], which helps out the designing part of the comparator with low power and high speed. This paper explains basics of comparator and its parameters of comparator in the Section 1.1. The application of CMOS schematic of the proposed design of the comparator in Cadence Virtuoso in 45nm CMOS technology is signified in the Section 1.2. The Section 2 explains the results obtained from the design and the comparison of the

design parameters with the previous work has been given in this Section.

Operational Amplifier: DC coupled electronic voltage amplifier having high gain, consisting of two input terminals viz. inverting input terminal and non-inverting input terminal and is capable to produce a single output potential at V_{out} terminal.



To produce an amplified output, potential difference is applied to both of the input terminal that amplifies and the amplified output thus obtained is nearly equal to hundreds of thousands of times of the difference the input signal. Mathematically, output of the amplifier can be written as

$$V_{out} = A_{OL}(V^+ - V^-)$$

Where, A_{OL} is an open loop gain of the amplifier and V^+ and V^- corresponds the non-inverting and inverting input of the amplifier respectively.

Operation amp based Comparator

The block present in Sigma-Delta Modulator is the comparator block. The comparator is a circuit that contrasts one simple sign and another simple sign or a reference voltage and yields a double sign dependent on the examination. The plan of the comparator depends on Operation Amp worked in open circle mode. The comparator is essentially a 1-bit Simple to-Advanced Converter. Comparator is one of the principle obstructs in nearly all ADC's, contingent on its size and structure it can survey affect the presentation of ADC.

