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Leakage Power Reduction Techniques for Low Process Technology VLSI Design Circuits

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Abstract: ***In VLSI based applications; specifications such as area, delay and power dissipation are taken in to account. In all the power dissipation plays important role. Power consumption reduces the battery life. In process technology is decreasing, in which the channel length is reduced leakage power increases. When the process technology is reducing leakage power becomes dominate. Leakage power is reduced considerably by using few techniques. We use LECTOR, LCNT and STACK ONOFIC techniques to reduce leakage power in VLSI design circuits such as inverter, NAND, NOR, MUX. For simulation EDA Tanner tool is used with 250nm technology.***

Keyword: LECTOR, LCNT, PMOS, NMOS, Leakage power

1.Introduction

In digital systems, specifications such as area, delay and power dissipation are key challenge parameters. High power dissipation causes to reduce the battery life time and more cooling is required to cool the components. Power dissipation can be reduced by reducing activity factor, decreasing load capacitance, decreasing voltage and step-down frequency, decreasing the sizes of the devices (W/L). We use techniques to reduce power dissipation. Static dissipation is present when circuit is not running mode and dynamic power dissipation is present when circuit switching. Dynamic power consumes more power compared to all powers. Leakage power is dominant when channel length is decreasing.

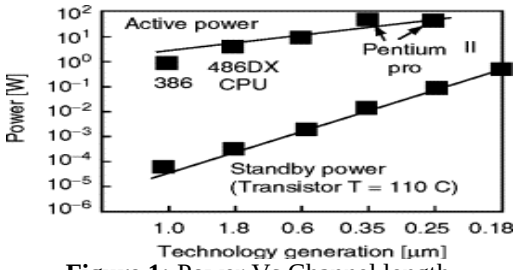


Figure 1: Power Vs Channel length

Consider a CMOS there are two types of powers are present namely static power and leakage power.

Static power cab be occurred due to following possible ways;

1. Sub-threshold leakage current
2. Drain induced barrier leakage
3. Punch through effect
4. Gate induced leakage
5. Short channel
6. Reverse bias effect

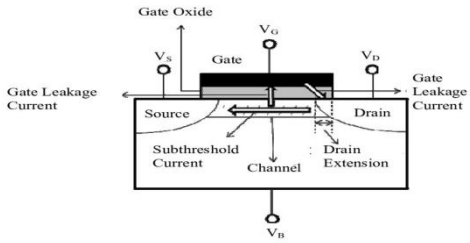


Figure.2: Leakage currents

When we come in to dynamic power, short circuit power and switching power are the dominant powers. . SC power is present between supply voltage and ground when both transistors are conducting at a time and that is due to difference in rise time fall times of input transition. Leakage power is present in MOS devices in static mode and dynamic mode. In dynamic mode also leakage power is present when circuit is in running mode and produces more leakage power compared to active power whenever the technology is decreasing. Leakage power is becoming dominant when the channel length is reduced.

We see major power dissipation powers;

1. Switching Power

It occurs when output is switching from one state to another it depends on

Activity factor
Decreasing load capacitance
Decreasing voltage
Step-down frequency

$$P = \alpha * f * C * Vdd^2$$

2. Static Leakage Power

Leakage power mainly due to Reverse-biased P-N junction and sub-threshold current.

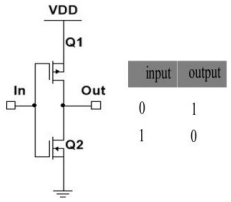
Sub threshold depend on thermal voltage and difference between gate voltage and threshold voltage

3. Short Leakage Power

It is present between voltage and ground when both transistors are running state at a time and glitch is present due to difference in rise time fall times of input transition.

2.Proposed Method

Inverter is a circuit, in which output is complement of input, when input is 0, PMOS transistor is going to conduct and NMOS transistor turn-off. There supply voltage charges the capacitor which is connected at the output, so for input logic 0 we will get output as logic 1. When input is 1, NMOS transistor is going to conduct and PMOS transistor turn-off. There capacitor voltage discharges to the ground. So, for input logic 0 we will get output as logic 1.



Fugue 3: Inverter

I. Lector Cell

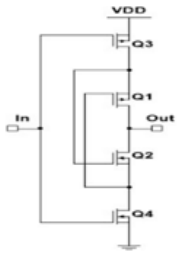


Figure 4: LECTOR Cell

In this technique, two extra transistors (Q1 & Q2) are used, here gate of each transistor is connected source of another transistor. Effective of this stacking between supply voltage and ground results low power consumption. During each transition input cycle one of the transistors are in cut of region which offers higher resistance, there by reduces leakage power dissipation.

II. LCNT Cell

In this technique, two extra NMOS transistors are used and these are connected between PMOS and NMOSS transistor. The gates of two extra transistors are connected to the output node. With this it increases the resistance between supply voltage and ground. In these techniques, disadvantage is that transistors cannot pull up or pull down to the exact value.

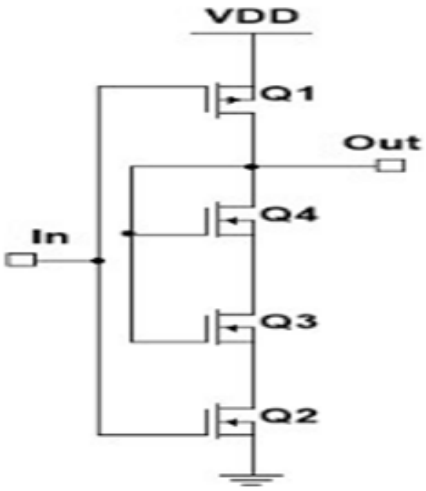


Figure 5: LCNT Cell

III. ONOFIC Cell

It is similar to the LCNT, except addition of PMOS transistor is added, gate of the extra Q5 transistor is connected to the output node and its drain terminal is connected to the gate of two transistors (Q1 & Q2). It reduces the leakage power as it offers higher resistance during the input transition.

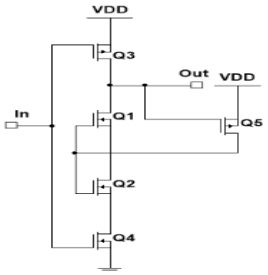


Figure 6: ONOFIC Cell

3.Simulation

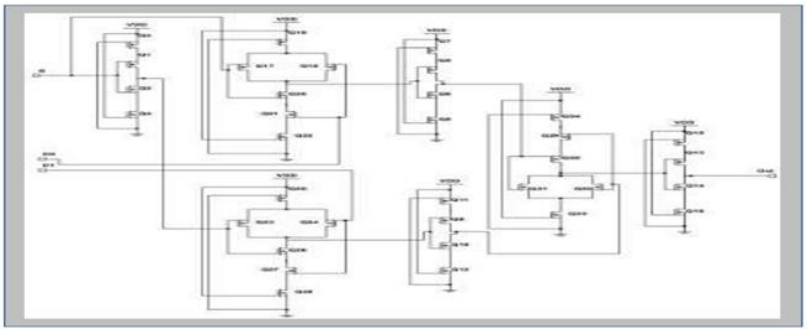


Figure 7: MUX Implementation

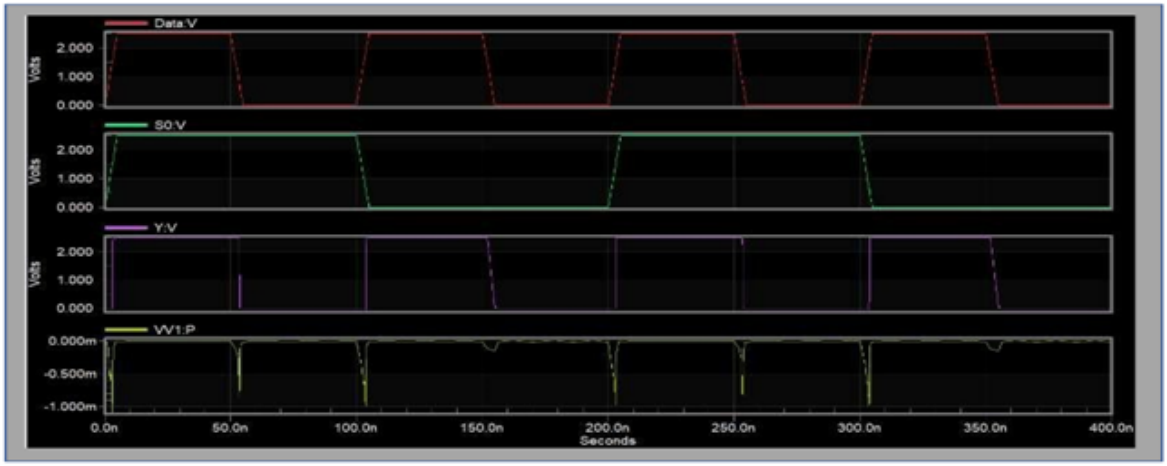


Figure 8: Simulation results

4.Conclusion

We use these techniques to reduce leakage power when channel length is reduces greatly. LECTOR, LCNT and ONOFIC cell are used to realize various; logic gates such as inverter, NAND gate, NOR gates etc. With these techniques area requirement is increased but leakage power decreased greatly which is very important parameter in low process technology. LECTOR, LCNT and ONOFIC decreases leakage power by 17%, 13% and 12% respectively.

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