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Design of Low Power Logic Gates for VLSI Design Circuits

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Abstract: ***High power consumption has become key role in VLSI design circuits, when it comes in battery - operated applications such that to save the battery life. Short - circuit power and switching power play key role in power dissipations, there are so many techniques to reduce power. By stacking arrangement, we can reduce power and we can utilize technique for various circuits. In this paper NAND and NOR gates realized, stacking technique consumes low power than standard reduction techniques. These circuits are simulated in Tanner EDA Tool with Generic 250 nm transistors.***

Keywords: NAND gate, NOR gate, Leakage Power, STACK, CMOS Transistor

1. Introduction

Digital systems have increasing demands in the area of low power consumption. area, power consumption, and propagation delay are significant designing parameters. High power consumptions lead to reduce battery life and it requires more cooling and packaging cost. We can reduce the power by reducing sizes of the devices, frequency and by using low load capacitance. In this paper low power ON transistor is used to reduce power consumption.

Source of Power Consumption

The short - circuit energy dissipation results due to short circuit path current flowing from the power supply to the ground during dynamic of a static CMOS gate. Short - circuit energy constitutes 10 - 20% of the total energy dissipation of a static CMOS gate. The dynamic power consumption of a CMOS IC is calculated by adding the switching power consumption (P, and load capacitance power consumption. Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. For better results large capacitive load is required but it increases the power dissipatio0n in dynamic state. Leakage power plays import role in CMOS circuits there are so many leakage currents in CMOScircuits. Energy consumes approximately 40 - 50 percentage of total power dissipation

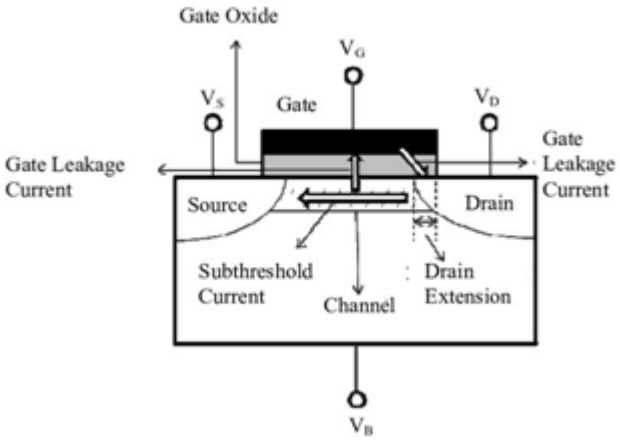


Figure 1: Leakage Currents

Dynamic power deals with short circuit and switching power whereas static power deals with static leakage power. Switching power: When there is a toggle of zero to one or vice versa charging and discharging of the parasitic capacitor happens. Static power leakage: Leakage power is mainly due to the reverse bias P - N junction current and sub - threshold channel conductance current. Sub - threshold power is due to the leakage current below the threshold voltages.

When both transistors are ON short circuit current is present and that is due to delay in rise time and fall times short circuit current power dissipation is present. there are so many ways to reduce short circuit power. by using stacking of NMOS transistors leakage power reduce greatly. By using muilt - threshold and various threshold CMOS circuits we reduce the leakage and short circuit power.

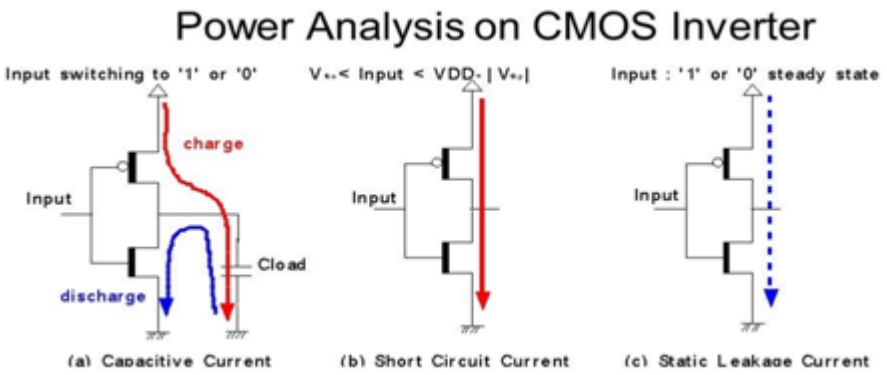


Figure 2: Short - Circuit Path Current

2. Proposed Technique

In the proposed technique, the logic block contains two SAPON transistors (PMOS and NMOS) whose gate terminal is connected to the ground and Vdd which operates in the active region. EDA trainer tool is used to analyze power. In this two leakage control transistors are built outside the circuit which increase the resistance between the Vdd and ground and also sub threshold leakage current is also reduced. In addition to this with CMOS SAPON transistors power switching performance increased. SAPON PMOS is placed above pull - up network and SAPON NMOS transistor is place below pull - down network. These two SAPON transistors need to operate in an active region which in turn makes them active in all phases. Hence, it provides desirable output by maintaining low power consumption across circuits.

When logic 0 is given PMOS transistor is on and NMOS transistor is OFF and SAPON transistors remain in active, output reads 1. Similarly when logic 1 is applied PMOS is OFF and NMOS transistor is ON and SAPON transistors remain active output will be logic 0.

NAND and NOR gates:

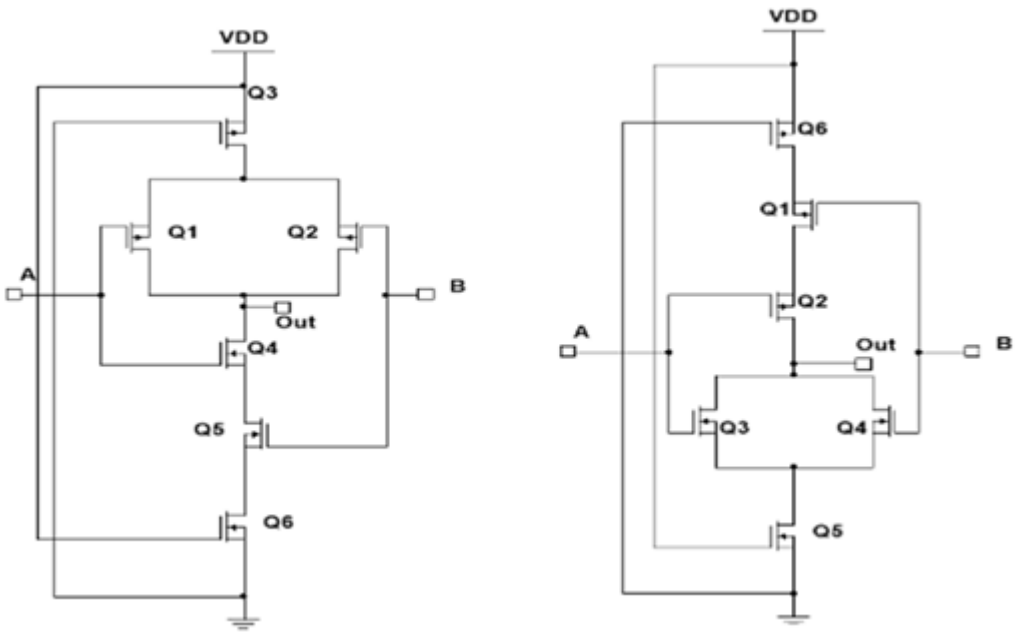
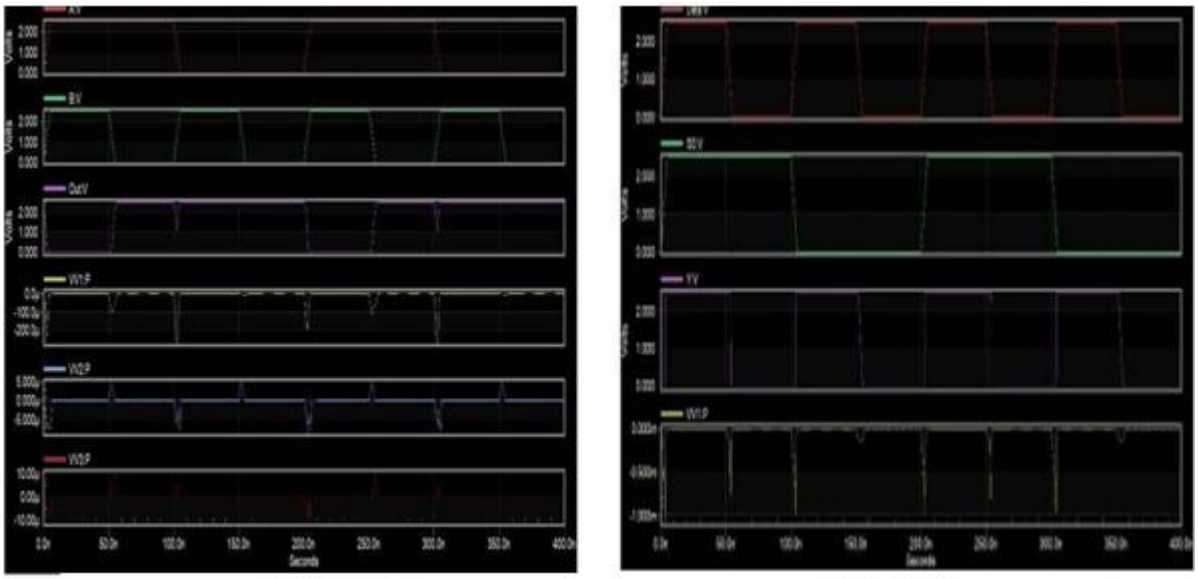


Figure 3: NAND gate NOR gate

Simulation Results

Proposed technique reduce 26% compared to existing method NAND, NOR gate transient analysis is for given combination of inputs and simulation results are observed in Tanner EDA



Fig(a) NAND gate

Fig(b) NOR gate

Figure 4: Simulation Results

3. Conclusion

In low power VLSI circuits, power dissipation plays key role to get optimize results. Using SAPON technique 26% power can be saved compared to existing method which in turn saves energy and yields better performance. Since we have achieved low power consumption using SAPON techniques in basic logic gates, one can attain the same in combinational circuits which are derived from basic gates.

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Author Profile

Telagamalla Gopi Received B - Tech degree from Scient Institute of Technology Hyderabad, completed M - Tech with VLSI system design from Sree dattha Institute of Engineering and Science. Currently working as Assistant Professor in Annamacharya Institute of Technology and Sciences, Hyderabad. Has published seven research papers in reputed journals. Areas of interest include digital signal processing and VLSI.