# Comparison of Conventional Single Phase 21-Level Cascaded H-Bridge MLI and Single Phase 21-Level MLI with Reduced Switches and Sources and Verifying the Topology with Hardware of 7-Level MLI

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Abstract: Multilevel Inverters are influencing many industries because of their applications in renewable energy with low switching losses, low THD and high dv/dt stress. In this paper, conventional single phase 21 level cascaded H-bridge multilevel inverter and single phase 21 level multilevel inverter with reduced switches and sources have been compared. Here, a conventional single phase 21 level cascaded H-bridge multilevel inverter and 21 level multilevel inverter with reduced switches and sources, the switching angles and the corresponding time required to generate the gating pulses of IGBT switches of both multilevel inverters is calculated by Equal Phase (EP) Method. The conventional single phase 21 level cascaded H-bridge MLI with 40 IGBT switches and 10 separate DC sources whereas multilevel inverter with reduced switches and sources require only 8 IGBT switches and 4 separate DC sources to obtain 21 level output voltage. Since, in case of 21 level multilevel inverter with reduced switches and sources, the number of switches are less, the cost is less and the circuitry is simple. The simulation results of both were presented using MATLAB/SIMULINK. Also hardware implementation of 7 level reduced numbers of switches and sources multilevel inverter is done and the results are shown.

Keywords: Multilevel Inverter (MLI), Equal Phase(EP), Separate DC Sources (SDCS), Total Harmonic Distortion (THD).

#### 1. Introduction

Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low Total Harmonic Distortion (THD). The term multilevel starts with the three-level inverter introduced by Nabae et al (1981). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference.

There are different types of inverter topologies are available in which some are popular. Different types of MLI are Diode Clamped MLI, Flying capacitor type MLI and Cascaded H-Bridge multilevel inverter and that is very popular among all the topologies. In this paper, conventional single phase 21 level Cascaded H-Bridge Multilevel Inverter and single phase 21 level multilevel inverter with reduced switches and sources have been compared. The output voltage results were simulated and presented in this paper [1] [2]. Also, Switching angles of both multilevel inverters can be calculated by following methods:-

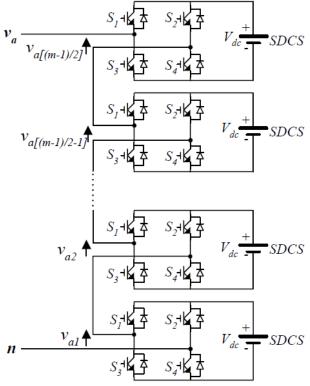
- Equal Phase (EP) Method.
- Half Equal Phase (HEP) Method.
- Half Height (HH) Method.
- Feed Forward (FF) Method.

In this paper switching angles of both a conventional single phase 21 level cascaded H-bridge multilevel inverter and single phase 21 level multilevel inverter with reduced switch and sources have been calculated by using Equal phase method. Finally, these two topologies have been compared and corresponding work has been embodied as follows.

#### 2. Conventional Single Phase 21 Level Cascaded H-Bridge Multilevel Inverter

As the name suggest, conventional single phase cascaded Hbridge multilevel inverter is constructed by a series of Hbridge inverter in cascade configuration. This type of topology is a conventional configuration structure. The topology proposes a concept with a use of separate DC sources connected to each H-bridge to generate a sinusoidal voltage. The final ac output voltage is produced by cascading the individual H-bridge voltage outputs [3].

Figure 2.1 illustrates a generalized block diagram of Conventional Single Phase m-level Cascaded H-bridge Multilevel Inverter. In this case, 21 different voltage output levels were generated for each inverter level with an appropriate control scheme of the switches. The output waveform is generated was as according to the switching table given below in the table. The sum of different individual H-bridge inverter outputs connected in series synthesized the final sinusoidal output voltage of the multilevel inverter. An equation m=2s+1 determine the number of voltage levels 'm' in a conventional single phase 21 level cascaded H-bridge inverter where 's' is the number of independent DC source connected to the individual Hbridge inverter. Thus there were 10 separate DC sources used in this topology. The final output voltage  $V_{a[(m-1)/2]}$  is a sum of all individual voltage values of H-bridges connected in cascade. The simulink result of voltage output is shown in Figure 2.2. Also THD analysis of conventional single phase 21 Level cascaded H-bridge MLI is shown in figure 3.1. by FFT analysis with the aid of MATLAB/SIMULINK[4].



**Figure 2.1:** Generalized block diagram of Conventional Single Phase m-level Cascaded H-bridge Multilevel Inverter

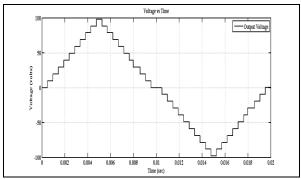


Figure 2.2: Voltage output of conventional single phase 21 level cascaded H-Bridge MLI by EP method

<b>Table 2.1:</b> Voltage levels of conventional single phase 21
level cascaded H-Bridge MLI by EP method

Voltage Level	Numbers of on Switches
10 <b>V<sub>dc</sub></b>	1,2,6,10,14,18,22,26,30,34,37,38
9 V <sub>dc</sub>	1,2,6,10,14,18,22,26,30,33,34,38
8 V <sub>dc</sub>	1,2,6,10,14,18,22,26,29,30,34,38
7 <b>V<sub>dc</sub></b>	1,2,6,10,14,18,22,25,26,30,34,38

6 V <sub>dc</sub>	1,2,6,10,14,18,21,22,26,30,34,38
5 V <sub>dc</sub>	1,2,6,10,14,17,18,22,26,30,34,38
4 V <sub>dc</sub>	1,2,6,10,13,14,18,22,26,30,34,38
3 <b>V<sub>dc</sub></b>	1,2,6,9,10,14,18,22,26,30,34,38
2 <b>V<sub>dc</sub></b>	1,2,5,6,10,14,18,22,26,30,34,38
$1 \frac{V_{dc}}{V_{dc}}$	1,2,6,10,14,18,22,26,30,34,38
0	-
- 1 V <sub>dc</sub>	4,8,12,16,20,24,28,32,36,39,40
-2 <b>V<sub>dc</sub></b>	4,8,12,16,20,24,28,32,35,36,39,40
-3 <b>V<sub>dc</sub></b>	4,8,12,16,20,24,28,31,32,36,39,40
-4 V <sub>dc</sub>	4,8,12,16,20,24,27,28,32,36,39,40
-5 V <sub>dc</sub>	4,8,12,16,20,23,24,28,32,36,39,40
-6 V <sub>dc</sub>	4,8,12,16,19,20,24,28,32,36,39,40
-7 V <sub>dc</sub>	4,8,12,15,16,20,24,28,32,36,39,40
-8 V <sub>dc</sub>	4,8,11,12,16,20,24,28,32,36,39,40
-9 V <sub>dc</sub>	4,7,8,12,16,20,24,28,32,36,39,40
-10 <b>V<sub>dc</sub></b>	3,4,8,12,16,20,24,28,32,36,39,40

## 3. Calculation of Switching Angles

The several methods of estimating the switching angle have been proposed. In this paper, Equal phase (EP) method is considered for calculation of switching angles for both a conventional single phase 21-level cascaded H-bridge multilevel inverter as well as single phase 21 level multilevel inverter with reduced switch and sources[5].

#### Equal Phase Method

In this method, the estimation of switching angles were performed by the equation (3.1),

$$\alpha_i = i * \left(\frac{180}{m}\right) \tag{3.1}$$

Where, 
$$i = 1, 2, 3, 4, \dots, \frac{(m-1)}{2}$$

and 'm' is number of output level. These switching angles are distributed averagely over the range 0 - 180 degree.

The switching table of conventional single phase 21 level cascaded H- bridge MLI is illustrated in Table 2.1. The switching angles(by EP method) and corresponding PWM inputs were given to both conventional single phase 21 level cascaded H-bridge MLI as well as 21 level MLI with reduced switches and sources. Figure 2.2 shows the voltage output conventional single phase 21-level cascaded H-bridge MLI obtained from Equal Phase method. The harmonic spectrum for the conventional single phase 21 level cascaded H-bridge multilevel inverter output voltage has been computed with the help of Fast Fourier Transform function (FFT) in MATLAB Simulink[6].

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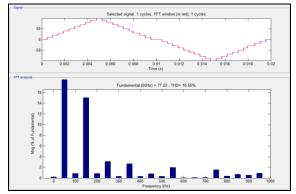


Figure 3.1: THD and FFT analysis of conventional single phase 21 Level Cascaded H-Bridge MLI

## 4. Proposed 21 Level Multilevel Inverter With Reduced Switches And Sources

The advantages of the DTC is to eliminate the direct and Figure 4.1 shows the circuit diagram of the proposed 21 level multilevel Inverter with reduced switches and sources. In this, 8 IGBT switches, 4 separate DC sources and 8 power diodes were used[7]. The working principle of this inverter is described with the help of Table 4.1.

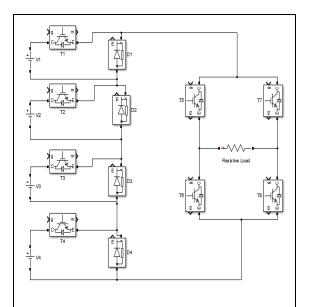


Figure 4.1- The circuit diagram of the proposed single phase 21 level multilevel inverter with reduced switches and sources

#### Modes of operations:

- Mode 1: In this mode, when switches T1, T2, T3, T4, T5, T6, T7, T8 are turned "off", the output voltage will be '0'.
- Mode 2: When switches T1, T5, T8 are turned "on", the output voltage across the load will be 'V1'.
- Mode 3: When switches T2, T5, T8 are turned "on", the output voltage will be 'V2'.
- Mode 4: When switches T3, T5, T8 are turned "on", the output voltage will be 'V3'.
- Mode 5: when switches T4, T5, T8 are turned "on", the output voltage across the load will be 'V4'.

- Mode 6: When switches T1, T4, T5, T8 are turned "on", the output voltage will be 'V1+V4'.
- Mode 7: When switches T2, T4, T5, T8 are turned "on", the output voltage will be 'V2+V4'.
- Mode 8: When switches T3, T4, T5, T8 are turned "on", the output voltage will be 'V3+V4'.
- Mode 9: When switches T1, T3, T4, T5, T8 are turned "on", the output voltage across the load will be 'V1+V3+V4'.
- Mode 10: When switches T2, T3, T4, T5, T8 are turned "on", the output voltage will be 'V2+V3+V4'.
- Mode 11: When switches T1, T2, T3, T4, T5, T8 are turned "on", the output voltage will be 'V1+V2+V3+V4'.
- Mode 12: When switches T1, T6, T7 are turned "on", the output voltage across the load will be '-V1'.
- Mode 13: When switches T2, T6, T7 are turned "on", the output voltage will be '-V2'.
- Mode 14: When switches T3, T6, T7 are turned "on", the output voltage will be '-V3'.
- Mode 15: when switches T4, T6, T7 are turned "on", the output voltage across the load will be '-V4'.
- Mode 16: When switches T1, T4, T6, T7 are turned "on", the output voltage will be '-V1-V4'.
- Mode 17: When switches T2, T4, T6, T7 are turned "on", the output voltage will be '-V2-V4'.
- Mode 18: When switches T3, T4, T6, T7 are turned "on", the output voltage will be '-V3-V4'.
- Mode 19: When switches T1, T3, T4, T6, T7 are turned "on", the output voltage across the load will be '-V1-V3-V4'.
- Mode 20: When switches T2, T3, T4, T6, T7 are turned "on", the output voltage will be '-V2-V3-V4'.
- Mode 21: When switches T1, T2, T3, T4, T5, T8 are turned "on", the output voltage will be '-V1-V2-V3-V4'.

 Table 4.1: The all positive level switching states of single

 phase 21 level MLI with reduced switches and sources with

 corresponding voltage levels

	лтеsp	onun	ig vo	nage	levers	\$		
Output voltage	T1	T2	T3	T4	T5	T6	T7	T8
V1+V2+V3+V4	1	1	1	1	1	0	0	1
V2+V3+V4	0	1	1	1	1	0	0	1
V1+V3+V4	1	0	1	1	1	0	0	1
V3+V4	0	0	1	1	1	0	0	1
V2+V4	0	1	0	1	1	0	0	1
V1+V4	1	0	0	1	1	0	0	1
V4	0	0	0	1	1	0	0	1
V3	0	0	1	0	1	0	0	1
V2	0	1	0	0	1	0	0	1
V1	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0

# 5. MATLAB Result of Single Phase 21 Level MLI with Reduced Switches and Sources

Equal Phase Method for calculation of switching angle gives better output voltage. The switching pulses obtained through Equal Pulse Method is illustrated in Figure 4.1.

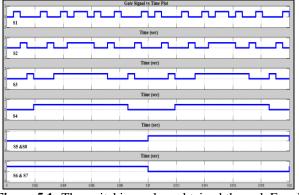


Figure 5.1: The switching pulses obtained through Equal Pulse Method

Figure 4.2, shows voltage output for the proposed single phase 21-level MLI with reduced switches and sources obtained from Equal Phase method. The harmonic spectrum for the proposed inverter output voltage has been computed with the help of Fast Fourier Transform function (FFT) in MATLAB/ SIMULINK.

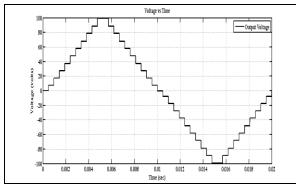
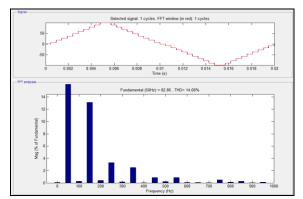


Figure 5.2:- Voltage output waveform of proposed single phase 21 level MLI with reduced switches and sources by EP method



**Figure 5.3:** THD analysis of proposed single phase 21 level MLI with reduced switches and sources by EP method

A brief study which is based on the number of switches, diodes, sources of proposed topology with conventional topology for 21 level voltage output is carried out. The results are given in Table 4.1. From this table, it is clear that the proposed Multilevel Inverter requires a lesser number of switches and voltage sources to achieve the required output voltage.

	Table 5.1- Comparison of MLIs					
		Cascaded	Reduced			
	Parameter	Conventional	Switches and			
		MLI	Sources MLI			
1.	Number of Levels	21	21			
2.	No. of DC Sources	10	4			
3.	No. of Switches	40	8			
4.	THD	16.65%	14.66%			
5.	Cost	More	Less			

amples C compo Tundamen	per oner	cycle t	= = =	0.1587 77.22 peak (54.6	rms)
THD			=	16.65%	
0	Hz	(DC):		0.21%	270.0°
50	Hz	(Fnd) :		100.00%	0.3°
100	Hz	(h2):		0.81%	
150	Hz	(h3):		15.07%	
200	Hz	(h4):		0.83%	-1.2°
250	Ηz	(h5):		3.08%	-2.4°
300	Hz	(h6):		0.31%	
350	Hz	(h7):		2.66%	
400	Hz	(h8):		0.31%	18.2°
450	Hz	(h9):		0.77%	23.9°
500	Ηz	(h10):		0.30%	-2.7°
		(h11):		1.94%	
600	Ηz	(h12):		0.03%	
650	Hz	(h13):		0.08%	
700	Ηz	(h14):		0.06%	
750	Hz	(h15):		1.51%	202.9°
800	Hz	(h16):		0.32%	50.8°

Figure 5.4: Harmonic analysis of conventional single phase 21 Level Cascaded H-Bridge MLI

		6.87285e-05 s	
Samples p	per cycle =	291	
DC compon	nent =	0.04501	
Fundament	al =	82.86 peak (58.	59 rms)
THD	=	14.66%	
0 H	Iz (DC):	0.05%	270.0°
50 H	Iz (Fnd):	100.00%	-4.2°
100 H	Iz (h2):	0.27%	50.1°
150 H	Iz (h3):	13.15%	167.5°
200 H	Iz (h4):	0.42%	23.7°
250 H	Iz (h5):	3.31%	-19.4°
300 H	Iz (h6):	0.18%	186.7°
350 H	Iz (h7):	2.52%	145.3°
400 H	Iz (h8):	0.03%	35.3°
450 H	Iz (h9):	0.88%	-44.4°
500 H	Iz (h10):	0.20%	112.8°
550 H	Iz (h11):	0.84%	134.9°
600 H	Iz (h12):	0.09%	259.3°
650 H	Iz (h13):	0.08%	-77.9°
700 H	Iz (h14):	0.04%	206.0°
750 H	Iz (h15):	0.47%	120.6°
800 H	Iz (h16):	0.11%	169.8°

Figure 5.5: Harmonic analysis of single phase 21 level mli with reduced switches and sources

## 6. Hardware Model

#### A.List of components

- 1) Arduino uno R3 microcontroller board- 2 No
- 2) IRFZ44N n channel MOSFET- 2 No
- 3) IRF9630 p channel MOSFET- 2 No
- 4) IRF630 n channel MOSFET- 2 No
- 5) 2N2222 Transistor- 4 No
- 6) Resistors- 10 No

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- 7) 1N4007 Diodes- 2 No
- 8) LED-6 No
- 9) Zero PCB- 2 No
- 10) Batteries- 2 No

#### **B.7.5.2** Specification of hardware Components

Sr.	Name of Component	Specification of
No.	Finite of Component	Component
1	Arduino uno R3	component
2	IRFZ44N - n channel	VDSS = 55V, ID = 49A
	MOSFET	
3	IRF630 - n channel MOSFET	VDSS = 200V, ID = 9A
4	IRF9630 - p channel MOSFET	VDSS = -200V, ID = -9A
5	2N2222 Transistor	VEB = 6V, IC 600 mA
6	BC548 Transistor	VEB = 6V, IC 100 mA
7	Resistor	0.25W, 10 KΩ
8	Resistor	0.25W, 220 Ω
9	Resistor	0.25W, 110 Ω
10	1N4007 Diodes	IF = 1 A, VF < 1.1 V
11	LED	IF = 25  mA, VF = 3.5V
12	Zero PCB	-
13	Battery 1	6 V
14	Battery 2	14 V
15	Auxiliary power supply	9 V
16	Power supply for Arduino uno	Constant DC 5V supply

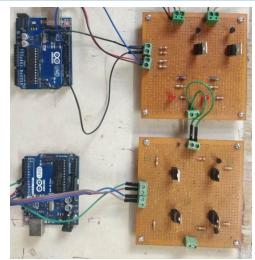


Figure 6.1: Hardware model of 7-Level MLI with reduced switches and sources

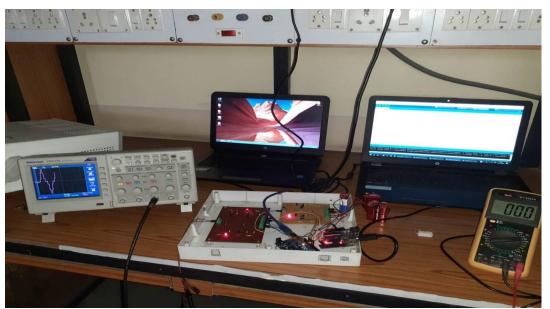


Figure 6.2: Complete hardware setup

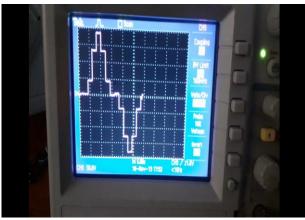


Figure 6.3: Voltage output on CRO

#### 7. Conclusion

The proposed single phase 21 level multilevel inverter with reduced switches and sources offers minimum switching devices and minimum separate DC sources for generating 21 level output voltage. The results of the proposed MLI comes in diminished size, lesser loss, along with low installation cost. In addition, THD in the output voltage of the proposed single phase 21 level MLI with reduced switches and sources is low. Therefore, it is reasonable for medium and high-power applications. The calculation of switching angles was obtained through Equal Phase Method. The simulation result showed that the Equal Phase method offers less THD compared with normal pulse generator input. Besides, Equal Phase Method achieves high RMS output voltage. Future work can be performed having made a 31-level inverter from

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the same circuit. The hardware implementation of 7 level reduced number of switch multilevel inverter is done with simulations in MATLAB/SIMULINK. The observations taken from the simulation and hardware results are mentioned in the table given below:

Sr. No.	MATLAB Observations	HARDWARE Observations
	for output voltage of 7	for output voltage of 7 level
	level Reduced number of	Reduced number of Switch
	Switch MLI	MLI
1	15 Volts Sinusoidal	14 Volts Sinusoidal
	staircase waveform	staircase waveform

## References

- [1] M. bin Arif, S. Ayob, A. Iqbal, S. Williamson and Z. Salam, "Ninelevel asymmetrical single phase multilevel inverter topology with low switching frequency and reduce device counts", 2017 IEEE International Conference on Industrial Technology (ICIT), 2017.
- [2] Aditay Vardhan Singh, Ravi Shankar Singh, "A Comparative Study of Multilevel Inverter Topologies" IRJET, Volume: 05 Issue: 03 | Mar-2018
- [3] V. Devi and S. Srivani, "Modified phase shifted PWM for cascaded H bridge multilevel inverter", 2017 Third International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), 2017.
- [4] Ehsan Najafi, Member, IEEE, and Abdul Halim Mohamed Yatim, Senior Member, IEEE, "Design and Implementation of a New Multilevel Inverter Topology ",IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 59, NO. 11, NOVEMBER 2012.
- [5] N. Agrawal and P. Bansal, "A new 21-level asymmetrical multilevel inverter topology with different PWM techniques", 2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE), 2017.
- [6] Aparna Prayag, Sanjay Bodkhe, "A Comparative Study of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology for Industrial Drive." IRJET, Volume: 05 Issue: 02 | Feb-2018.
- [7] Md. Tariqul Islam, Md. Shahidul Islam and Arnob Kumar Bairagi, "A New Single Phase 21 Level Inverter Topology with Reduced Number of Switches and Sources for Renewable Energy Applications", 4th International conference on Electrical Engineering and information and communication technology.

# **Author Profile**



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