Design and Implementation of Physical Aware Synthesis for Processor Core Application

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Abstract: *The predominant influence of physical synthesis lies in fostering a streamlined, anticipatable design flow, minimizing the necessity for rework and corrections as the design transitions seamlessly from the front - end to the back - end and ultimately reaches tape - out. This coherent design flow not only accelerates the time - to - market for the chip but also enhances its overall quality. The expeditious time - to - market can significantly bolster the lifetime revenue of advanced design projects by establishing an early market lead, potentially capturing a larger market share. Concurrently, heightened product quality can yield comparable advantages. In a physical synthesis design flow, an initial floorplan is established to provide placement information, accompanied by estimates of routing requirements derived from this floorplan. Cutting - edge design flows employ signoff - quality tools for these preliminary phases, maintaining consistency through the utilization of a unified data model shared among all tools in the workflow.*

Keywords: Architecture Design, Red Channel Compensation, Underwater Image Processing, Floating point arithmetic, power

1. Introduction

Prior to delving into the concept of physical synthesis, it is beneficial to elucidate the notion of logic synthesis. Originating from Synopsys, logic synthesis receives a circuit description in a high - level language like Verilog or VHDL as its primary input. Additional inputs encompass timing constraints for the design and specifications for the target implementation technology. The logic synthesis software scrutinizes these inputs and translates them into a specific configuration of interconnected logic elements sourced from cell libraries, which are integral inputs to the process. The overarching goals of logic synthesis encompass optimizing the timing, area, and power aspects of the resulting design.

For an extended period, logic synthesis served as a highly efficient approach for designing integrated circuits (ICs). The synthesized logic was then transferred to a place - and - route tool, which executed the necessary procedures to physically instantiate the circuit in silicon. However, at advanced process nodes, this conventional process encounters challenges. Following placement and routing, the physical manifestation of the circuit experiences deviations from its logical counterpart due to the impact of wiring, such as heightened signal delay and voltage drop, and parasitic effects arising from the proximity of specific devices. Consequently, achieving a functional design necessitates numerous iterations between logic synthesis and place - and - route.

Physical synthesis incorporates these implementation effects by taking into account the physical properties and constraints of the materials and fabrication process. The early establishment of a design floorplan, coupled with detailed routing estimates, offers preliminary insights into the aforementioned physical effects. Consequently, physical synthesis facilitates a convergent design flow, minimizing the need for extensive iterations.

Physical aware synthesis, on the other hand, is a methodology for designing and synthesizing electronic circuits that acknowledges the physical characteristics and limitations of the materials and fabrication processes employed. This encompasses considerations such as temperature, power consumption, and manufacturing tolerances. The primary objective of physical aware synthesis is to enhance the performance and reliability of electronic devices while concurrently reducing costs and design time. Advanced simulation tools and techniques, including physics - based modelling and machine learning, are instrumental in achieving these goals.

The considerable impact of wiring and placement in advanced technology nodes introduces significant physical effects. Failure to account for the delays and voltage drops resulting from extended wires during the synthesis phase poses a substantial challenge in meeting the power, performance, and area specifications of the chip.

Numerous extended design iterations between the front - end and back - end design stages lead to heightened design project expenses and a considerable elongation of the time needed to finalize the design. This is further elucidated below.

2. Proposed Methodology

As electronic devices evolve in complexity and sophistication, the significance of the physical limitations and properties inherent in the materials and devices utilized in their construction becomes increasingly pronounced. These limitations and properties wield a substantial impact on the device's performance, reliability, and energy efficiency. To devise and enhance electronic devices that align with the requisite standards for performance, reliability, and energy efficiency, it is imperative to take into

account the physical properties of the materials and devices employed.

This undertaking is particularly demanding as the specifications for electronic devices grow more stringent, with an escalating demand for devices that exhibit heightened energy efficiency, reliability, and environmental friendliness. Furthermore, the increasing integration and interconnectivity of electronic devices compound the challenge of designing and optimizing them while considering the physical properties of the materials and devices in use.

Physical aware synthesis endeavours to tackle this issue by furnishing a suite of techniques and tools tailored to design and optimize electronic devices, all while accounting for the physical properties of the materials and devices employed. This encompasses considerations such as temperature, power consumption, and electromagnetic interference. The ultimate objective is to craft electronic devices that are not only more efficient and reliable but also environmentally friendly.
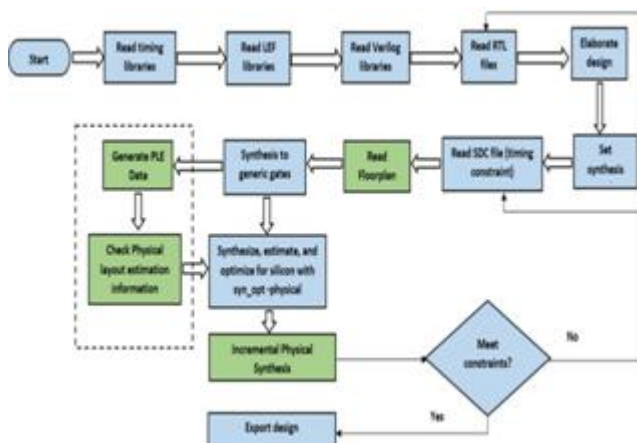

Figure 1: Methodology / Project Flow

This flow which is indicated in Fig.1 typically includes the following steps:
- **High - level design**: In this step, the overall architecture and functionality of the IC are defined.
- **Logic synthesis**: In this step, the high - level design is translated into a gate - level representation using a logic synthesis tool.
- **Physical synthesis**: In this step, the gate - level design is optimized for the physical layout of the IC, considering factors such as placement, routing, power, and thermal constraints.
- **Place and Route**: In this step, the IC's components are placed and routed on the chip, considering the physical constraints and design rules.
- **Timing and power analysis**: In this step, the timing and power characteristics of the IC are analyzed to ensure that they meet the required specifications.
- **Design for Manufacturability (DFM):** In this step, the design is optimized for manufacturability by considering the effects of manufacturing variations.
- **Tape out:** After all the above steps are done, design is sent to the foundry for fabrication.

- A physical aware synthesis project can be challenging and requires expertise in both digital design and physical design.

3. Experimental Results and Discussions

Our proposed hardware design flow was Verilog coded and simulated using Cadence Genus tool. Fig.2. showsthe simulation output of the Processor core application design. The Synthesis was done using Cadence Genus tool for 45nm Technology node at 100 MHz of operating frequency. The Fig.3. shows the synthesized hardware of proposed architecture.
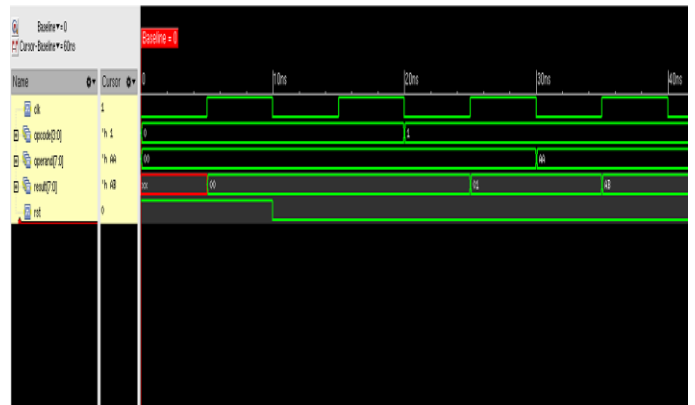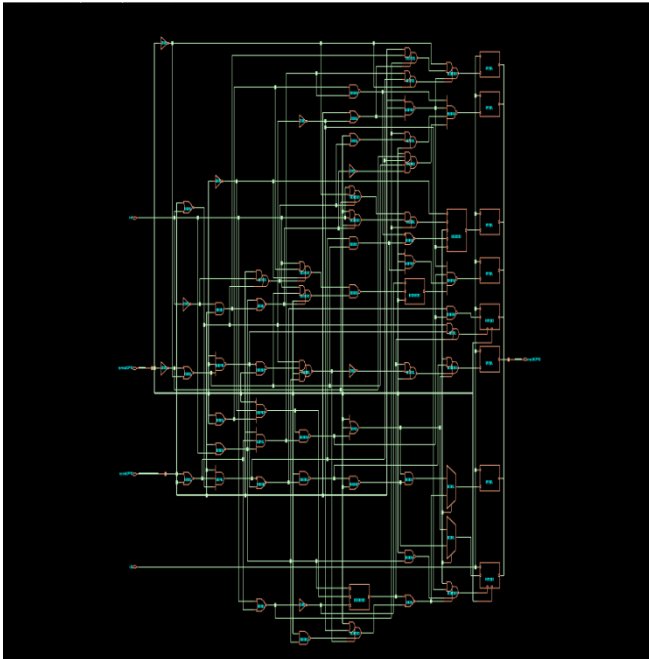

Figure 2: Simulation Result.

At first, the RTL code and test bench for the Processor Core Application was written and simulated in Cadence Genus tool to observe the design's behavior and the functionality which is depicted in Fig.2
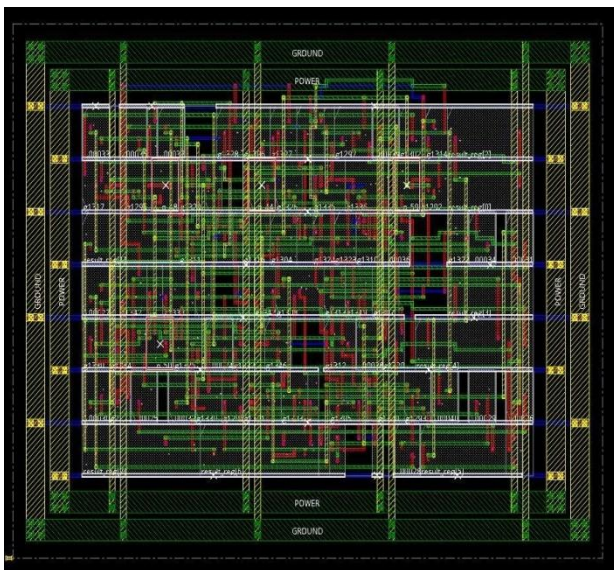
This functionality testing for the design in the simulation was carried out by feeding various combinations of the inputs on verifying its behavior.

The above depicted Table 1. gives the comparison between Logical and Physical Aware Synthesis in terms of Power, Area, and Timing. It clearly conveys that Physical Aware Synthesis has the better results in terms of PPA when compared to Logical Synthesis.

4. Conclusion

In general, physically aware synthesis is a technique that utilizes the use of physical information such as physical libraries, placement of macros, blockages, and area information to the synthesis tool.

Physical aware synthesis is a method of designing and synthesizing electronic systems that consider the physical constraints and properties of the materials and devices used in the system. The goal of physical aware synthesis is to improve the performance and reliability of electronic systems while reducing the cost and power consumption. The process typically involves the use of advanced simulation and optimization techniques to optimize the design of the system based on the physical properties of the materials and devices used.

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Figure 3: Synthesis Result (Gate Level Netlist)

After Successful completion of simulation, the design was carried out the next step which is Logical Synthesis where the RTL logic will be converted to Gate level Netlist which is depicted in the Fig 3

Figure 4: Final PnR Layout

The above depicted figure is of Final PnR (Place and Route) Layout of the design which was captured from Cadence Innovus tool. The tool used for Logical Synthesis was Cadence Genus Synthesis Solution

Table 1: Comparison Table

S. No	Parameters	Logical Synthesis	Physical Synthesis
1	TimingSlack (ps)	15341	15511
2	Area (mm^2)	139.194	90.408
3	Power (µW)	3.013	2.282

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