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Leakage Reduction Technique for Scan Flip-Flop

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Abstract: ***Scanning of test vectors during testing causes unnecessary and excessive switching in the combinational circuit compared to that in the normal mode of operation. In proposed system we have created a scan flip-flop based on MTcmos for leakage reduction which eliminates the power consumed due to unnecessary switching in the combinational circuit during scan shift, with a little impact on its performance. Multi-threshold CMOS (MTCMOS) power gating is a design technique in which a power gating transistor is connected between the logic transistors and either power or ground, thus creating a virtual supply rail or virtual ground rail, respectively, the new scan flip-flop by using sleep transistors it will reduce the leakage.***

Keywords: Sequential circuit, MTCMOS, ATPG, CUT, Leakage current, scan flop.

1. Introduction

Testing of highly complex SoC designs is a big challenge faced by VLSI test community nowadays. Scan design is the only DFT approach that can effectively test a highly complex design with very high fault coverage. The objective of scan design is to achieve full controllability and observability of every flip-flop in the design. In a full scan design, each flip-flop is replaced by a scan flip-flop. A scan flip-flop is nothing but a muxed input master-slave based D type flip-flop. The scan multiplexer has two inputs: data input (D) and scan input (SI). The input selection is performed using a control signal called test enable (TE). In functional mode, data input is selected and the scan flip-flop function as a regular flip-flop. In test mode, scan input is selected, and all the scan flip-flops connect in a serial fashion to form one or more serial shift register (s). The serial shift register (s) is popularly known as scan chain (s). All flip-flops of the scan chain are loaded with desired data by consecutive application of the clock signal. A full scan design reduces the sequential test problem to combinational test problem. The serial scan is obviously not free from drawbacks. There are some inherent penalties associated with the serial scan. These penalties include: 1) performance overhead, 2) test data volume, 3) test power consumption, and 4) test application time. The performance overhead of serial scan is due to the scan multiplexer. The scan multiplexer falls into each clocked path and adds performance penalty of approximately two gate-delays. A circuit without scan design and with scan design is shown in Figure 1. As it is observable in Figure 1a, the critical path of a sequential circuit without scan insertion is decided by the longest combinational path between two flip-flops. However, in a scan inserted sequential circuit (see Figure 1b) the same critical path is elongated by a scan multiplexer at the end of the combinational path. The scan design also adds an extra fan-out at the output of a flip-flop. Both of these factors increase the critical path delay, hence reduces functional clock speed by 5% to 10%. This makes it necessary to eliminate the performance overhead of the scan multiplexer. Several solutions have been proposed to alleviate the performance penalty of scan design. One such solution that alleviates the performance overhead, as well as the other penalties associated with the serial scan design is the use of partial scan instead of full scan. In partial scan design, only a subset of all flip-flops in Circuit-Under-Test (CUT) are replaced by scan flip-flops to form a scan chain. This subset does not include flip-flops of the critical paths, hence reduces the performance penalty of scan. Additionally, the partial scan design techniques also reduce test data volume and test application time which are directly related to test cost. However, the partial scan design techniques may lead to lower fault coverage of the CUT. The selection of flip-flops to be included into partial scan design can be testability measures based, structure-based, or ATPG based.

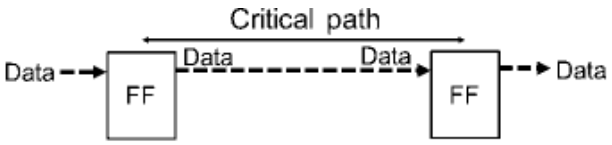

Figure 1: (a) Critical path of a sequential circuit

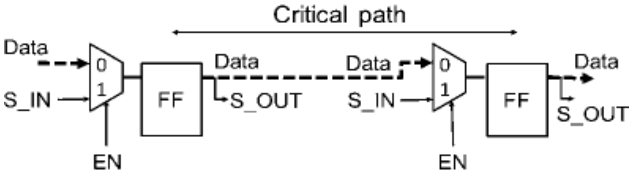

Figure 1: (b) Critical path after scan insertion

The structure-based techniques select flip-flops to cut-off the feedback path. These techniques make use of heuristics

based on network topology for selecting a minimum set of flip-flops and do not explicitly analyze the circuit behavior. The ATPG based techniques select flip-flops that are useful for test generation. These techniques first use sequential ATPG to generate test vectors for all possible faults. For the faults which remain undetectable, the related flip-flops are found and these are included in partial scan design. Most of the partial scan techniques require computationally demanding sequential ATPG, and cannot be afforded with ever increasing circuit complexity. Furthermore, partial scan design techniques do not provide high fault coverage as provided by the full scan design, and it is difficult to integrate them into the existing industrial design flow.

MTcmos:

Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with the multiple threshold voltages (V_{th}) in order to optimize delay or power. The V_{th} of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low V_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low V_{th} devices have substantially higher static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage by 10 times compared with low V_{th} devices.

One method of creating devices with multiple threshold voltages is to apply different bias voltages (Vb) to the base or bulk terminal of the transistors. Other methods involve adjusting thegateoxide thickness, gateoxide dielectric constant (material type), or dopant concentration in the channel region beneath the gate oxide.

A common method of fabricating multi-threshold CMOS involves simply adding additional photolithography and ion implantation steps. For a given fabrication process, the V_{th} is adjusted by altering the concentration of dopant atoms in the channel region beneath the gate oxide. Typically, the concentration is adjusted by ion implantation method. For example, photolithography methods are applied to cover all devices except the p-MOSFETs with photoresist. Ion implantation is then completed, with ions of the chosen dopant type penetrating the gate oxide in areas where no photoresist is present. The photoresist is then stripped. Photolithography methods are again applied to cover all devices except the n-MOSFETs. Another implantation is then completed using a different dopant type, with ions penetrating the gate oxide. The photoresist is stripped. At some point during the subsequent fabrication process, implanted ions are activated by annealing at an elevated temperature. In principle, any number of threshold voltage transistors can be produced. For CMOS having two threshold voltages, one additional photo masking and implantation step is required for each of p-MOSFET and n-MOSFET. For fabrication of normal, low, and high V_{th} CMOS, four additional steps are required relative to conventional single-V_{th} CMOS.

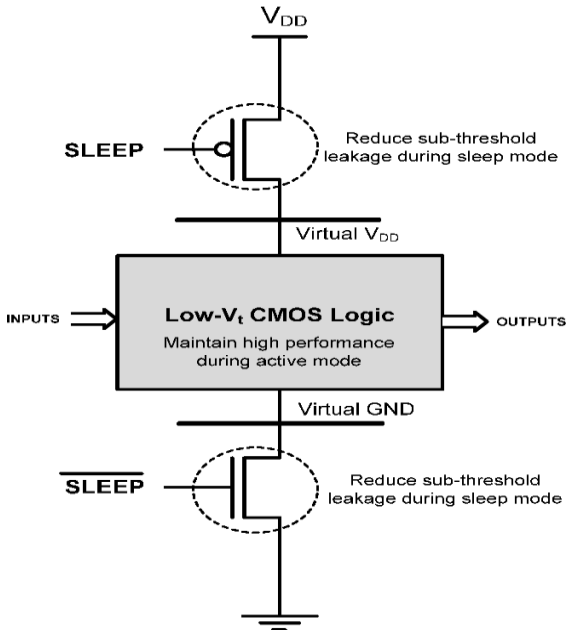

Figure 2: General MTCMOS circuit architecture

2. Analysis

Dealing With VLSI Circuits:

Digital VLSI circuits are predominantly CMOS headquartered. The best way average blocks like latches and gates are implemented is exceptional from what pupils have obvious so far, however the behavior remains the same. The entire miniaturization includes new matters to keep in mind. Plenty of thought has to go into precise implementations as well as design. Let us seem at some of the factors concerned.

a) Circuit Delays:

Significant complex circuits going for walks at very high frequencies have one colossal situation to tackle-the difficulty of delays in propagation of signals via gates and wires. Even for areas a number of micrometers throughout! The operation velocity is so large that as the delays add up, they are able to honestly become comparable to the clock speeds.

b) Energy:

Yet another result of high operation frequencies is improved consumption of power. This has two-fold influence-gadgets eat batteries rapid, and warmth dissipation raises. Coupled with the fact that surface areas have decreased, heat poses a primary danger to the soundness of the circuit itself.

c) Layout:

Laying out the circuit accessories is mission long-established to all branches of electronics. What's so specified in our case is that there are many possible methods to do this; there can be a couple of layers of exceptional substances on the same silicon, there will also be special preparations of the smaller elements for the identical element etc. The vigor dissipation and pace in a circuit present a exchange-off; if we try to optimize on one, the opposite is affected. The option between the 2 is set b the best way we chose the design the circuit components. Design may additionally influence the fabrication of VLSI chips, making it either convenient or difficult to put in force the add-ons on the silicon.

3. Proposed Work

1) *Gate-Leakage Current in a Single Transistor*

There are many published studies concerning gate currents in MOS transistors. In this work we consider only the parameters that affect the magnitude of gate-current in a transistor as it operates in relation to other transistors at the circuit level. We are assuming that Vdd, Vt, and the oxide thickness are fixed and depend on the technology used. Variables considered are the applied bias, the transistor type (NMOS or PMOS), and the transistor size.

The magnitude of the gate-current is a strong function of the applied bias. Since the gate-current is a static leakage current, we will consider the transistors at steady-state, i. e., in-between transitions only and not during transient switching. In general, a transistor in a static CMOS logic gate will be operating in one of 3 regions of operation, each with a significantly different amount of gate leakage: – Strong inversion, with |VGS| = Vdd. Gate-leakage current density for an NMOS in strong inversion can be as high as 103 A/cm2 for an oxide thickness. For an NMOS device, there is no leakage if Vdrain = 0 V. However, if the drain is pulled up to Vdd, a small leakage component in the reverse direction (from drain to gate) may be present, due to the gate-drain overlap area. This current depends of course on the transistor geometry, and is around 10 orders of magnitude smaller than the gate-leakage current in the strong inversion case. The above 3 regions represent 3 distinct conditions or states for the channel of a MOS transistor. Whether an "on" transistor will operate in strong inversion or at the threshold is determined by its position inside a structure, as well as by the states of other transistors in the structure.

2) *Transistor type:*

PMOS transistors in a static CMOS pull-up structure will also be operating in one of the same three modes as their NMOS counterparts. However, the main tunneling component in a PMOS device in inversion is hole tunneling from the valence band, as opposed to electron tunneling from the conduction band in NMOS devices, which results in PMOS gate currents being roughly 10 times smaller than NMOS currents. This fact has important implications in assessing a static CMOS structure from a gate leakage point of view.

3) *Transistor size:*

Since gate leakage currents are measured as current densities, it follows that the leakage current will be directly proportional to the gate area (W. L). Transistor sizing therefore has a direct impact on the amount of gate leakage in a CMOS circuit in static CMOS structures, the signals at transistor gates will always be strong (forcing), coming from either a signal source, or a previous output. In estimating the amount of gate-current in a given CMOS structure, we can therefore assume that a minimum-size transistor in strong-inversion will lead a specific amount that can be measured for a given technology, at a specific oxide thickness, with |VGS| = Vdd. Without loss of generality, we will consider that a PMOS transistor leaks exactly one tenth the amount in an NMOS.

4) *Structure Dependence*

The position of a specific transistor in relation to other transistors in a given structure will determine whether it will operate in strong inversion or at the threshold when switched on. In the following analysis, we will assume that the gate-leakage is significant only if a given transistor is operating in strong inversion.

3.1Structure-dependent channel states

An NMOS transistor will be in strong inversion when its source is pulled to ground either through a direct connection or through another NMOS device. This is the default state of an "on" transistor. Alternatively, the drain may be pulled low (through another device). Also, the NMOS transistor will be in strong inversion if the gate is high, with both the source and drain floating low and the substrate grounded. In general, an NMOS will be in strong inversion when switched on unless the channel is actively pulled towards Vdd, as in the following.

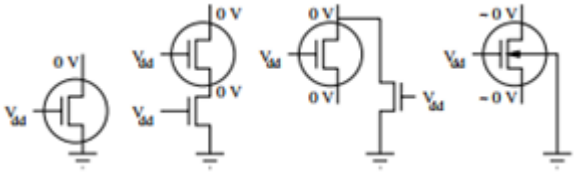

Figure 3: NMOS Inversion

An NMOS transistor will be operating at the threshold when the drain is pulled high through the PMOS pull-up network. This usually occurs when the transistor is in a stack, with one or more transistors in lower positions turned off. Depending on the transistor's position in the stack, the voltage at the drain may be either Vdd or Vdd −Vt. Alternatively, in more complex structures, the source of the transistor may be pulled to Vdd − Vt through another NMOS device.

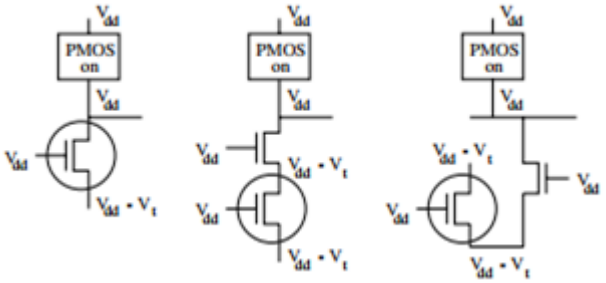

Figure 4: Pull up logic

The above structure-dependent transistor states can be re-iterated as follows:

- An NMOS transistor which is turned on (its gate is high) and whose drain or source is connected to ground (either directly or through a path of "on" transistors) will be in strong inversion and will leak.
- In a static CMOS gate whose output is high, any NMOS transistor which is turned on (its gate is high) and whose drain or source is connected to the output of the logic gate (either directly or through a path of "on" transistors)

will not leak. Such transistors will be in the threshold mode.

- The higher up an NMOS is in a stack, the lower the chances that it would leak (strong inversion), because there are fewer transistors which, if turned on, would cause it to be in the threshold mode.

Comparing NOR and NAND structures

The above observations are clearly illustrated in NMOS NOR and NAND structures. In a NOR-gate, each NMOS transistor will leak when turned on, independently from others. In that sense, the NOR structure is a 'worst case' structure. In the NAND structure however, we find that transistor B is at the threshold if A is off and C is on. Note that when A is off the output node is high. Transistor C leaks in only one case, when all three transistors are on. The different leakage states in the NOR and NAND pull-down structuresfor all input combinations. It is evident that a NAND structure (stacked NMOSes) will leak less that a NOR structure (parallel NMOSes) in 3 out of 8 possible cases, corresponding to the inputs (A, B, C) = (0, 0, 1), (0, 1, 1), and (1, 0, 1).

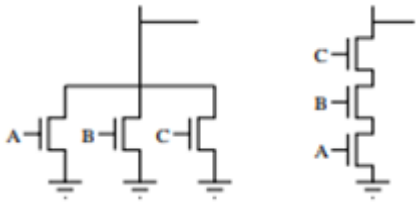

Figure 5: NOR and NAND structures

Logically equivalent structures

Structure-dependent channel states are useful for comparing different implementations of the same logic function. Considering the two logically equivalent structures shown in Fig.6, it is clear that the first structure leaks more than the second structure, because of the parallel transistors connected to ground, which will always leak when switched on. In the second structure, any or all of the parallel transistors may be on, however there will be practically no gate leakage through all these devices when the bottom transistor is off. Note also that both pull-up structures for this circuit are identical, making the second structure overall better from the point of view of gate-leakage.

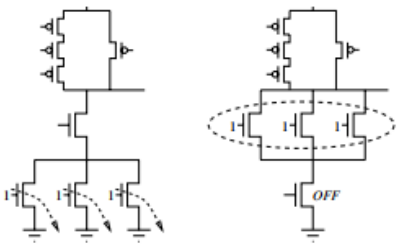

Figure 6: Similar operation

State-dependent leakage

Considering all the possible states of a 2-input NAND gatewe find that the leakiest state corresponds to the inputs (1, 1) (2 NMOSes leaking, case 4 in the figure). The following state corresponds to the inputs (0, 1) (1 NMOS and 1 PMOS leaking), followed by the state corresponding to the inputs (0, 0) (2 PMOSes leaking). The least leaky state occurs when the inputs (1, 0) are applied, in which case only one PMOS transistor is leaking.

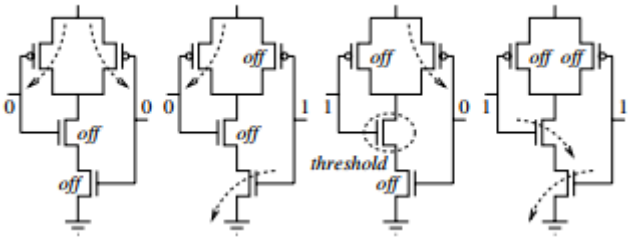

Figure 7: States of 2 input NAND gate

Outputs

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter Schematics, perform SPICE simulations, do physical design (i. e., chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks. There are 3 tools that are used for this process:

S-edit-a schematic capture tool
T-SPICE-the SPICE simulation engine integrated with S-edit
L-edit-the physical design tool
Using S-Edit (Schematic Entry Tool) & T-SPICE (Analog Simulation Tool)

Example: IV Curves of an NMOS Transistor

S-edit is a schematic entry tool that is used to document circuits that can be driven forward into a layoutof an integrated circuit. It also provides the ability to perform SPICE simulations of the circuits using a simulation engine called T-SPICE. T-SPICE can be setup and invoked from within S-edit.

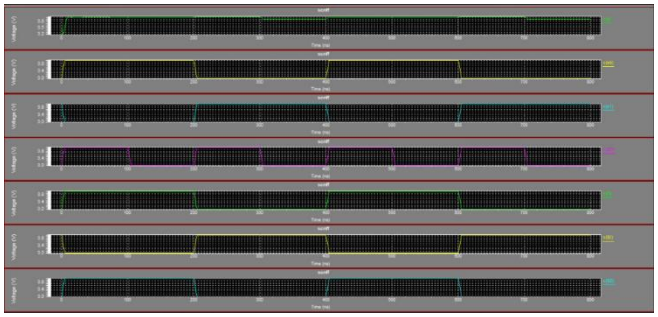

Figure 8: Output wave forms with tanner tool

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MEASUREMENT RESULTS

TRAN_Measure_Delay_1 = -9.2752e-008

TRAN_Measure_Delay_2 = 7.2480e-009
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Figure 9: Transistor measurements

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Power Results
VVoltageSource_5 from time 0 to 8e-007
Average power consumed -> 1.013170e-007 watts
Max power 1.030741e-004 at time 3.76109e-009
Min power 1.097634e-010 at time 6.91218e-007
```

Figure 10: Power results

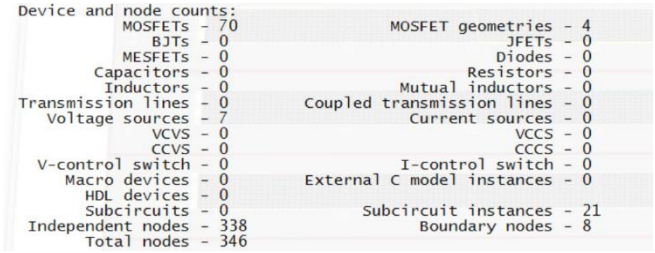

Figure 11: Device and Node counts

4. Conclusion

We have proposed a new design of scan flip-flop which eliminates the unnecessary power dissipation in the combinational circuit as well as the flip-flops during serial scan of test vectors. Our circuit provides a way of output gating wherein the test vector response is retained in the flip-flops after the capture cycle. The proposed solution has little impact on the performance with power reduction to a large extent during testing. We then considered specific combinations of transistors to illustrate the structure dependence of the leakage current. Structure dependence is used as the basis for designing low gate-leakage gates. We then considered the state dependence of the leakage current through state-dependent leakage tables, which can be used for a proper pin assignment if the input signal probabilities are known, as well as to estimate the total power lost due to gate-leakage in a large multi-gate circuit. Finally, we presented recommendations and design guidelines that summarize the main points of the paper. Furthermore, the proposed scan flip-flop can be used both as a serial scan cell as well as a RAS cell, in the mixed mode scan test. The mixed mode scan design implemented with proposed scan flip-flop shows a promising reduction in interconnect wire length, test data volume, and test application time

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