International Journal of Science and Research (IJSR)
ISSN: 2319-7064
SJIF (2022): 7.942

Review for Design Considerations of SAR ADC in CMOS 32 NM Technology

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Abstract: ***Analog-to-Digital Converters (ADCs) are key components for the design of power limited systems, in order to keep the power consumption as low as possible. Among all ADCs, Successive Approximation Register (SAR) ADCs are mostly used due to their simpler structure, fewer analog blocks, smaller area, and lower power consumption. This review paper is focuses on a study to summarize developments in SAR based ADC. It also focuses on the new CMOS 32nm technology and on some major designing components, parameters like area, power, current and techniques analysis like parametric, delays, speed critical paths and cross talks while designing a SAR ADC.***

Keywords: ADC, SAR, CMOS 32nm Technology, Low power, comparator, sample-and-hold

1.Introduction

Analog to Digital Converters (ADCs) are important components of the day- to day communication and signal processing area [1] [2]. ADCs translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems [5]. Among the all ADCs, the most generic option for choosing an ADC could be Flash type ADC as it uses (2n-1) comparators. But the high number of comparators makes the architecture more power hungry even for low resolutions [4]. In the same manner, the pipeline ADC architecture is not a suitable for ultra-low-power as each stage uses an active gain element whose power equals the one of many comparators. The sigma-delta and the time interleaved have similar limit because of their speed or multiple paths to increase resolution, they use active power hungry elements [4] [5] [8] [10]. On the other hand, successive approximation register (SAR) ADCs have a decent conversion speed and take small overall chip area in comparison and is suitable for low or medium to control a DAC in a feedback loop with a single comparator [1] [3].

CMOS has been the dominant technology for VLSI implementation [5]. The development in CMOS technology is characterized by the minimum feature size, power dissipation, maximum operating frequency, number of gates on chip, die size etc. [4] [5]. Over the time, because of the advancement in CMOS technology, more and more functions are fabricated with higher density that results in transforming the system becoming more compact throughout [2] [3]. In this proposed work, we proposed the physical design of SAR based ADC using MCOS 32 nm technology. Here we proposed new architecture cum design for SAR logic as Up-down counter that help in good accuracy and stability.

2.CMOS 32 NM Technology

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area [14] [15]. Due to the advantage and current demand in CMOS technology, the effort has been taken to design proposed SAR based ADC using 32 nm Technology. The main novelties related to the 32 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 32 nm technology is 25nm. Some of the key features of 32 nm technologies from various providers like TSMC, Fujitsu, and Intel are as given below [14] [15].

Table 1: Key Features of 32 nm Technology

Sr. No.	Parameter	Value
1	VDD (V)	0.85-1.2 V.
2	Ioff N (nA/um)	5-100
3	Ioff P (nA/um)	5-100
4	Gate dielectric	SiON, HfO2
5	No. of metal layers	6-10
6.	VTHO	0.250V
7.	TOXE	1.00

Compared to earlier 45 nm technology, 32 nm technologies will offer:

- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

3.SAR ADC

The SAR-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and logic control unit.

A. Sample and Hold Circuit: A sample and hold circuit is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time. A sample and hold circuit is to acquire the input voltage (V_{in}).

B. Comparator: Comparator is widely used in the process of converting analog signals to digital signals. In the A/D conversion process, it is necessary to first sample the input. This sampled signal is than applied to a combination of comparators to determine the digital equivalent of the analog

signal and it compares the analog signal with another reference signal. Outputs are binary signal based on the comparison.

C. Successive Approximation Register (SAR): A successive-approximation ADC uses a comparator to successively narrow a range. At each successive step, the converter compares the input voltage to the output of an internal DAC. At each step in this process, the approximation is stored in a SAR. SAR ADCs have a decent conversion speed and take small overall chip area in comparison to flash ADCs.

D. Digital to Analog Converter: An internal reference DAC that, for comparison with VREF, supplies the comparator with an analog voltage equal to the digital code output of the SAR input.

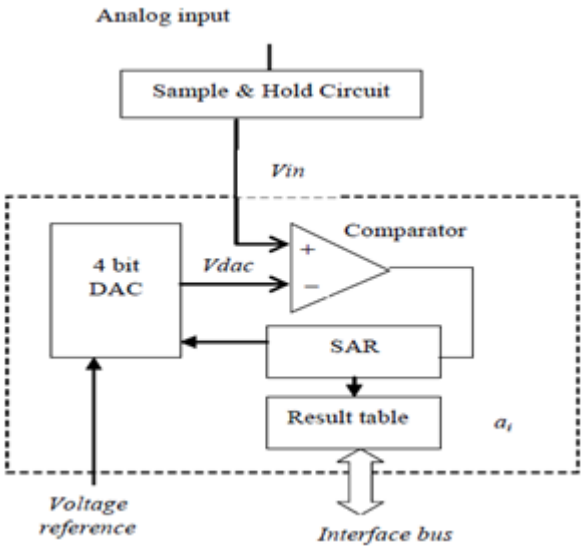

Figure 1: Block diagram for the SAR ADC

4.Working of SAR Algorithm

The SAR algorithm works by switching on a large voltage and comparing that to the input voltage. If the switched voltage proves higher than the input voltage then the algorithm turns off that voltage and turns on a voltage half that size and repeats. If the voltage comes up lower than the input voltage it keeps that voltage on and then adds a voltage that represents half the size of the first voltage and repeats. This then corresponds to a series of 1s and 0s. These values are known as bits with the first voltage that is turned on corresponding to the most significant bit (or MSB) and the last voltage corresponding to the least significant bit (or LSB).

When the algorithm finishes the result is a binary code that corresponds to the input voltage. This process is referred to as successive approximation. The code produced results in a readable data form for a computer or micro-controller. Figure 2 below shows the basics of how the algorithm works where VREF represents the max voltage that the SAR ADC can measure.

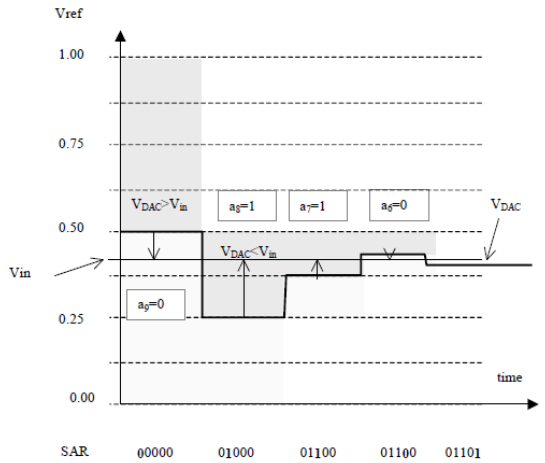

Figure 2: Example of the SAR working [10]

5.Literature Review

The recent development in CMOS SAR ADC made to reduce the power consumption and increase efficiency. Many researcher have propose different architecture, solutions and methods of their own for minimizing power, reducing complexity or increasing efficiency.

Devitha P.S, & Anuja George in 2019 [1] proposed Low power high speeds ADC [1] can be design using VLSI. They have implemented ADC design suitable for standard CMOS technology with low power low-cost VLSI implementation. The power consumption of the ADC is 2.59 mW at 1.2V supply.

Vijay Pratap Singh, Gaurav Kumar Sharma, Aasheesh Shukla in 2017 [2] presents Successive Approximation Register (SAR) Analog to Digital Converter (ADC) is designed using non redundant SAR structure and sequencer/code Register structure for low power operation using 90 nm CMOS Technology. The designed ADC structures provide optimum results for all three circuit design challenges: speed, area and power.

Prof. Chandrakant S. Ragit & Dr. Sanjay S. Badjate in 2016 [3] proposed up down counter as Successive Approximation Register using 45nm tehnology. They suggested the SAR logic for ADC that is one of the best suited for low power. Here the resolution proposed is 4- bit and a power consumption of few mill watts.

Hur A. Hassan, Izhal Abdul Halin, Ishak Bin Aris, Mohd Khair Bin Hassan in year 2009 [4] have proposed successive approximation analog to digital converter implemented in a conventional 0.18u CMOS technology with low power. They have designed SAR with composite of sample and hold dummy switch compensation, comparator with low voltage latched and realized based on current mode approach, control logic circuit and DAC as binary weighted capacitor arrays for the differential inputs.

Siamak Mortezapour [5] presents ADC designed for low-power, medium-quality applications such as data acquisition. The requirement is usually to integrate these ADC's with digital signal processors (DSP's) in a low-cost CMOS

technology. ADC's that are integrated with a DSP are required to operate in the same range of supply voltage.

A. R. Kasetwar, & V.G.Nasre in 2011 [6] provided a re-view data for understanding the design of SAR based ADC. They have done rigorous data collection on the design terminologies, CMOS technologies and Successive Approximation Register (SAR) based ADCs used in low power, high resolution area efficient circuits and the recent development in CMOS SAR ADC is distinctive in the denomination of architecture and its performance.

Hassan Sepehrian, Mehdi Saberi, and Reza Lotfi [7] presents a modified structure and a new switching algorithm in successive-approximation analog-to digital converters to reduce the power consumption. This technique is more efficient in applications where the input signal activity is low most of the time such as biomedical signals. For slow-varying samples, only the least significant bits of the new analog sample are extracted leading to power saving in both the capacitor-based DAC and the comparator.

Zhangming Zhu, Zheng Qiu, Maliang Liu, and Ruixue Ding [8] proposed an asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) for sensor applications. They proposed low leakage latched dynamic cell in SAR logic and wide range configurable delay element extend the flexibility of speed and resolution tradeoff. The ADC fabricated in 0.18 CMOS process covers 6–10 bit resolution and 0.5 V–0.9 V power supply range.

Mon Mon Thin, Myo Min Than, and Theingi Myint [9] describes a successive approximation ADC that uses a charge-redistribution digital- to-analog Converter (DAC) designed to achieve a good accuracy and high speed. They proposed the new algorithm of SAR ADC which can reduce the number of conversion step is proposed. This algorithm enhances the speed of SAR ADC system that to be apply in high speed application.

Ms. Kiran P. Kokate1, Prof. A. O. Vyas [10] implemented Successive Approximation analog-todigital converter (ADC) in a conventional 90nm CMOS technology with low power consumption. They came across results as sampling frequency of the ADC IS 2.1GHz. CMOS layout and simulation is drawn by using Microwind 3.1 software. Nilofar M. A. Shaikh, Prof. Seema H. Rajput [11] opted to implement a Successive Approximation Register (SAR) ADC that is one of the best suited for low power. They targeted a resolution of 4-bit and a power consumption of few mill watts. The SAR ADC is implemented in 45 nm CMOS technology with a power supply of 1V.

Anuradha S. Kherde, Pritesh R. Gumble [12] provides a detailed view of a 4 bit R2R ladder with optimum accuracy by using Microwind 3.1. This paper provides a detailed view of a 4 bit DAC with optimum accuracy by using Microwind 3.1. For all about Pre Layout simulation has been realized using 90 nm (0.09um) CMOS process Technology.

Ms. Kiran P. Kokate1, Prof. A. O. Vyas [13] designed and implement a successive approximation register (SAR) analog to digital converter (ADC) for communication domain using CMOS layout and simulation is drawn by using Microwind 3.1 software.

6.Problem Definition / Formulation

Power consumption is very crucial in CMOS technology design. In this project we are going to design the physical of Up Down counter based SAR based ADC architecture for optimization using 32 nm CMOS technology. While lower the CMOS technology, we need to think about the MOS modelling techniques. There are three MOS modelling techniques available out of which BSIM4 MOS modelling is applicable for CMOS technologies below 90 nm.

The goal is to reach a total power consumption of few µ-Watts as compared to the earlier design proposed by researcher. The final design of will be with consideration of all physical optimization parameters including area, power, current and analysis like parametric, delays, speed critical paths and cross talks.

7.Proposed Work

The proposed work is to design the SAR counter logic by simplest method, an Up/down counter to control DAC o/p. It works by starting by binary o/p 8(1000) and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments. The counter o/p and Vin is compared using comparator which gives the value of that count directly. The comparison is performed for the next count, and so on until all count are checked for below or greater than value 8. The conversion would start with SOC signal and cycle finishes after 8 clock cycles, with active low EOC output. The Iterative algorithm for ADC conversion for up-down counter as SAR logic is given in figure 3.

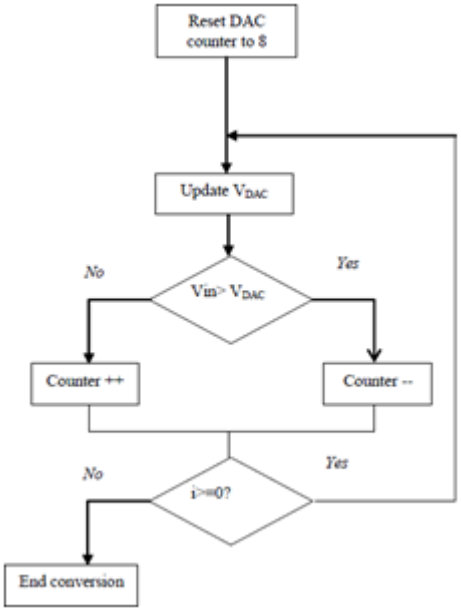

Figure 3: Iterative algorithm for ADC conversion

The complete process is faster than the iterative converter as only N comparisons are necessary. The algorithm is showed in detailed in figure 3.

The physical design of all sub-components as Sample and Hold Circuit, Comparator, up-down counter based Successive Approximation Register (SAR) and Digital to Analog Converter is implemented using CMOS Microwind EDA tool and at the end all physical designs are merged on the same substrate in order to get the final ADC. The care is taken for power optimization.

8.Conclusion

Recent progress in CMOS 32 nm and on the SAR-ADC architecture and performance was reviewed. SAR ADC is one of the most efficient ADC available. This is because of its Power efficiency, complexity, conversion rate better than conventional Flash, Delta-sigma or Dual slope ADCs. This impacts the overall efficiency and its flexibility. This paper stated ADC's basic architecture which are Sample and Hold circuit, Comparator, Up-Down as SAR logic and DAC. The schematic logic structure of SAR ADC will be built by DSCH software to verify its feasibility. The CMOS level circuit will be designed and simulated and simulation verification with Microwind EDA tool with 32nm CMOS technology.

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