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High Speed Low Power 8-Bit Binary up Counter in 45nm CMOS Technology

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Abstract: ***This article presents the schematic design of a new 8-bit binary counter. The 8-bit binary counter is designed to achieve lower power consumption with high-speed operation. Circuit level simulations are done to check the circuit functionality and the layout is made by connecting the components manually. At last, the layout is simulated to know whether the output signal is affected by parasitic resistance and capacitance. Test structures of the Counter are designed using 45 nm Technology with Tanner EDA environment. Thus, the proposed circuit is designed and implemented to overcome these limitations.***

Keywords: Power dissipation, lower offset voltage, binary up counter, Tanner EDA tool

1. Introduction

Integrated circuit (IC) is manufactured by placing thousands of transistors into a single chip. The number of applications of integrated circuits is in the fields of high-performance computers, telecommunications, and consumer electronics. The required computational power (or the intelligence) of these applications is the driving force the fast development of this field. As more and more complex functions are required in various data processing and telecommunications devices, the need to integrate these functions in a small system/package is also increasing.

Prior to the initiation of VLSI innovation, most of the ICs perform on restricted set of capability. A hardware circuit might comprise of different parts like ROM, Smash, computer processor etc. VLSI allows IC originator to add every one of these into single chip. With the headway in the VLSI plan, more transistors are added, and as an outcome, more individual capabilities or framework were coordinated over the long run. The principal IC held a couple of gadgets, upwards of ten diodes, transistor, resistor, and capacitor; subsequently manufacture one or more logic gates.

Hardware can be made smaller to use less space and power. As a result, there is a growing need for batteries with smaller sizes and longer lives. The main goal of a VLSI designer is to minimise leakage current and leakage power dissipation to improve functionality and battery longevity.

Leakage power in CMOS circuit is because of dynamic power dissipation which increases with the reduction of threshold voltage, thickness of gate oxide and channel length. The average power dissipated in any logic circuit is given by [2]

$$P_{Total} = P_{Dynamic} + P_{SC} + P_{Static}$$

$$P_{Total} = \mathrm{K}CV_{dd}^2 f_{sw} + I_{sc}V_{dd}\, t_s f_{sw} + P_{Static}$$

Where,
K- technology factor,
C- capacitance of switching node,
V_{dd} - supply voltage,
f_{sw} - effective switching frequency,
I_{sc} - short circuit current,
t_s - switching delay

2. Literature Survey

- Utilizing Cadence Virtuoso's UMC CMOS 180nm technology, the MOD-13 down counter's design was successfully realised. The counter begins counting at 14 (1110_2) and stops at (0010_2). The triggers begin to malfunction, and the output signals get distorted when the clock frequency is higher than 1.4 GHz, which is the maximum working frequency that is permitted. [1]
- Design and simulation are used to create a 3-bit asynchronous up counter with a high area and speed \ the NAND gate design, 14 transistors are utilised, but only 6 transistors are used in pass transistor logic. Thus, the final circuit for a barrel shifter that employs a standard design, or one that uses a universal gate, takes 56 transistors and has a longer delay. However, the suggested barrel shifter utilises 24 transistors in total, using less power and with less latency. The percentage reduction. Therefore, it can be said that the suggested barrel shifter is superior to the traditional circuit. [3]
- For traditional and modified 1-bit Full Subtractor circuits in 65nm technology, the Microwind / DSCH tool is used to examine the decrease in average power that results in the reduction of leakage current and dynamic power dissipation as well as area, delay, and Power Delay product. In 65nm technology, proposed 1-bit Full Subtractor circuits are studied for power consumption, area, delay, and power delay product at various supply voltages at room temperature. It is discovered that the suggested design using the MTCMOS approach consumes less power overall than both the proposed circuits with twenty and fourteen transistors and traditional static mode. Therefore, the MTCMOS technique's Fourteen transistor One Bit Full Subtractor is Energy Efficient since its PDP value is lower. [4]
- The implementation, simulation, and analysis of synchronous 4-bit up counters. In terms of space, delay, and power consumption, the counter's performance is evaluated. Utilizing the sea of gate arrays concept and the Cadence tool, the layout optimization objective is successfully completed. With the help of the simulation results, the logic and properties of the synchronous 4-bit up counter and master-slave D flip-flop can be easily validated. As a result, we propose the synchronous 4-bit

up counter design and implementation, which is area-optimized. [5]

- The most common ratioed logic circuit uses a 4-input NAND gate using pseudo-NMOS logic gates, which demonstrates how such designing can reduce area, input capacitance, and component count. However, it also increases power dissipation and increases delays when compared to conventional CMOS, so ratioed circuits can be used in situations where smaller areas and lower input capacitance are required. [6]
- A transistor gating method that lowers the complete subtractor's power dissipation. Performance is improved, and power consumption is decreased, through CMOS technology. According to the simulation results, we were able to minimise leakage current by 17.58% and leakage power by 24.38% after using this approach. By using the Cadence simulation tool in 45nm CMOS technology at 0.7 supply voltage, the results for a complete subtractor are simulated. [7]
- A high-speed parallel counter with scalability made with digital CMOS gate logic components. The sole components of counter design logic are three-input AND gates and 2-bit counting modules. The pipelined paradigm and state look-ahead path logic, whose interoperation activates all modules simultaneously at the system's clock edge, provide all counter state values at precisely the same time without rippling effects, are the counter structure's key features. Additionally, this design removes the need for a lengthy chain detector circuit, which is generally needed for wide counters. All early overflow states for modules of greater significance are produced by an initial-bit counting module, which also pre-scales the counter size. By applying modern circuit design approaches, the gate count on all timing routes is reduced to two gates, significantly increasing the counter frequency. To align all modules in vertical columns with the system clock, further considerations must be taken during synthesis or layout implementations. This design stays within setup and hold times, which may ultimately be constrained by race conditions. [8]
- A parallel counter based on a brand-new state look-ahead mechanism and a frequency divider for high speed is both described. The divider structure, which offers a range of frequency dividing factors from 2 to 255, is implemented for an 8-bit data size. For our CMOS implementation, the M-bit frequency divider measures a delay of 3.5+log4 (M), which is only five gates delay at a maximum frequency dividing factor N=256. Additionally, the 8-bit divider uses 9600μm^2 of silicon and has 508 total transistors. According to the results of the HSPICE simulation, the divider operates at a frequency of 2GHz and dissipates 16.78mW of power at worst-case process corners when utilising 0.15m TSMC CMOS technology. [9]
- This study presents the design of a high-speed up/down counter using digital CMOS gate logic components. The counter design is based on a straightforward circuit implementation, but we used specially created cells to substitute important parts. The counter's chip was created using the TSMC 0.18-m CMOS process, and it has an 80 by 100-m core area. The measured results demonstrated that the counter could operate satisfactorily at 1.6GHz clock frequency and 7.7mW power dissipation. [10]

3. Methodology

To design a Binary Up Counter with reduced power consumption and low kickback.

A counter is a piece of digital logic equipment used in computing that continuously records and shows a certain event in line with configuration and programming. A sequential digital logic circuit, which has a single input line (the clock) and a few output lines, is a common type of counter.

The values on the output lines correspond to binary coded decimal (BCD) numbers. Flip-flops are frequently coupled in a cascade in these digital circuits. Both independently and in combination as parts of larger ICs and PCBs, these tools and devices are often used in digital circuits as ICs.

True Single-Phase Clock (TSPC)

Traditional latches require complementary and genuine clock signals. The True Single-Phase-Clock (TSPC) circuit approach suits both static and dynamic CMOS circuits and uses a single clock signal that is never reversed. Dynamic logic is frequently used to construct edge-triggered D flip-flops in integrated high-speed processes. This means that when the device is not transitioning, the digital output is held on parasitic device capacitance. Since the reset operation may be carried out by merely discharging one or more internal nodes, this architecture of dynamic flip flops also permits straightforward resetting. The true single-phase clock (TSPC) kind of dynamic flip-flop is a popular version that operates at high speeds and with minimal power.

At low or static clock rates, however, dynamic flip-flops won't normally function because, given enough time, leakage routes may deplete the parasitic capacitance to the point that the flip-flop enters incorrect states.

Precharged p-and n-phases, as well as non-precharged (static) p-and n-stages, are the four fundamental stages in the TSPC D Flip Flop. These stages are precharged N (PN), precharged P (PP), non-precharged N (SN), and non-precharged P. (SP).

The construction of a falling edge triggered true single phase (TSPC) flip flop is shown in the accompanying image. By including a pmos pass transistor and an inverter at the very end to invert the D' logic into D, i. e., Q, this design offers a reset facility.

Operation of 8 BIT Upcounter

Compared to an asynchronous counter of the same range, its operating frequency is substantially greater. Additionally, because all flip-flops or counter stages are connected to a parallel clock source, which simultaneously activates all counters, there is no propagation delay with synchronous counters.

All D Flip-flops simultaneously receive the external clock in a parallel fashion. If we look at the circuit, the D pins of the first flip-flop, the least important bit in this 8-bit

synchronous counter, link it to an external Logic 1 input. This connection causes HIGH logic to be applied across the Logic 1 signal, which changes the first flip-state flops on each clock pulse.

The output of the first flip-flop is crossed by the input pins of the second flip-flop and output of the second flipflop is crossed by the input of the third flipflop and so on.

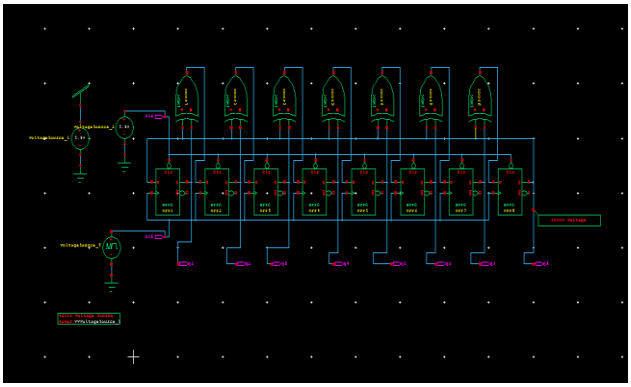

Figure 1.1: 8-bit up counter

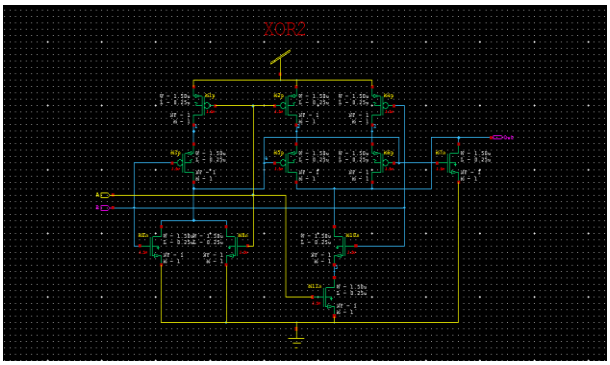

Figure 1.2: Xor gate Circuit

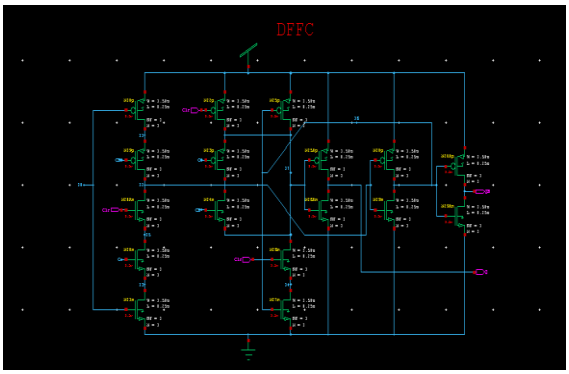

Figure 1.3: D Flip-Flop Circuit

Fig 1.1 shows the overall diagram of 8-bit counter using D flipflop. Fig 1.2 shows the transistor level diagram of Xor gate. Fig 1.3 depicts the transistor level diagram of D Flipflop.

4. Result

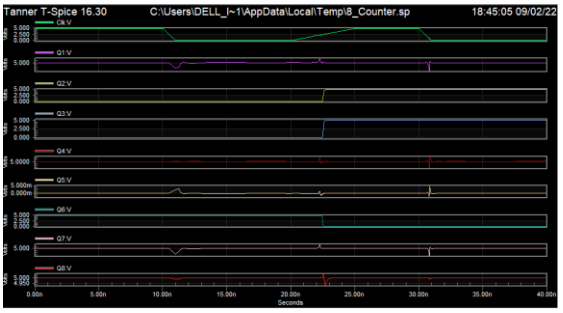

Figure 1.4: Simulation of 8-bit Up counter using 45nm Technology.

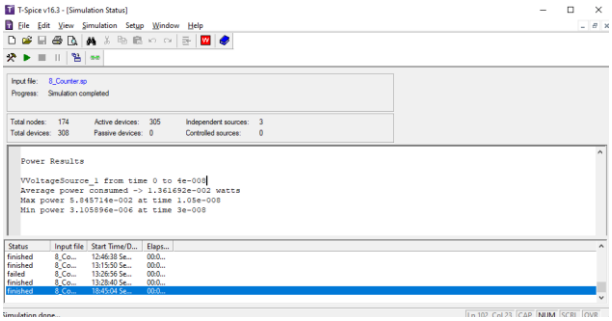

Figure 1.5: Power Analysis of 8-bit Up Counter using 45nm Technology

Fig 1.5 denotes the Minimum Power consumed is 1.361692e-002 watts. Fig 1.4 shows the waveforms of output of each flipflop.

5. Conclusion

Thus, a Binary Up Counter topology for low power and high-speed applications is presented. The circuit is designed and simulated in Tanner 45 nm Technology with Tanner environment. Test results will be obtained from the test structures designed for different parameters be obtained from the test structures designed for different parameters.

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