International Journal of Science and Research (IJSR)
ISSN: 2319-7064
SJIF (2020): 7.803

Design of 256 x 256 bit Vedic Multiplier

Aishwarya K M[1], Dr. Kiran V[2]

[1]Department of Electronics and Communication Engineering, R V College of Engineering, Bangalore, Karnataka, India

[2]Professor, Department of Electronics and Communication Engineering, R V College of Engineering, Bangalore, Karnataka, India

Abstract: ***Multilplication has turned out to be an important operation in many DSP based applications and processors. The design for an area efficient, high speed and low power circuits are the prime objective for most of the VLSI circuits today. This paper presents a design for the implementation of 256 x 256 vedic multiplier. The design was carried out by designing the vedic multiplier for lower bits and by designing adders required for the design. The design was synthesized and delay was tabulated for varios vedic multipliers. The tool used in achieving this is Vivado.***

Keywords: Urdhva Tiryagbhyam, Vedic mathematics, Vedic multiplier, Verilog

1. Introduction

Multiplication is an important arithmetic operation and is carried out in many applications. These applications include DSP applications, processors etc. Also modern VLSI technology has turned its focus onto low power, high speed and low area circuits. The regular methods may lead to operations than consume greater power or delay. So performing multiplication in an optimised way can help with these factors to a greater extent.

General classification of multipliers include – serial multiplier, parallel multiplier and serial parallel multiplier. The serial multiplier needs less area but is slow. Whereas parallel multiplier provides faster operation but is expensive interms of area. Therefore we go for a comination of both seial and parallel to get a tradeoff between area and performance [1]. In case of array multiplier, the product can be obtained with a single micro operation. Even though its efficient it has a requirement of large area. So as number of bits increases, array multipliers are not preferred. In case Wallace tree multiplier, carry save adders are used in the implementation to get the product. This also has a limitation on execution time when the number of bits in the multiplicand term increases [2]. Also the number of steps to obtain the product is also higher in these multipliers for higher bits [3].

Vedic multipliers are based on the Vedic Sutras. There are sixteen sutras which can be applied to mathematics. These will help to reduce the complex calculations and perform the calculations in an optimised manner. It is also preferred for its fast and low power nature as this a key concern now [4]. The 16 sutras include Anurupye Shunyamanyat, halana - Kalanabyham, Ekadhikina Purvena, Ekanyunena Purvena, Gunakasamuchyah, Gunitasamuchyah, Nikhilam Navatashcaramam Dashatah, Paraavartya Yojayet, Puranapuranabyham, Sankalana - vyavakalanabhyam, Shesanyankena Charamena, Shunyam Saamyasamuccaye, Sopaantyadvayamantyam, Urdhva Tiryakbyham, Vyashtisamanstih, Yaavadunam [4].

In this paper Urdhva Tiryakbyham sutra is used to design the 256 x 256 multiplier. For this, design of 2x2 vedic multiplier is done first, followed by 4x4, 8x8, 16x16, 32x32, 64x64 and 128x128 multipliers. Later it is simulated using Xilinx Vivado tool.

1.1 Urdhva Tiryakbyham

Urdhva Tiryakbyham means “veritically and crosswise” [2]. This principle is applied to multiplication to reduce the complexity of the operation. This makes it faster and easier, especially for the higher bits. This can be illustrated with the example of decimal number - 1252 x 1132. The number to be multiplied are written on two adjacent sides of the square. The square is divided into smaller blocks. These square contains the product and the carry term written as specified in the fig.1. After this, the digits are diagonally added and written as carry and the product term. Finally we get the product term.

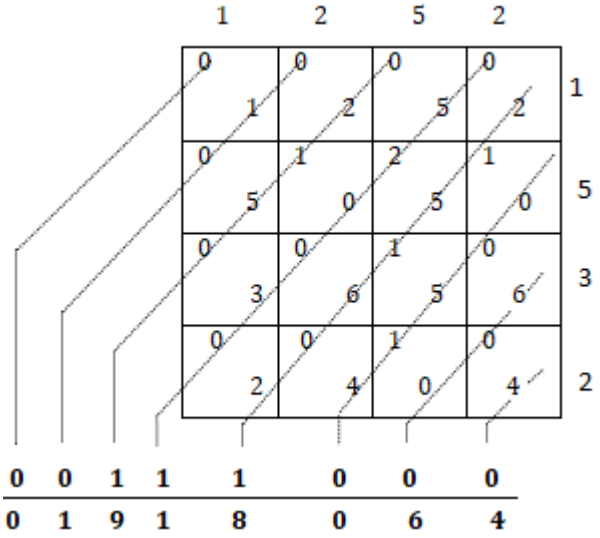


Figure 1: Multiplication of decimal numbers

2. Multiplication using Urdhva Tiryakbyham

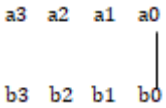
The multiplication using Vedic mathematics can also be extended to binary numbers. To illustrate this consider, an example to multiply a number a3a2a1a0 with b3b2b1b0. The example is multiplication of 4 bit binary word.

a3 a2 a1 a0

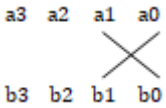
x

b3 b2 b1 bo

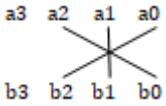
Step 1:



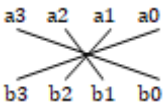
Step 2:



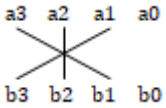
Step 3:



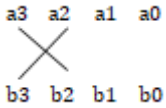
Step 4:



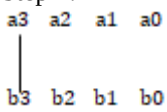
Step 5:



Step 6:



Step 7:



The above example clearly illustrates how the multiplication is carried out for a binary number containing 4 bits using Urdhva Tiryakbyham vedic method. From step we get the LSB of the product term P0 = a0*b0. Similarly we get the other terms as follows:

P1 = a0*b1 + a1*b0
P2 = a2*b0 + a1*b1 + a0*b2
P3 = a3*b0 + a2*b1 + a1*b2 + a0*b3
P4 = a1*b3 + a2*b2 + a3*b1
P5 = a3*b2 + a2*b3
P6 = a3*b3

By implementing vedic multiplier in circuits, the multiplication is performed efficiently and area is also optmised. From the above example, the final product will be P7P6P5P4P3P2P1P0, where P7 will be the carry term of P6.

3. Design of Vedic Multiplier

First, the 2x2 vedic multiplier is designed using two half adders and and gates. First the terms a0bo, b1a0, a1b0 and a1b1 are obtained using and operation. Later this is fed to the inputs of half adders as shown in fig.2.

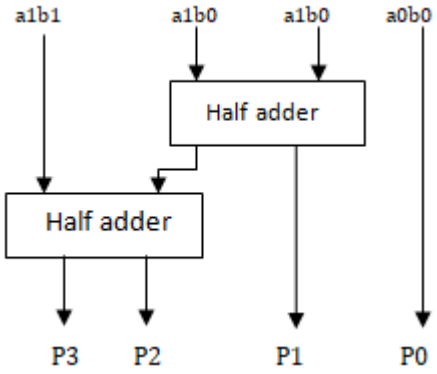


Figure 2: 2x2 vedic multiplier

Using the 2x2 vedic multiplier, 4x4 can be designed. Further using that, 8x8 can be designed. Thus a 64x64 vedic multiplier can be designed using four 32x32 vedic multipliers and a 64bit adder and two 96bit adders. The design is illustrated in fig.3.

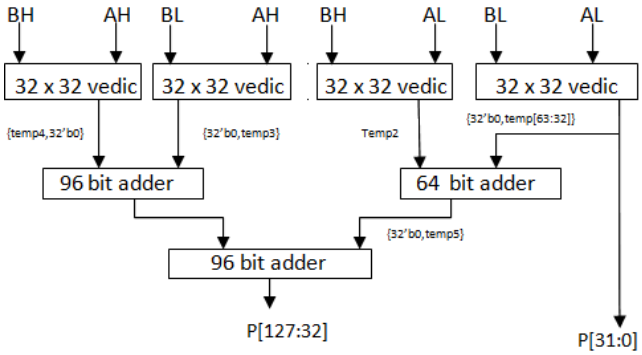


Figure 3: 64 x 64 vedic multiplier

To design a 64 x 64 vedic multiplier, four 32x32 vedic multipliers are used. Here AL is a0 to a31, i. e., lower 32 bits of the first number. Similarly AH is a32 to a63, BL is b0 - b31 and BH is b32 – b63. These are fed as input to the vedic multipliers as shown in figure. Finally we get a product which is 128 bits.

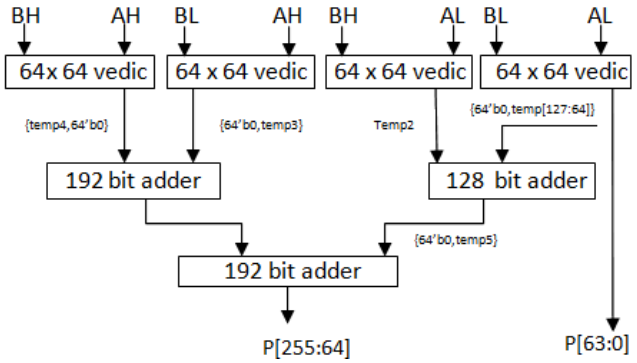


Figure 4: 128 x 128 vedic multiplier

Similarly 128 x 128 vedic multiplier can be designed as shown on figure.4. Here AL is the lower 64 bits of the number, AH is the upper 64 bits. Same is the case for BL and BH.

4. Design and Implementation of 256 x 256 Vedic Multiplier

256 x 256 bit vedic multiplier can be designed using four 128 x 128 bit vedic multipliers. Here apart from the vedic multipliers, the design requires three adders. A 256 bit adder and two 384 bits adder. The design is shown in fig.5 below.

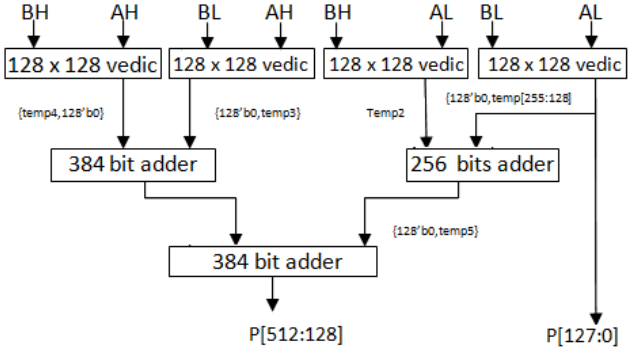


Figure 5: 256 x 256 vedic multiplier

For the design of 256 x 256 vedic multiplier, as shown in fig.5, lower 128 bits of the numbers are fed as input to the first multiplier. That is AL is a0 to a127. Also AH is the upper 128 bits, BL and BH are lower and upper 128 bits respectively. A 256 bits adder and 384 bits adders are used. Further optimisation of the design can be done by optimising the adders. This will provide an even more faster multiplication. In this design for the ease of designing, the adder was coded with a simple '+' operator. Adders like carry look ahead adder, carry save adder can give better performance [6]. In the design the results from 128 x 128 vedic multipliers are termed as temp1, 2, 3 and 4 accordingly. The product term will have 512 bits starting from P0 to P511.

5. Results

First the 2x2 vedic multiplier was designed and simulated. From that the higher bit multipliers – 4x4, 8x8, 16x16, 32x32 vedic multipliers were designed and simulated. The simulation was carried out in Xilinx Vivado tool. The figure 6 shows the schematic results of 32x32 vedic multiplier simulated in vivado.

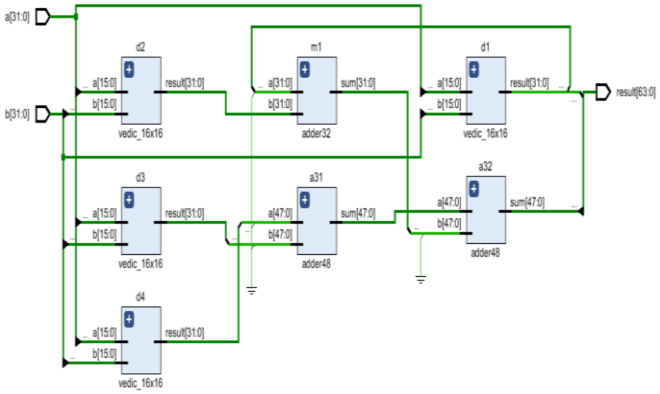


Figure 6: RTL view of 32x32 vedic multiplier

By nesting this module to the top module, 64x64 vedic multiplier was designed and simulated. The RTL view of 64x64 vedic multiplier is shown in fig.7.

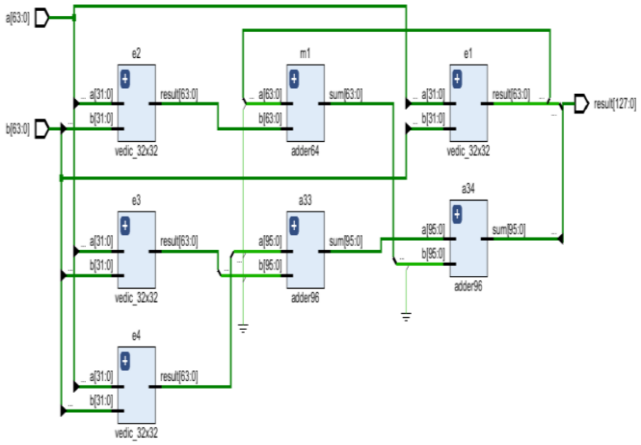


Figure 7: RTL view of 64x64 vedic multiplier

128x128 vedic multiplier was designed and simulated by nesting the module of 64x64 vedic multiplier to the top module. The RTL view of 128x128 vedic multiplier is shown in Fig.8.

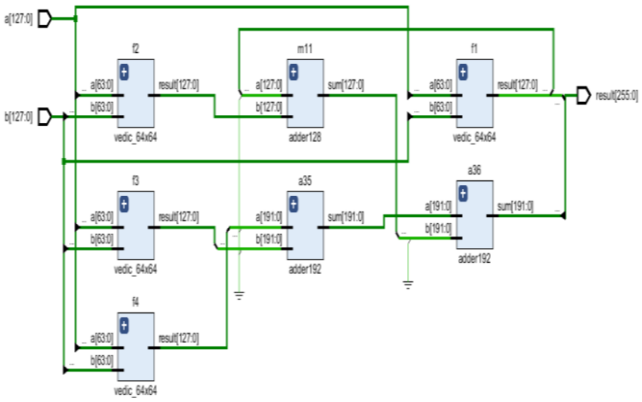


Figure 8: RTL view of 128 x 128 vedic multiplier

256x256 vedic multiplier design was completed using the above designed 128x128 vedic multiplier. In addition to the multipliers a 256 bit adder and 384 bit adder was designed. The simulation was completed using Vivado tool and the utilization report and RTL view of the design is given below.

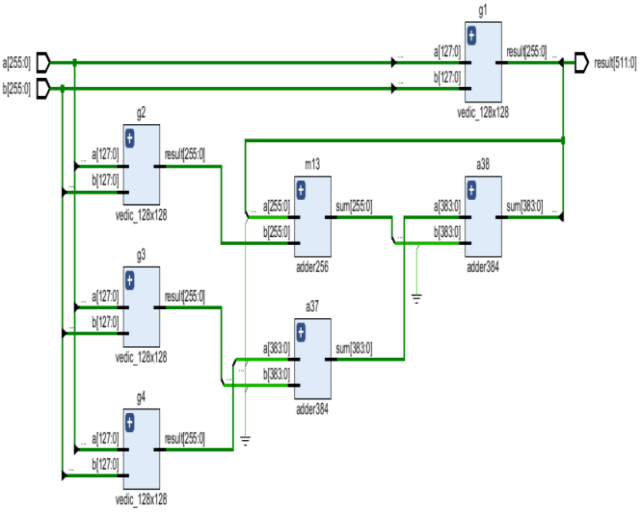


Figure 9: RTL view of 256x256 vedic multiplier

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	87233	0	41000	212.76
LUT as Logic	87233	0	41000	212.76
LUT as Memory	0	0	13400	0.00
Slice Registers	0	0	82000	0.00
Register as Flip Flop	0	0	82000	0.00
Register as Latch	0	0	82000	0.00
F7 Muxes	0	0	20500	0.00
F8 Muxes	0	0	10250	0.00

Figure 10: Utiilization report of 256x256 vedic multiplier

Table 1: Delay of multipliers

Vedic multipliers	Delay (in ns)
32 x 32	14.626
64 x 64	19.31
128 x 128	25.275
256 x 256	31.632

The table.1 shows the delay values of the vedic multipliers. As seen from the table, the delay values increase as the number of bits increases.

6. Conclusion

In this paper, the design of 256 x 256 vedic multiplier has been carried out. The design was based on lower level multipliers implemented using vedic mathematics. Unlike array multipliers and wall ace tree multiplier, which even though performs well for smaller number of bits and has limitations in terms of area and execution time, vedic multiplier implements efficiently with comparatively lesser area. Furthermore optimisation can be achieved by replacing the adder with hybrid adder or designing a new adder according to the requirement.

References

[1] V. Kunchigi, L. Kulkarni and S. Kulkarni, "High speed and area efficient vedic multiplier, " 2012 International Conference on Devices, Circuits and Systems (ICDCS), 2012, pp.360 - 364, doi: 10.1109/ICDCSyst.2012.6188747.
[2] Tiwari, H. D., Gankhuyag, G., Chan Mo Kim, & Yong Beom Cho. (2008). Multiplier design based on ancient Indian Vedic Mathematics.2008 International SoC Design Conference. doi: 10.1109/socdc.2008.4815685
[3] P. Saritha, J. Vinitha, S. Sravya, V. Vijay and E. Mahesh, "4 - Bit Vedic Multiplier with 18nm FinFET Technology, " 2020 International Conference on Electronics and Sustainable Communication Systems (ICESC), 2020, pp.1079 - 1084, doi: 10.1109/ICESC48915.2020.9155707.
[4] V. G. Pooja, B. S. Premananda and G. S. Ramesh, "Design of Compact Vedic Multiplier for High Performance Circuits, " 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), 2018, pp.1168 - 1172, doi: 10.1109/RTEICT42901.2018.9012654.
[5] Y. Bansal, C. Madhu and P. Kaur, "High speed vedic multiplier designs - A review, " 2014 Recent Advances in Engineering and Computational Sciences (RAECS), 2014, pp.1 - 6, doi: 10.1109/RAECS.2014.6799502.
[6] Y. Harshavardhan, S. Nagaraj, S. Jaahnavi and T. M. Reddy, "Analysis of 8 - bit Vedic Multiplier using high speed CLA Adder, " 2020 2nd International Conference on Innovative Mechanisms for Industry Applications (ICIMIA), 2020, pp.128 - 132, doi: 10.1109/ICIMIA48430.2020.9074953.